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FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

NOVEMBER 29, 1984

**Color palette chip
with video output
swiftly paints
a million pixels**



**Technology Report:
Tackling VLSI testing
in the design stage**

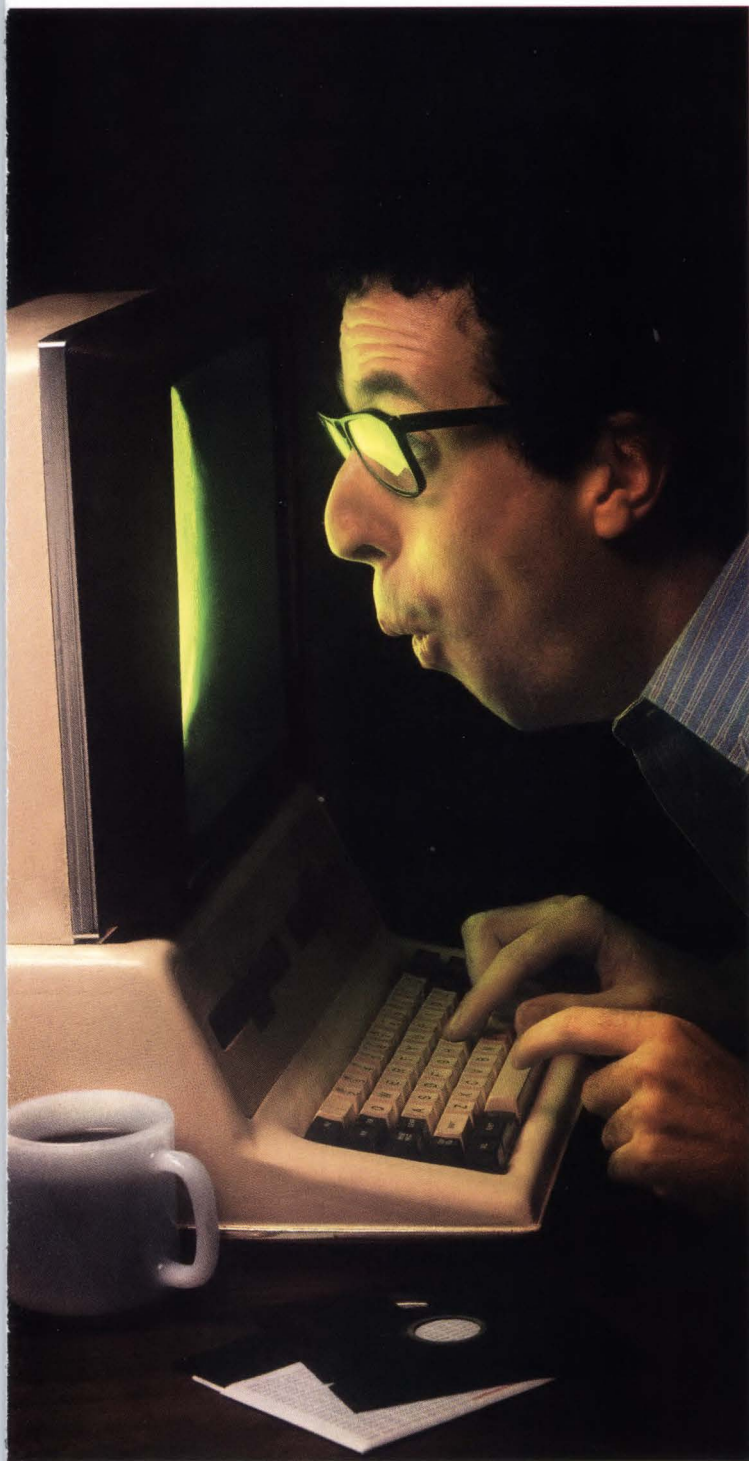
**Personal Computer
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evaluate their PCs**

**Product Report:
Focus on
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**Conference Preview:
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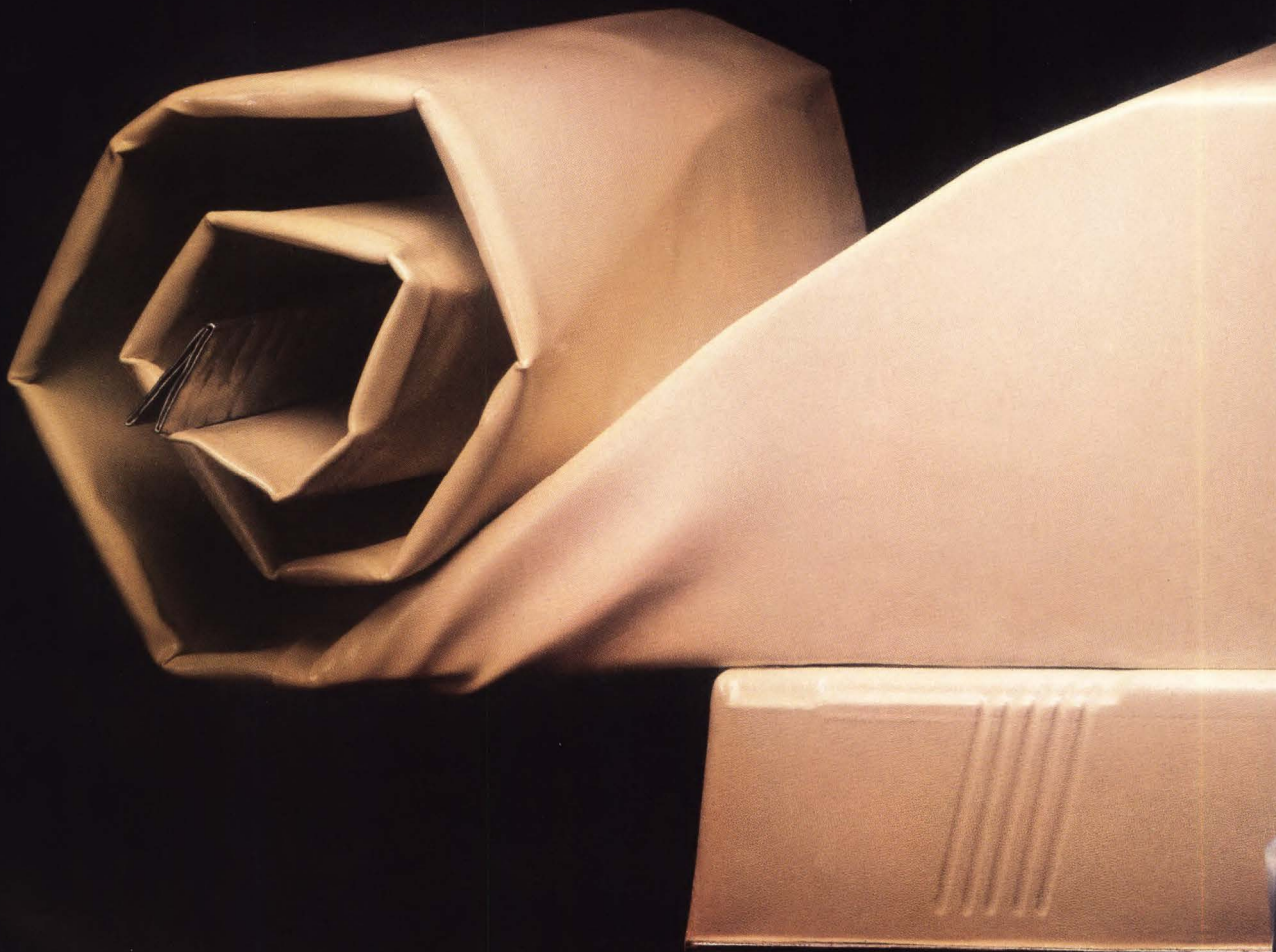
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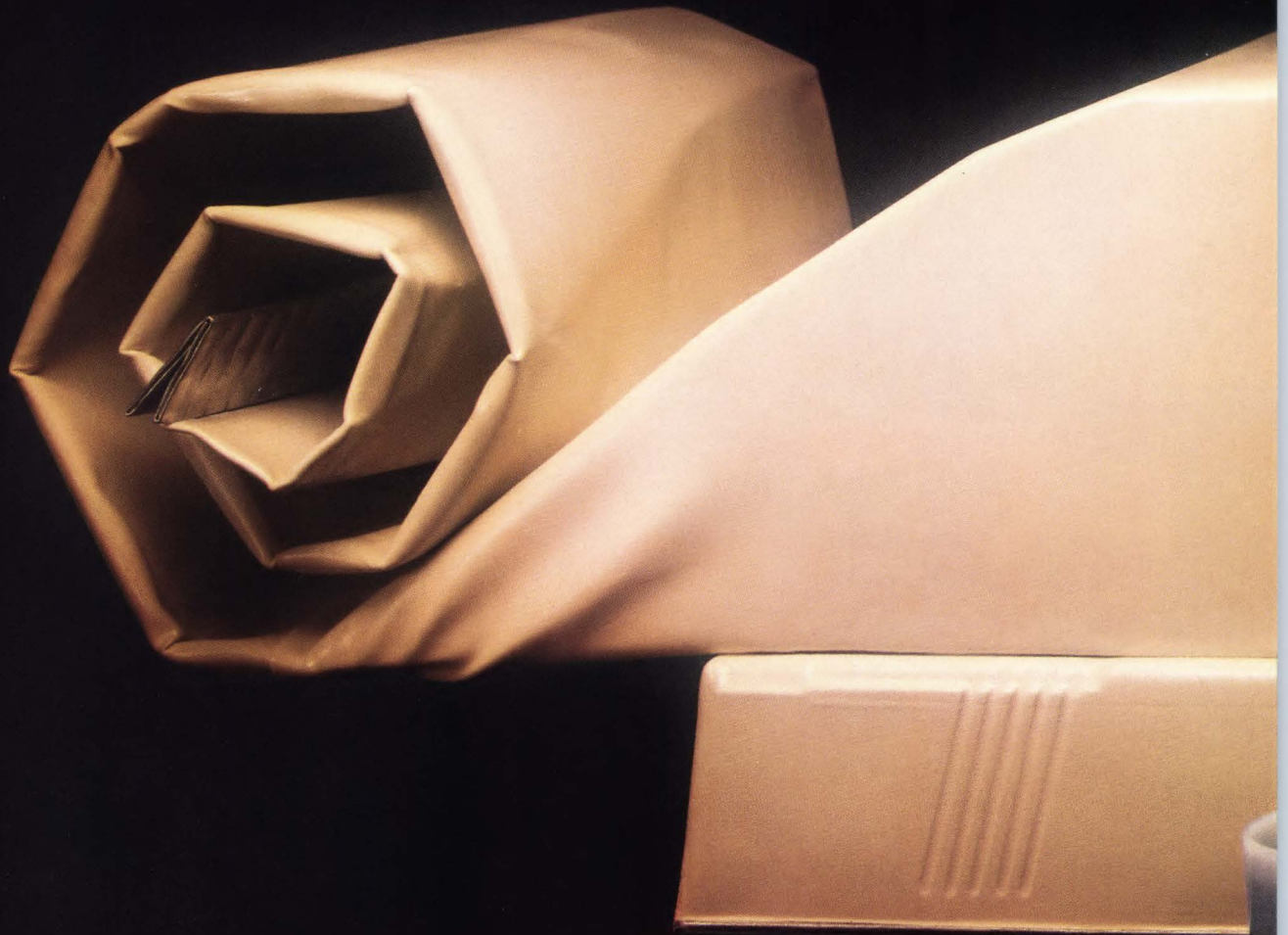
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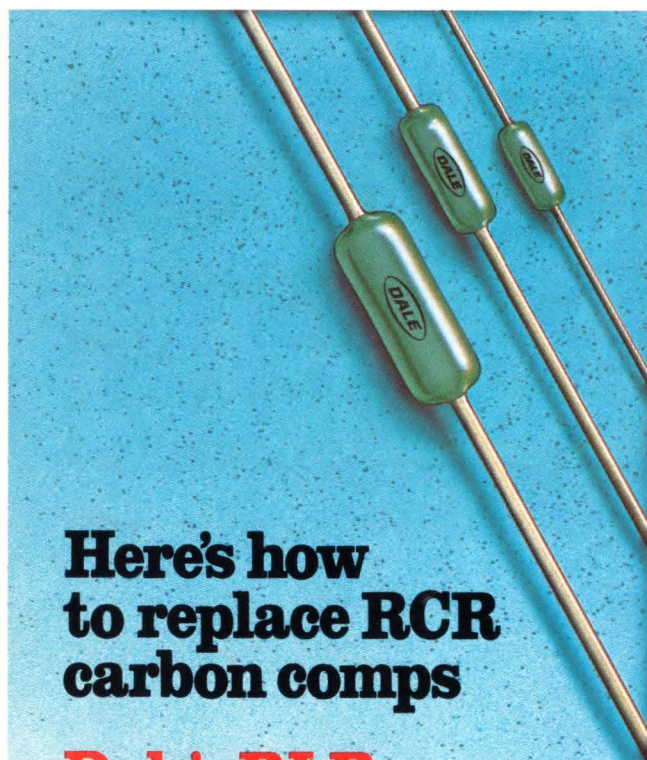
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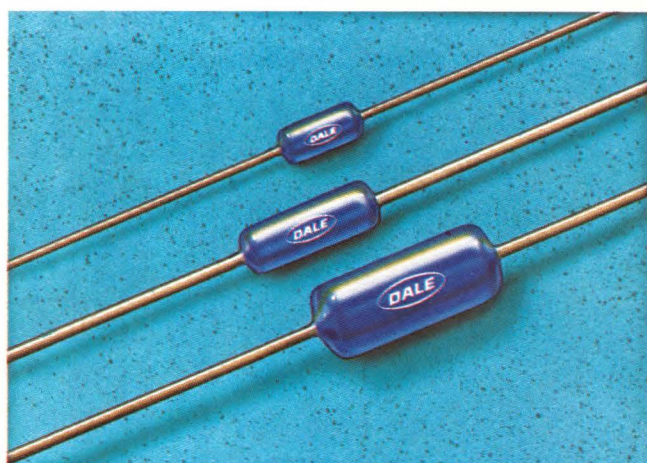
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BEHIND THE COVER

The customer is always right," asserts one business axiom, and planners at Advanced Micro Devices could not agree more. When several designers of bit-mapped graphics systems asked for a registered version of a high-speed digital-to-analog converter, the chip maker's product planners became curious. Then they made an interesting discovery: What those designers really wanted—what they needed the converter for—a color palette. In high-performance color graphics systems, a color palette creates a wealth of hues without needing a huge memory array.

The new concept fitted nicely into a plan already brewing at AMD—to blend analog and digital technologies into single ICs and then present families of those ICs as system solutions. Therefore, to launch the new plan AMD embarked on the quest for a single-chip color palette, complete with a very fast, low-glitch d-to-a converter, what it produced is described in this issue's cover story (p. 187).

For several reasons, the job turned out to be bigger than expected. At least twice, outside consultants were called in to help solve difficult problems. The palette's 103-MHz clock rate was just one of the factors that made the job interesting. In fact, the original plan called for integrating enough circuitry to drive all three color guns of a display terminal, but the heat created at such high speeds quashed that idea. Even now, the chip's high speed makes testing it a major achievement. In the midst of an intense design effort, tasks like reducing the d-a converter's glitch energy, improving its linearity, and trimming a RAM's access time were all uphill battles. In the broader picture, even the supervision of melding analog and digital technologies created problems, as ruffled engineers clashed over different design methodologies.

When the dust finally settled, however, managers and designers from the many groups involved had kept true to their goal: They had built not just what they knew how to build, but what they knew was needed and wanted by designers. Once again the customer was right.

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231 With its paged structure, a 512k EPROM relaxes system storage constraints

The limits imposed by the addressing range of today's 8-bit microprocessors are removed by a page-addressed EPROM that acts like four 128-kbit chips.

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A single TO-220 package and a common heat sink ensure that a pair of p- and n-channel power DMOS FETs remain matched as temperature changes.

257 Systolic array chip recognizes patterns quicker than a wink

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Single control adjusts variable oscillator over four decades.
Zener diode increases fixed pnp regulator's voltage ratings.
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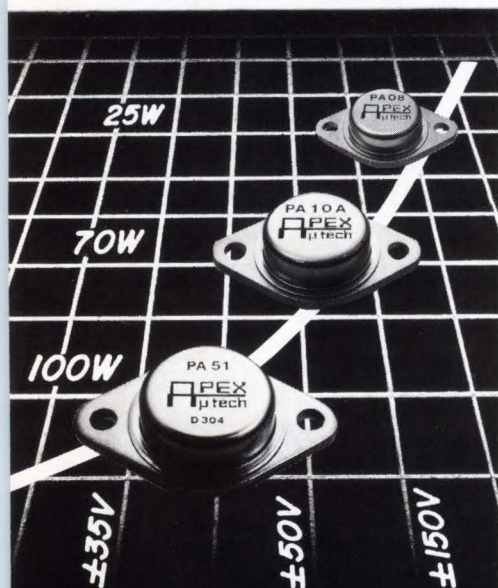
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CIRCLE 5

CONTENTS SPOTLIGHT

Testing VLSI circuits 140

The advent of VLSI circuitry makes a "leave it to testing" attitude a thing of the past: As our Technology Report demonstrates, testability begins with design. In fact, share and share alike may ultimately be the motto of designers and test engineers. The latter are drawing on the designer's bag of tricks to streamline the modeling of faulty circuits. For their part, designers are using simulators and test program generators to create better and more testable ICs.

Personal Computer Series 161

The first in a two-part survey of ELECTRONIC DESIGN'S readers focuses on the types of personal computer-based workstations favored and the range of jobs they are being asked to do. Not surprisingly, given the effect that personal machines have had over the last five years, PCs are being pressed into service across the board by both engineers and engineering managers.

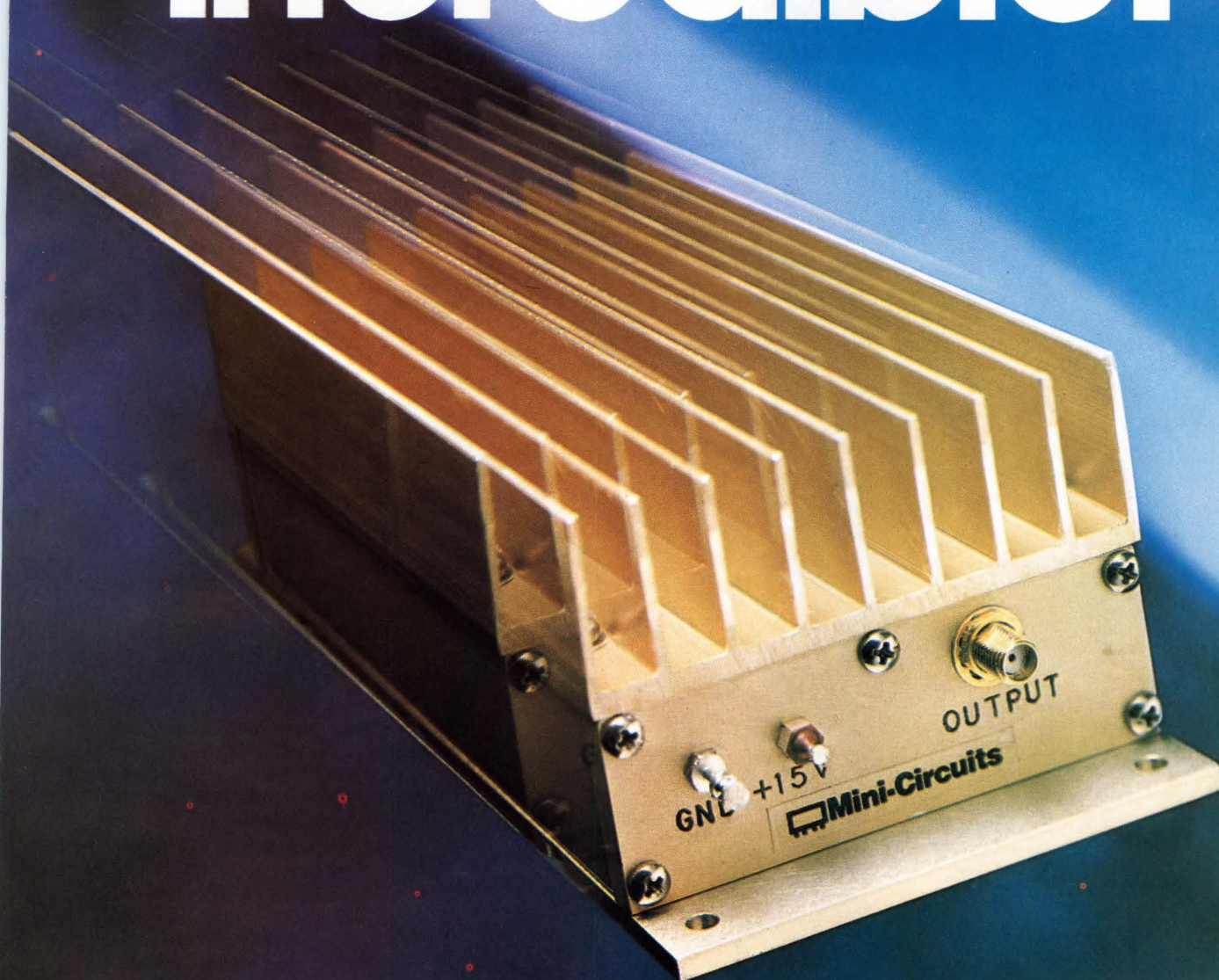
Cover: Color palette chip 187

The color palette approach is well known to designers of graphics systems as a way to keep memory requirements in check: Now a single IC puts an astonishing 16.8 million hues at a designer's disposal. What's more, the color palette chip is the central element of a graphics set that also includes a display refresh controller, a video shift register, and a video timing controller (p. 208).

Conference Preview: IEDM 73

Memories are regularly cited as the first beneficiaries of process advances, and this year's International Electron Devices Meeting proves no exception to that rule. But as memories go, so goes the industry: Semiconductor sensors, for instance, are also taking advantage of new processing techniques, picking up speed and uses in the bargain. And the once-arcane silicon-on-insulator technology may soon be called into service to supply low-cost dielectric isolation.

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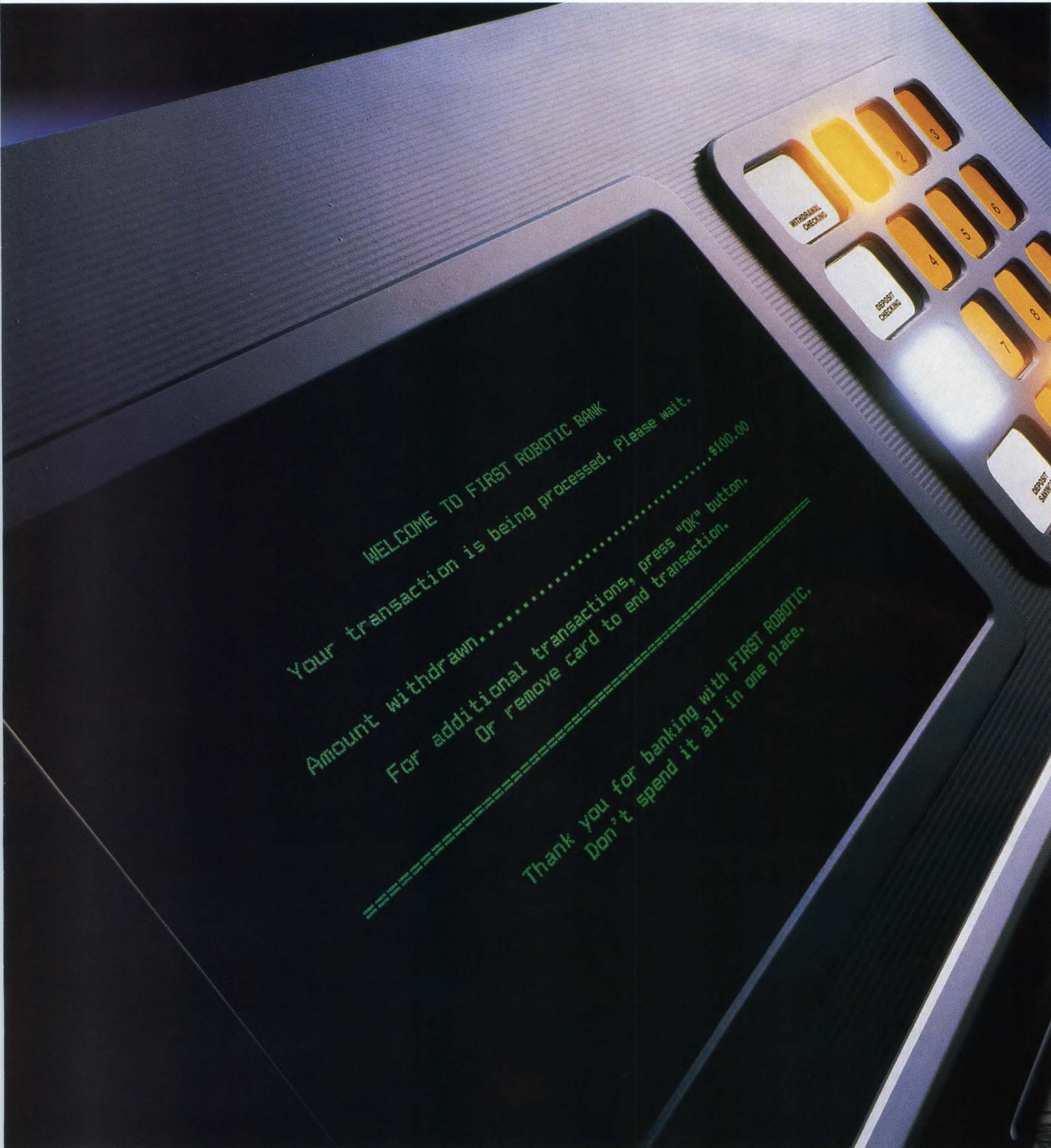
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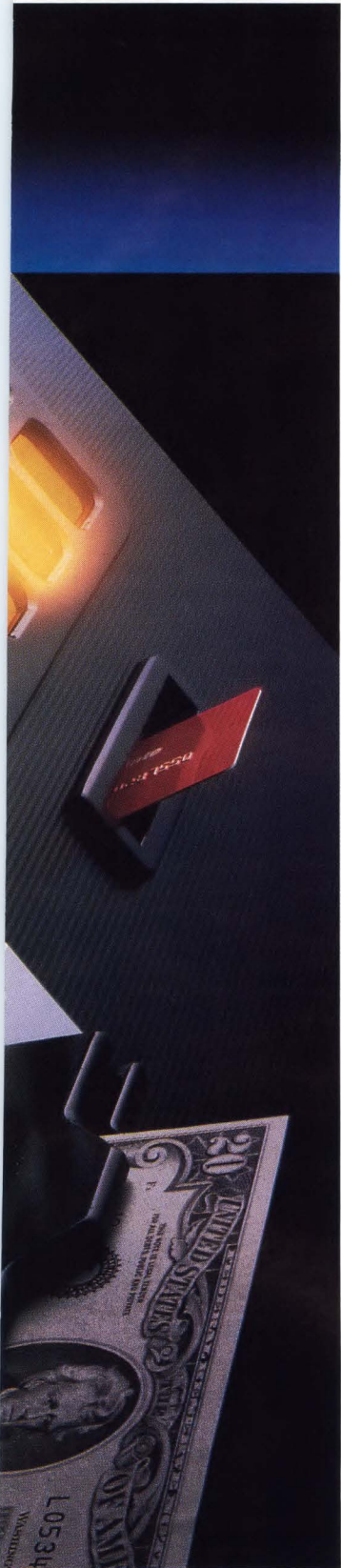
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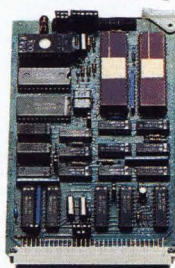
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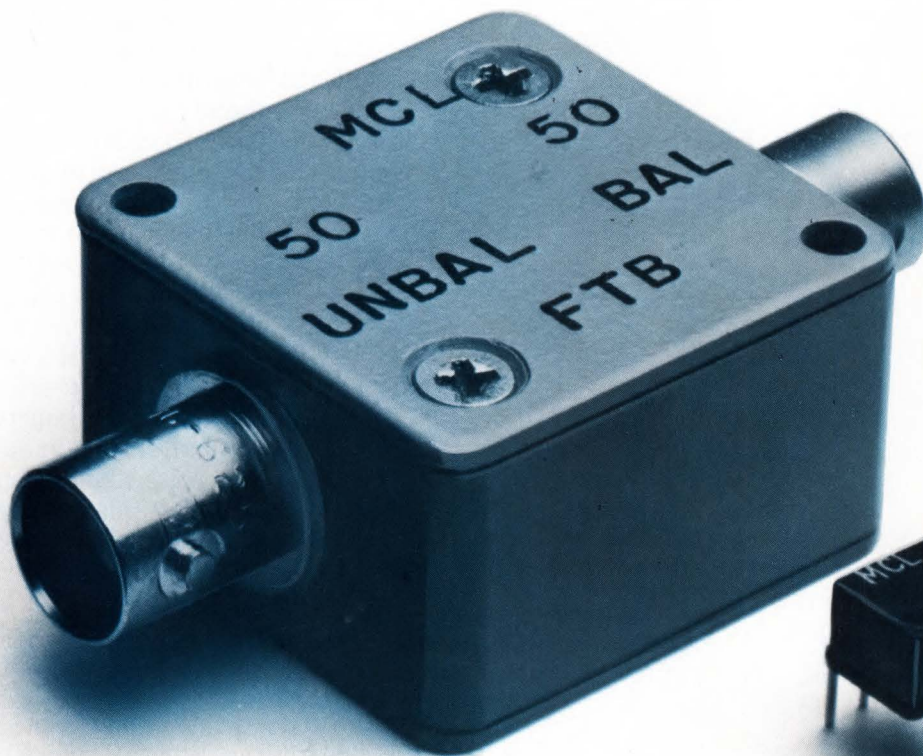
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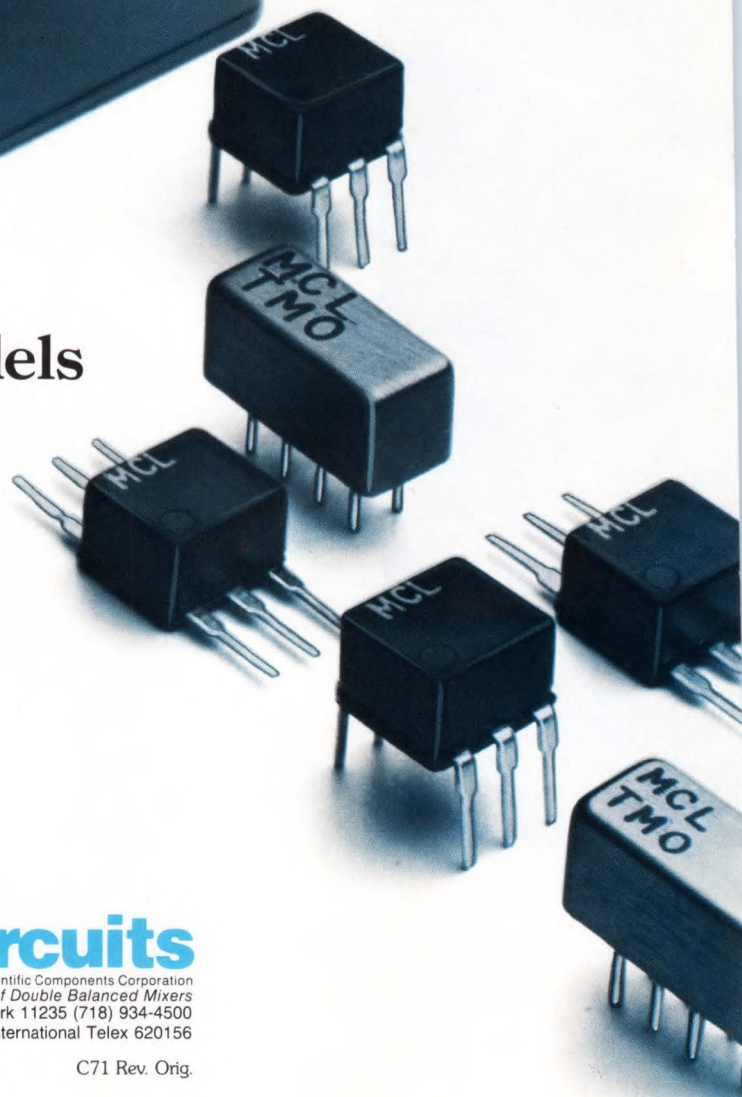


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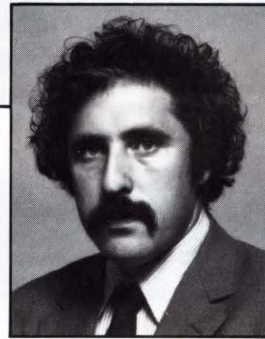
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CIRCLE 8

C71 Rev. Orig.

ON REFLECTION

Optical-disk drives may soon rival Winchesters, floppies



For years, Winchesters and floppy-disk drives have been dropping in size and picking up speed and density. But magnetic storage, despite these enhancements, could well be replaced by optical disks in most instances.

Optical platters are already on the scene that retain hundreds of megabytes. Philips and 3M, for instance, have just unveiled a 600-Mbyte read-only optical disk that is a mere 100 mm in diameter. The drive hits a transfer rate of greater than 1.41 Mbits/s and can be accessed in less than 2 seconds. Although the unit can only be read, its extremely low price and extensive storage should make it particularly attractive for archival purposes.

In contrast, 8-in. Winchesters can hold up to 100 Mbytes, and their access times come in at roughly 30 ms. Transfer rates are in the neighborhood of 10 Mbits/s. Although improvements are expected, the 8-in. Winchester will probably store under 300 Mbytes for many years to come, and experts have estimated that its recording density is limited to 100 Mbits/in.². Floppy disks hold even less: A 5¼-in. drive can be pushed to 6.6 Mbytes. And even with work, the capacity of 5¼-in. floppies is estimated at about 12 Mbytes.

But optical technology is not limited to read-only drives. Last year, Shugart's Optimem Division announced a unit that both reads and writes. This 1-Gbyte drive achieves densities of 225 Mbits/in.² and records data by increasing the intensity of its read/write laser diode. It transfers information at 10 Mbits/s and accesses in 450 ms. Already, system integrators are using this optical read/write ability to back up less dense magnetic devices, as well as applications where document retrieval and im-

age retention are important.

Further, with appropriate file management, the high density of optical disks can compensate for the fact that—at least for now—they cannot be erased. The greatly increased capacity of optical disks lets updated files be recorded onto fresh disk areas and data stored earlier to be retained for reference.

Moreover, even erasability is on the horizon for optical disk drives. Panasonic is working on a tellurium suboxide disk that delivers this ability. Additionally, Philips Research Laboratories has created an erasable prototype by working with magneto-optics. An optical disk that can be read from, written to, and erased should be here by 1986.

In short, optical storage, with its significantly higher capacity and comparable data transfer rates, definitely holds out the promise of displacing Winchesters and floppies. Access times, which are typically longer because optical disks hold so much more, will likely decrease as work continues. Also, optical drives can probably use the very same controllers as standard Winchesters.

Before long, most computer users will think back nostalgically to the days when they had to buy floppy disks by the box, and they will fondly recall today's Winchester drives in much the same manner as core memory is remembered. There can be little doubt that optical disks are only beginning to make good on their bright promise.

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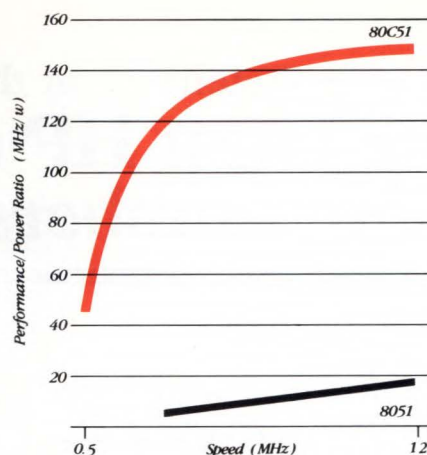
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to factory line powered controllers, to portable communications systems. A military version of the 80C51 will be available soon.

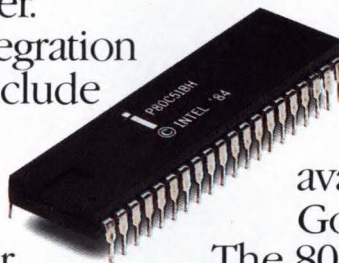
The 80C51 also boasts the world standard in development tools. Like the Series II/ICE™-51 emulator and the iPDS™ system/EMV-51. As well as a relocatable assembler and high level languages.

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CIRCLE 9



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READER FEEDBACK

Silicon compilers need standard benchmarks

I appreciated your Sept. 20 News Analysis of silicon compilation [p. 67]. I realize that because of the lack of standard nomenclature, it is a very difficult subject to write about, but I feel that in general you have done a commendable job. I would like, however, to comment on one particular section because it brings out an important issue for our industry and the practicing engineers who are your readers.

In your article, MetaLogic's compilation time was quoted for a microprocessor chip, whereas another compilation time was quoted for 30,000 transistors. No market exists for "30,000 transistors."

For example, simply "compiling" a ROM or a PLA in a few minutes is not in itself astounding or even useful. The system designer must still come up with the program for the PLA, which is one of the things MetaSyn does in its three hours (two with the latest version).

If compilation time only is to be used as a basis for comparison, the time should be measured for the same finished product. However, an even better measure would be total design time (again, for the same product).

The same extensions could be made for other measures currently being used for comparison, such as density or

clock rate. Instead of comparing the number of transistors per square millimeter, compare the functions per chip; and instead of clock cycle time, use function execution time.

Unlike comparisons are not a new problem. Minicomputer manufacturers used to provide meaningless statistics for "add instruction execution times" that had been calculated on the basis of totally unreasonable conditions. Today, however, these manufacturers typically quote performance in Whetstones, performance for an arbitrary, but nonetheless plausible, scientific algorithm.

Think of what it would mean if we could adopt the same type of benchmark measures for silicon compilers. A set of specific application requirements could be developed (from digital signal-processing or real-time control systems, for example) and used as an industry-wide standard.

Once these standards have been selected, all compilers could be graded on the bases of the speed of the design process and implementation efficiency and adequacy. Thus we would have more effective grounds for comparison.

I realize that we are dealing with a relatively new field, it and as with any new field, it takes time to develop standards in everything from nomenclature to methods of comparison. However, stan-



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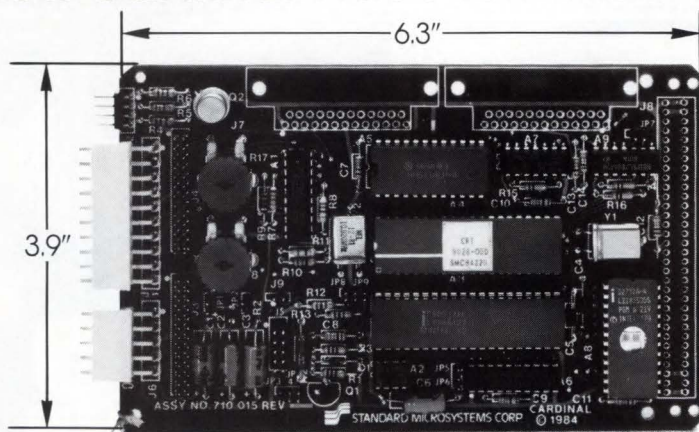
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CIRCLE 10

Check out the numbers on our new Cardinal Video Terminal Board.



If you're a systems designer looking to save space and money, Standard Microsystems has your number: the new Cardinal Video Terminal Controller Board. The Cardinal meets the Eurocard Form Factor (3.9" x 6.3") and is priced below \$200. Yet, it has a host of big system features, including thin and wide graphics, smooth scrolling, video attributes, full/half duplex operation and a menu-driven setup mode stored in a non-volatile memory. In fact, the Cardinal is so advanced, you only have to add a power supply, keyboard and video monitor to build a complete video display terminal. To find out more, contact Standard Microsystems Corporation, 35 Marcus Blvd., Hauppauge, NY 11788. (516) 273-3100.

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CIRCLE 11

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CIRCLE 12

READER FEEDBACK

dards are nonetheless important.

Jay R. Southard
Vice President
MetaLogic Inc.
Cambridge, Mass.

Corrections

The Design Solution "Isolation Amp Drifts ± 5 mV over 8 Hours" (Oct. 18, p. 258) incorrectly indicates that the voltage gain of the second stage is six. In fact, that is the overall gain of the entire circuit.

Because of a mistake on the company's literature, our Oct. 31 write-up of the ME090 switching power supply from MicroEnergy Inc. (p. 396) gave the wrong telephone number. The correct phone number is (312) 620-8101.

Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Editor, Electronic Design, 10 Mulholland Dr., Hasbrouck Heights, N.J. 07604. Try to keep letters under 200 words. Letters must be signed. Names will be withheld upon request.

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FOR TEXAS INSTRUMENTS,
CIRCLE 13 →



Texas Instruments digital signal processor helps Lear Siegler Inc. make your message loud and clear...from anywhere.

- TI's single-chip, high-performance TMS32010 digital signal processor (DSP) assures highest quality telephone transmission (Page 2).
- TMS320 DSPs from TI support high-speed and numeric-intensive applications from communications to seismic processing (Page 3).
- Complete development support for TI digital signal processors includes hardware, software, documentation, and application workshops (Page 4). ►

TI digital distortion

When you're depending on the telephone to get your message through, you don't need "singing" on the line. A standard two-wire circuit "sings" when signals traveling in opposite directions are insufficiently isolated in a repeater. To eliminate this problem, Lear Siegler, Inc., manufacturer of repeaters used worldwide, relies on the Texas Instruments TMS32010 digital signal processor (DSP). And cuts setup time for each repeater from hours to minutes.

In the unique VFR-7608 repeater, TI's TMS32010 performs all the functions of analog equalizers, filters, and amplifiers (see diagram opposite). It compensates automatically for line impedance 8,000 times per second. Completely isolates the opposing signal streams. Puts an end to "singing."

TMS32010 eliminates reflections "by the numbers"

The standard solution to "singing" is an analog network designed to cancel out reflected signals on the line. But even with expensive "precision" hybrids, the best solution is a compromise that limits usable bandwidth and gain.

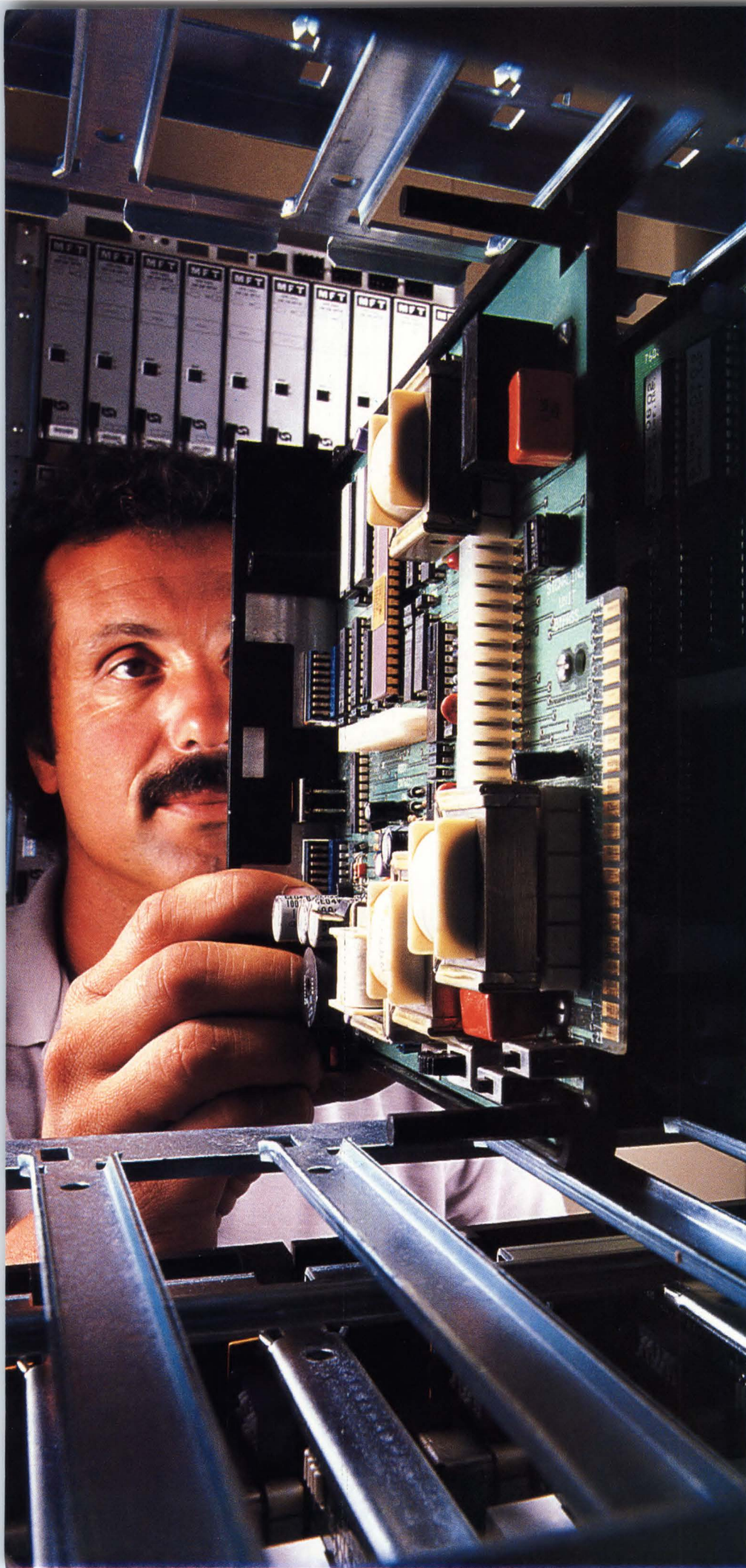
Digital signal processing with the TMS32010 balances the circuit across the entire frequency band every 125 μ s. Because the repeater adapts continuously, the circuit cannot "sing" at any frequency, and its gain can be fully utilized.

DSP cuts setup time to minutes

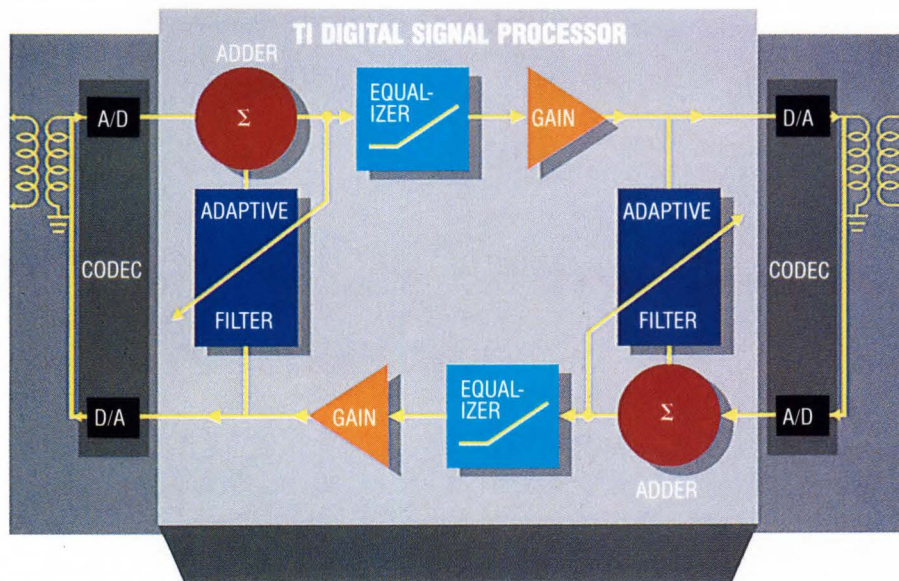
Tuning each analog repeater is an hours-long, trial-and-error procedure for a highly skilled technician. Using a comprehensive history of each circuit, he must set 68 switches in an analog repeater. TI's TMS32010 in Lear Siegler's new digital repeater eliminates 65 of those switches. Ends the need to keep detailed circuit histories. And the small, affordable plug-in unit is interchangeable with older repeaters.

So your message can always come through—loud and clear.

- ◀ **Setup is as simple as 1-2-3** with Lear Siegler's adaptive telephone repeater using TI's TMS32010 DSP. Whereas manual adjustment of an analog repeater can take many hours, only three simple switch settings are required to assure rock-stable, "sing"-free performance from the digital repeater.



signal processor squelches in unique adaptive repeater.



Heart of the adaptive repeater is TI's single-chip, 16/32-bit TMS32010 digital signal processor. All the functions shown are achieved in real time through software operating on signals digitized by conventional single-chip codecs.

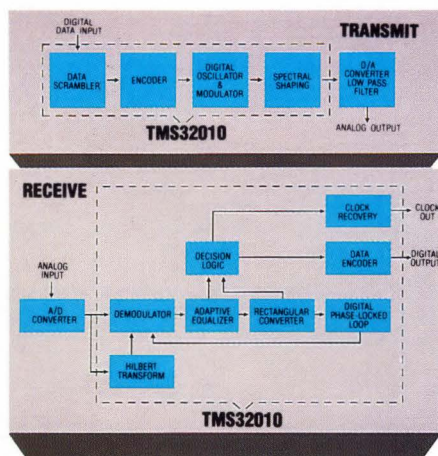
The TMS320 family from Texas Instruments: "Workhorse of digital signal processing."

The TMS32010, first member of the TMS320 DSP family, is TI's trailblazing contribution to an important new technology. A Lear Siegler engineer who has been following the progress of digital signal processing from its inception says, "The TMS32010 is the first device that can reliably do what we need. It's a real workhorse: The '8080' of DSP."

TI's TMS320 DSPs excel at high-speed, numeric-intensive applications

High-performance TMS320-family DSPs from Texas Instruments will find widespread use in many fields where large volumes of high-speed computation are required. In telecommunications, they can also be used to build high-speed modems with data-transmission rates up to 9,600 baud. They can make speech recognition, analysis, and synthesis practical. Speed image processing and pattern recognition. Facilitate high-speed process control and instrumentation. Process radar, sonar, and seismic signals. And furnish the multiple functions often required for a single application.

For example, a TMS320 DSP could enable an industrial robot to synthesize and recognize speech, sense objects and their orientation, and perform mechanical operations through digital servo-loop computations.



High-speed modem functions are effectively performed by TI's TMS32010, as well as such expanded functions as auto-dial/answer, dial-tone verification, busy-signal detection, and self-test routines.

The TMS320 family, with its extensive development support (see page 4), can handle all the signal processing for spectrum analysis: Autocorrelation, windowing, fast Fourier transforms—performing a 64-complex-point FFT in only 550 μ s. And for seismic processing involving very low frequencies which only a digital system can implement.

Image enhancement, pattern recognition, and data compression are all possible with TMS320 processors. They can extract features and perform template comparisons for optical character recognition.

A one-chip alternative to bit-slice processing

TI's 16/32-bit TMS320 DSPs offer an inexpensive alternative to multichip bit-slice processors. They combine the flexibility of a high-speed controller with the numerical capability of an array processor—on a single chip, in one 40-pin DIP.

Highly pipelined architecture and a comprehensive instruction set give the TMS320 the speed to execute five million instructions per second with 32-bit precision: More than fast enough, for example, to handle the 40 additions and 40 multiplications necessary for realtime voice-frequency processing within the 125- μ s sampling interval. A conventional microprocessor, operating at 8 MHz, would require 900 μ s, and quickly become bogged down in the signal stream.

Now in three versions

The TMS32010 microprocessor has 288 bytes of on-chip data RAM, and can address up to 8K bytes of off-chip memory at full speed.

The TMS320M10 microcomputer is identical to the TMS32010, but it also includes 3K bytes of on-chip mask-programmed ROM.

The military version, SMJ32010JDS, is processed to the extended temperature range requirements of MIL-STD-883B.

To learn more about the many applications and available development support for TMS320-family DSPs, return the coupon on the following page.

See back page for more information.





In-depth support for the TMS320 family of TI DSPs includes a host-independent development system, an evaluation module, emulator and analog interface board, as well as assembler/linkers and simulators that can run on a variety of host computers and PCs. Documentation is extensive and thorough.

Develop your own DSP applications with comprehensive support from TI.

Texas Instruments has assembled an extensive group of development-support packages for the TMS320 family of VLSI digital signal processors (see table). Included are all the hardware, software, and documentation you need to utilize the power and speed of TMS320 DSPs in your designs. A rapidly growing volume of third-party support is also available.

Use your own PC as a TMS320 development station

The latest addition to TI's development-support software is the TMS32010 Digital Filter Design Package developed by Atlanta Signal Processors Inc. It makes your Texas Instruments Professional Computer or IBM PC a cost-effective, easy-to-use, digital-filter design

TMS32010 Software and Hardware Support

Host Computer	Operating System	Part Number
Macro Assembler/Linkers		
TI990	DX10	TMDS3240120-08
DEC VAX	VMS	TMDS3240210-08
DEC VAX	Berkeley UNIX 4.1	TMDS3240220-08
DEC VAX	Berkeley UNIX 4.2	TMDS3240230-08
IBM	MVS	TMDS3240310-08
IBM	CMS	TMDS3240320-08
TI/IBM PC	MS-DOS	TMDS3240810-02
Simulators		
DEC VAX	VMS	TMDS3240211-08
TI/IBM PC	MS-DOS	TMDS3240811-02
Hardware		
Evaluation Module (EVM)		RTC/EVM320A-03
Analog Interface Board (AIB)		RTC/EVM320B-06
Emulator		TMDS3262210

station. With it you can produce the TMS32010 source module. Then you can assemble the code and simulate it in software on the PC. Later you can download the code into the hardware-development system for realtime emulation.

Two versions are now available: **DFDP-TI001** for the Texas Instruments Professional Computer, and **DFDP-IBM001** for the IBM PC.

Learn in TI workshops

Texas Instruments supplies comprehensive documentation with each device. A growing library of application reports will also assist you in the design of digital signal processing circuits using TI's TMS320 DSPs.

Three-day DSP workshops, including extensive hands-on experience, are conducted periodically at Texas Instruments Regional Technology Centers. For registration information, call the Regional Technology Center nearest you: Atlanta, (404) 452-4686; Boston, (617) 890-4271; Chicago, (312) 228-6008; Dallas, (214) 680-5096; Northern California, (408) 980-0305; Southern California, (714) 660-8164.

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Please send me information about:

- PR 22 ☐ TI's TMS320 family of Digital Signal Processors.
PR 24 ☐ Third-party support for the TMS320 family.

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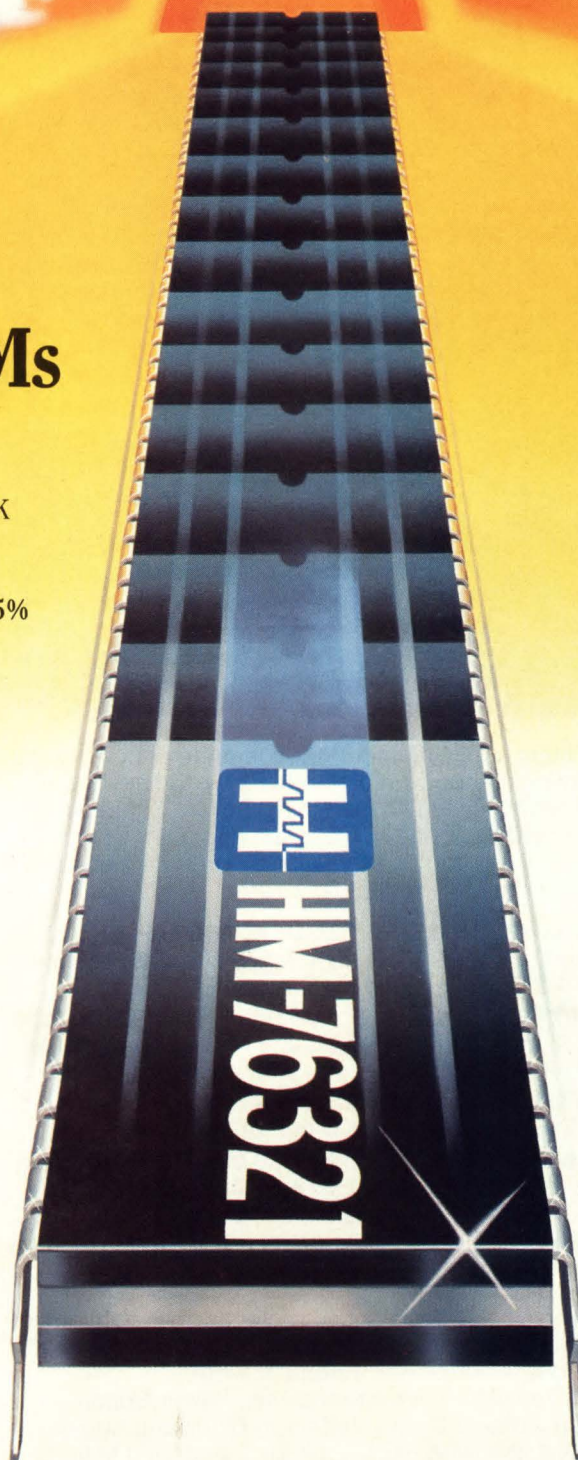
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Digital Avionics Systems Conference (6th DASC), Dec. 3-6. Baltimore Convention Center, Baltimore, Md. AIAA, 1633 Broadway, N.Y. 10019; (212) 581-4300.

Real-Time Systems Symposium, Dec. 4-6. Hyatt Regency Hotel, Austin, Texas. Mirosław Malek, Department of Electrical Engineering, University of Texas, Austin, Texas 78712; (512) 471-5704.

Western Design Engineering Show, Dec. 4-6. Moscone Center, San Francisco, Calif. Western Design Engineering Show, 999 Summer St., Stamford, Conn. 06905; (203) 964-8287.

The First Conference on Artificial Intelligence Applications, Dec. 5-7. Sheraton, Denver Tech Center, Denver, Colo. Conference on Artificial Intelligence Applications, PO Box 639, Silver Spring, Md. 20901; (301) 389-8142.

1984 IEEE International Electron Devices Society (IEDM), Dec. 9-12. San Francisco Hilton and Towers, San Francisco, Calif. Melissa Widerkehr, Courtesy Associates Inc., 655 15th St. NW, Suite 300, Washington, D.C. 20005; (202) 347-5900.

Computer Networking Symposium, Dec. 10-11. Gaithersburg, Md. Robert Rosenthal, NBS, B226 Technology Building, Gaithersburg, Md. 20899; (301) 921-3516.

Dexpo West '84, Dec. 11-14. Disneyland Hotel, Anaheim, Calif. Expoconsul International Inc., 55 Princeton-Hightstown Road, Princeton Junction, N.J. 08550; (609) 799-1661.

IEEE First International Conference on Office Automation, Dec. 17-19. New Orleans Hilton, New Orleans, La. IEEE First International Conference on Office Automation, c/o Dr. Donald Kraft, Department of Computer Science, Louisiana State University, Baton Rouge, La. 70803; (504) 388-1495.

1985 International Winter Consumer Electronics Show, Jan. 5-8. Las Vegas, Nev. Dennis Corcoran, CES, 2001 Eye St. NW, Washington, D.C. 20006; (202) 457-8700.

PC Fab Expo '85, Jan. 8-10. Sheraton Twin Towers Hotel, Orlando, Fla. Julia Wilson, PMS Industries, 1790 Hembree Road, Alpharetta, Ga. 30201; (404) 475-1818.

Automated Test Equipment West Conference (ATE), Jan. 14-17. Anaheim Convention Center, Anaheim, Calif. Morgan-Grampian Expositions Group, 2 Park Ave., New York, N.Y. 10016; (212) 340-9780.

Caldon West '85, Jan. 14-17. Anaheim Convention Center, Anaheim, Calif. Morgan-Grampian Expositions Group, 2 Park Ave., New York, N.Y. 10016; (800) 782-0009.

1985 Measurement Science Conference, Jan. 17-18. Marriott Hotel, Santa Clara, Calif. Darlene Diven, Lockheed Missiles and Space Co., PO Box 3504, Sunnyvale, Calif. 94088; (408) 756-0270.

Uniform, Jan. 21-25. Infomart, Dallas, Texas. Pemco, Inc., 2400 E. Devon Ave., Suite 205, Des Plaines, Ill. 60018; (800) 323-5155.

1985 Society for Computer Simulation (SCS) Multiconference, Jan. 24-26. Bahia Hotel, San Diego, Calif. SCS, PO Box 2228, La Jolla, Calif. 94038; (619) 459-3888.

Communication Networks Conference and Exposition, Jan. 28-31. Washington Convention Center, Washington, D.C. Louise Myerow, CW/Conference Management Group, 375 Cochituate Road, PO Box 880, Farmingham, Mass. 01701; (617) 879-0700 or (800) 225-4698.

4th International Symposium on Semiconductor Processing, Jan. 28-31. San Jose, Calif. Dinesh Gupta, Siliconix Inc., 2201 Laurelwood Road, Santa Clara, Calif. 95054; (408) 988-8000 or Thomas Kochaba, ASTM, 1916 Race St., Philadelphia, Pa. 19103; (215) 299-5560.

Mini/Micro West, Feb. 5-7. Anaheim Hilton Exposition Center, Anaheim, Calif. Electronics Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045; (213) 772-2965.

(continued on p. 25)

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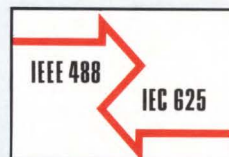
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U.S. MEETINGS

(continued from p. 23)

Conference on Optical Fiber Communication (OFC '85), Feb. 11-13. Town and Country Hotel, San Diego, Calif. Optical Society of America, 1816 Jefferson Place NW, Washington, D.C. 20036; (202) 223-8130.

IEEE International Solid-State Circuits Conference, Feb. 13-15. New York Hilton Hotel, New York, N.Y. Lewis Winner, ISSCC, 301 Almeria, Coral Gables, Fla. 33134; (305) 446-8393.

Integrated Machine Loading/Material Handling Systems Seminar, Feb. 19-21. Holiday Inn Livonia-West, Detroit, Mich. John R. McEachran, SME, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-1500, Ext. 382.

Automated Design and Engineering for Electronics Conference and Exhibition (ADEE), Feb. 26-28. Anaheim Hilton and Towers, Anaheim, Calif. Cahners Exposition Group, Cahners Plaza, 1350 E. Touhy Ave., PO Box 5060, Des Plaines, Ill. 60018; (312) 299-9311.

Nepcon West '85, Feb. 26-28. Convention Center, Anaheim, Calif. Nepcon West '85, 1350 E. Touhy Ave., Des Plaines, Ill. 60018; (312) 299-9311.

American Institute for Design and Drafting (AIDD) Exposition, March 3-8. Albert Thomas Convention Center, Houston, Texas. Philip Nowers, AIDD National Headquarters, 901 N. Washington St., Suite 509, Alexandria, Va. 22314; (703) 548-1263.

Interface '85, March 4-7. Georgia World Congress Center, Atlanta, Ga. The Interface Group Inc., 300 First Ave., Needham, Mass. 02194; (617) 449-6600.

Southcon '85 and Mini/Micro Southeast, March 5-7. Georgia World Congress Center, Atlanta, Ga. Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045; (213) 772-2965.

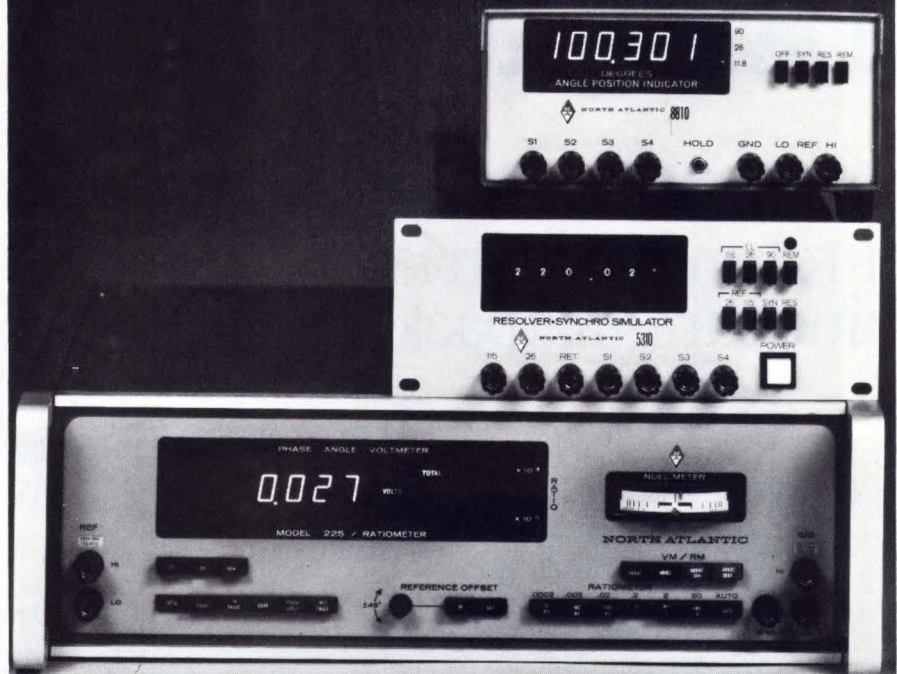
Integrated Services Digital Networks Exposition (ISDN '85), March 6-8. Bally's Park Place Casino Hotel, Atlantic City, N.J. Joan Barry, Information Gatekeepers Inc., 214 Harvard Ave., Boston, Mass. 02134; (617) 232-3111.

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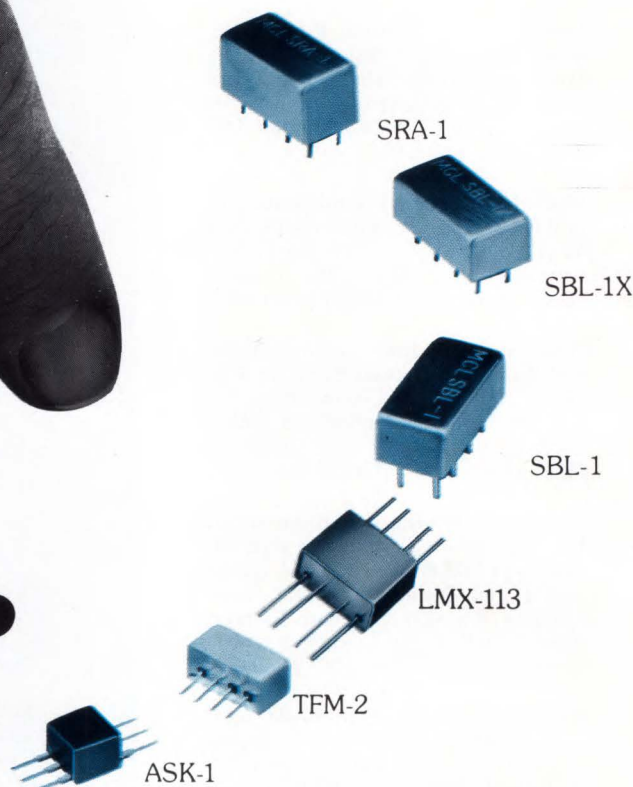
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SBL-1	world's lowest cost industrial mixer, only \$4.50, metal case	1-500	DC-500	5.5 typ.	6.5 typ.	50 typ.	45 typ.	35 typ.	3.95 (100) 4.50 (10-49)
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PERSONALLY SPEAKING



As flat panels move in, how long can CRTs hold sway over PCs?

A battle is brewing among a handful of flat-panel technologies: the goal, unseat the CRT as the dominant display for personal computers. A similar struggle took place in the early 1970s, when liquid crystals, LEDs, and gas-discharge tubes were fighting to become the preeminent display for instruments, calculators, and watches. Today's competition involves LCDs, electroluminescent panels, plasma displays, and even vacuum-fluorescent tubes. Interestingly, it revolves around some of the same issues—power dissipation, availability of driver circuitry, and cost. But there is now another factor to consider, the ability to deliver thousands of pixels.

Large arrays of LCDs, for instance, dissipate power that is measured in milliwatts, making them ideal for the new portable computers. Nevertheless, they cannot yet deliver the extremely large numbers of pixels demanded by high-resolution screens. To push LCDs to the forefront, projects are afoot investigating the use of an active thin-film transistor or a diode-switching element to create each pixel. That should not only solve resolution problems but improve viewing angle as well.

Traditionally, electroluminescent panels, which first saw the light of day nearly a decade ago, have not been commercially viable because of their power consumption, manufacturing cost, and lack of driver circuitry. Despite these historical drawbacks, the vast development efforts under way here and in Japan appear to be on the verge of turning the tide in favor of these flat panels.

Having the driver circuitry for electroluminescent panels more readily available and cutting back on their power dissipation should help reduce their manufacturing cost. With an

average power consumption of between 6 and 8 W, electroluminescent panels still draw far less power than do CRTs. The latter usually come in at around 30 W.

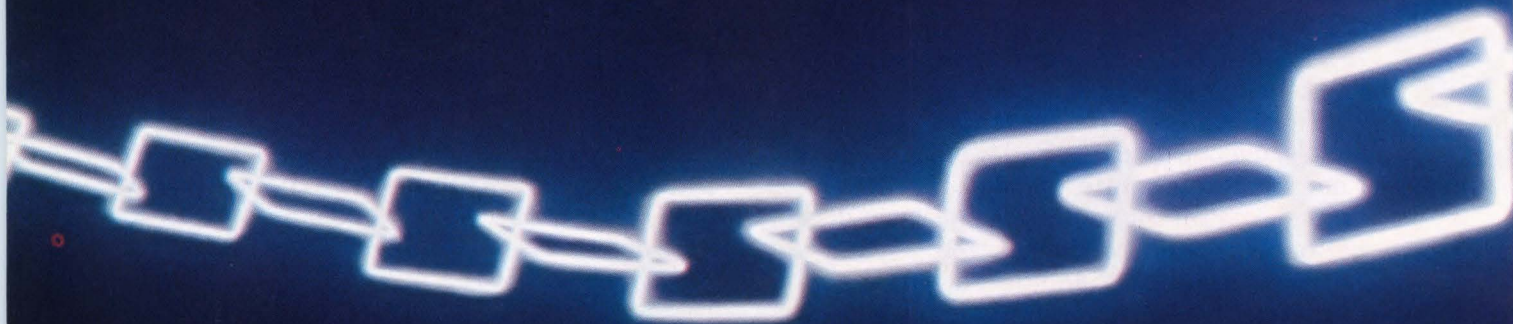
As far as the more mature vacuum-fluorescent and plasma panels are concerned, efforts now in progress will push these technologies to be more competitive with newer approaches. Cathode materials, for example, are being devised that improve the brightness of a display, thus boosting its legibility. The goal for plasma panels is to reduce power consumption from a high of 30 to less than 10 W; upgrade brightness from 30 to 50 fLs, and shrink the size of these traditionally bulky components from 35 to 9 mm.

Overall improvements in manufacturing costs—for all flat panels—should result from work in driver circuitry. Drivers are starting to emerge that employ NMOS to handle high voltages and CMOS for logic—all on one chip. To keep down the price of vacuum-fluorescent assemblies, bare driver chips will be bonded directly onto the glass substrates.

No matter which flat-panel technology wins out, one thing is for certain: We'll be seeing a new generation of personal computers. Portable and no thicker than an attaché case, these machines will boast a 12-in. or larger 80-character-by-25-line panel.

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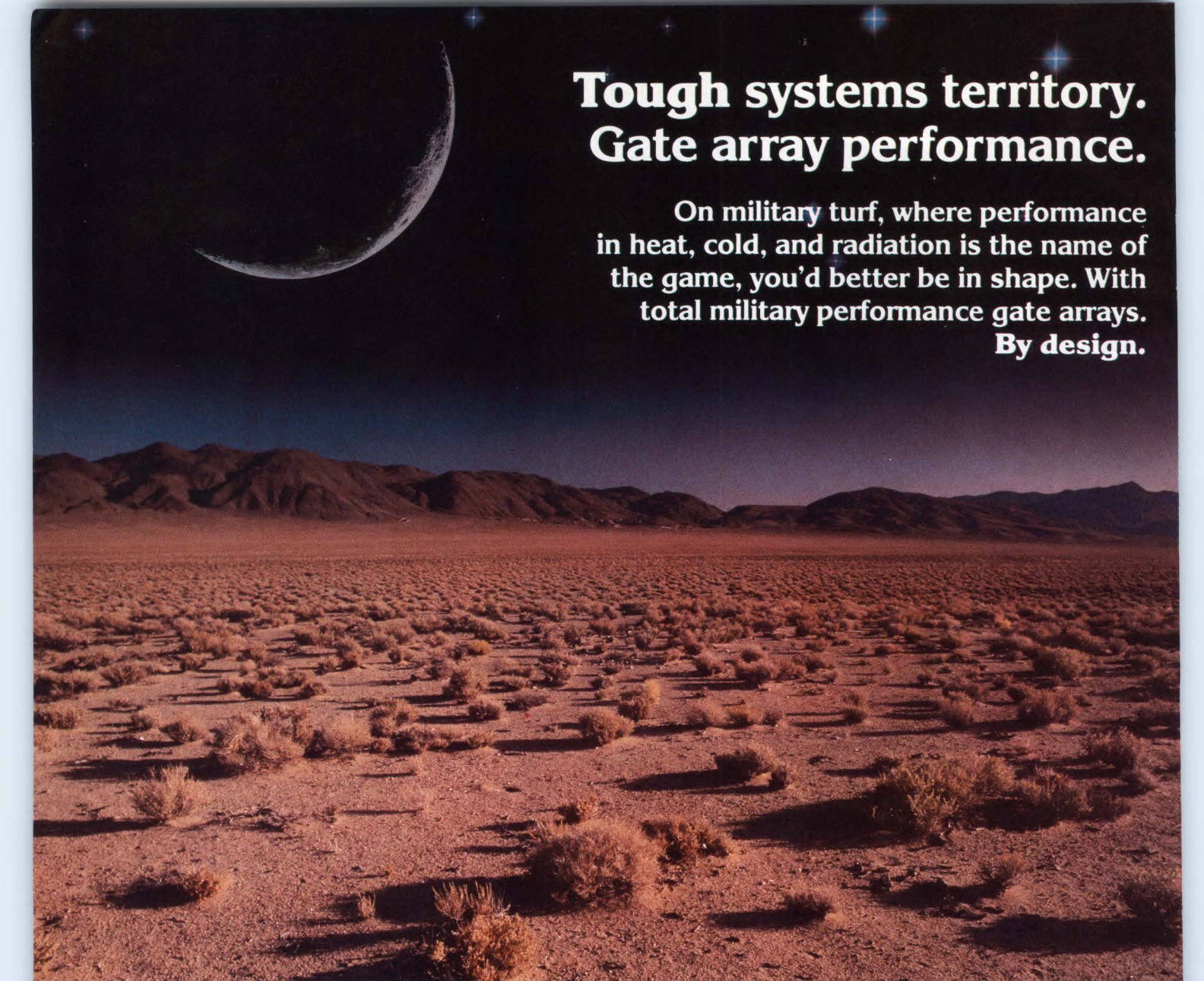
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Thin-film read head aims directly at servo tracking

For the first time, a thin-film head has been designed specifically for reading the servo-tracking information on a hard disk. Moreover, the head coil puts out a minimum voltage of $400\text{ }\mu\text{V}$, a full $100\text{ }\mu\text{V}$ more than the minimum specified for thin-film read/write heads. With that voltage output, the head proves valuable for $700\text{-}\mu\text{in.}$ servo tracks that are recorded once and read continually throughout a disk's life, even as the platter's flux strength diminishes.

The head, designed by Read-Rite Corp. (Milpitas, Calif.) for its RR-1212 hard-disk drive, builds a flat coil with 24 center-tapped turns on sliders composed of titanium carbide-treated alumina, which itself is a hard ceramic substance. The head works with an extremely small gap of $30\text{ }\mu\text{in.}$ and a tight low height of $13.5\text{ }\mu\text{in.}$

Standard-cell simulation software runs on personal computer

A software package aimed at developing semicustom ICs based on standard cells is one of the first to run on a personal computer fitted out with a hard-disk drive. It is also one of the first to perform logic simulation from both the circuit schematic and from the final physical layout of the chip.

The package, assembled by Control Data Corp. (Santa Clara, Calif.), consists of some proprietary programs that handle the user interface, extract the simulation net list from the layout, and adapt the standard-cell library to the computer. The cell library, developed by Alphatron, employs $3\text{-}\mu\text{m}$ single-level metal CMOS. Other commercially available software will round out the design package, including Case Technologies' schematic capture program and CAD Group's 12-state logic simulator. The entire collection will run about \$7400, putting it among the least expensive circuit simulation packages.

Interface standard is due for Unix application programs

The overwhelming popularity of Unix has fostered a broad assortment of application programs that are not necessarily compatible with one another.

Recognizing the potential problems, AT&T Technologies Inc. (Greensboro, N.C.) has produced a standard that defines the soft-code interface and run-time behavior of applications running under Unix System V. The initial document, scheduled to be distributed some time next year, will define the minimum set of system calls (commands to the operating system) and library functions common to all application programs running under the operating system. Eventually extensions will be added, dealing with kernels to data-base management. The interface definition follows initial work of the /usr/group standards committee.

Computer building blocks eliminate wiring concerns

A complete computer system can be assembled by stacking Lego-like modular components, thus eliminating the need for backplanes, wiring harnesses, and cabinets. The MA2000 MACROcomponents from National Semiconductor Corp.

NEWSPULSE

(Santa Clara, Calif.) represent a new direction for stand-alone computer systems. Users need not bother with engineering concerns; instead they can easily and efficiently tailor the systems to their needs. Built around a base power supply and an 8-bit CMOS microcontroller (NSC800), a full system can be created by stacking combinations of modules, which include RAM, ROM, digital-to-analog and analog-to-digital converters, and digital interfaces. The entire system is geared for real-time applications; as such, MVP-Forth is available as a ROM module. Among the future elements will be an interface for a terminal, a floppy-disk controller, and a printer.

SMD interface extension transfers data at 2.16 Mbytes/s

An extension to the Storage Module Device (SMD) interface boosts the parallel data-transfer rate between a host and a high-performance Winchester disk drive to 2.46 Mbytes/s over 50 ft of cable—up from the SMD's current 1.92-Mbyte ceiling. Devised by Fujitsu America Inc. (San Jose, Calif.), the extension is not intended to compete with the Intelligent Peripheral Interface, which transfers information at 10 Mbytes/s and is meant for SMD-type drives. Rather, the SMD extension will serve as an interim solution until IPI controllers are readily available.

The company created the extension for an updated version of its popular Eagle disk drive. The high-speed SMD interface works with a 3-MHz clock, which is double the clock speed of the current SMD interface. Besides increasing the transfer rate, the faster clock delivers a 100% increase in the drive's track capacity,—to 40,960 bytes a track.

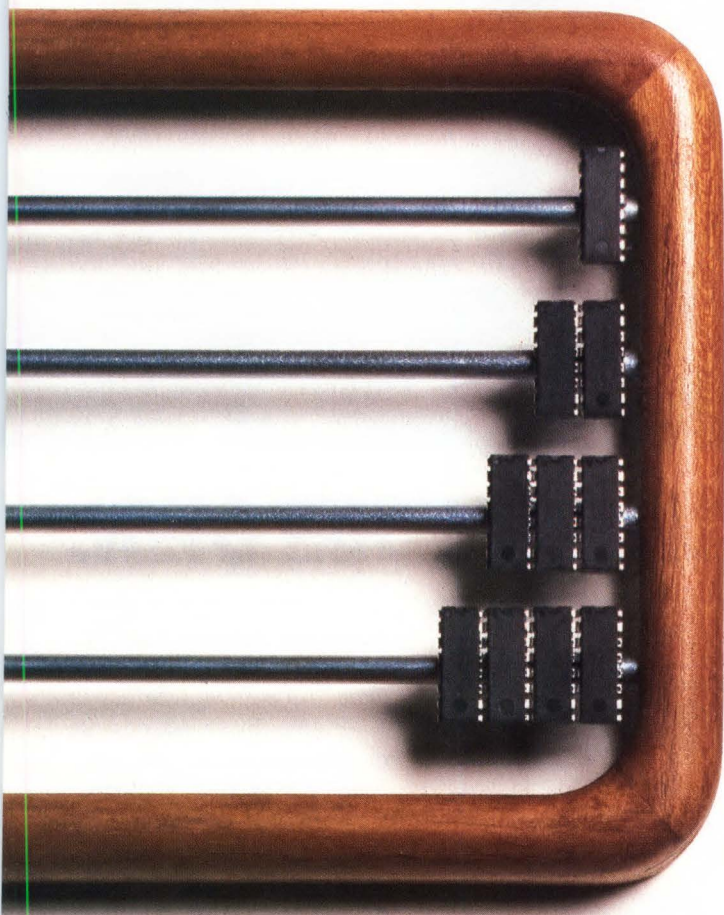
Power MOS driver replaces Darlington pair

A power MOSFET with drain-to-source diode protection and an output drive of up to 100 mA has been squeezed into a low-cost TO-92 can. Its creators at Siliconix Inc. (Santa Clara, Calif.) have christened the part "fetlington," because it does the job of a bipolar Darlington pair. It may be used as a lamp or relay driver, an analog signal switch, or a general-purpose buffer, in which case it switches up to 60 V. The part should go for around 10¢ in large quantities.

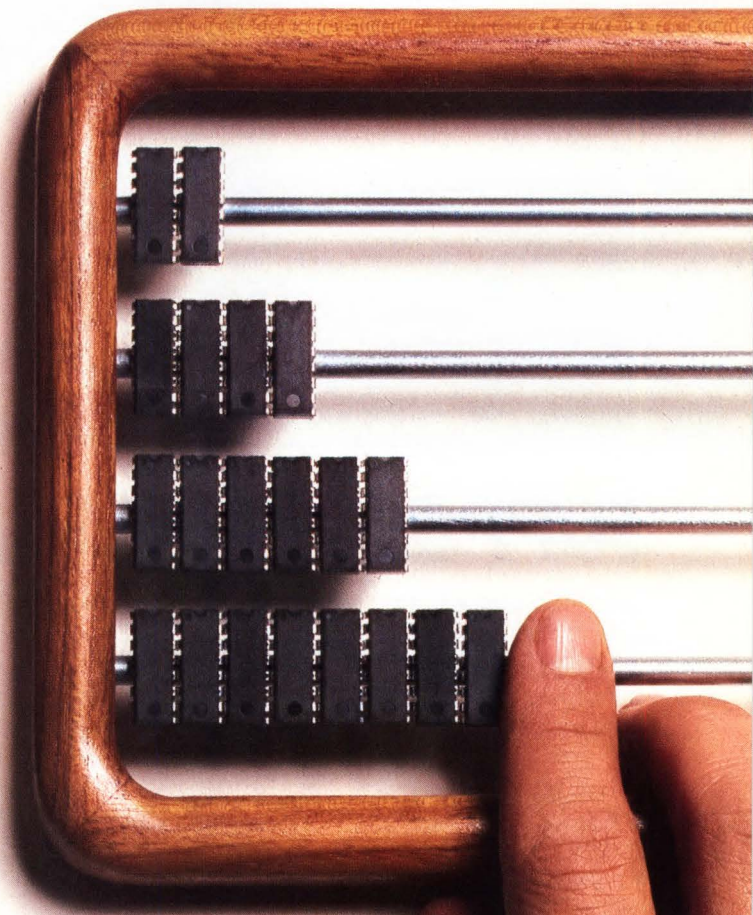
England initiates first ISDN signaling standard

Great Britain has taken a big first step toward worldwide telecommunications with a signaling standard geared for tying the next generation of PBXs to the up-and-coming Integrated Digital Services Network (ISDN). The digital access signaling standard, finalized by British Telecom, specifies an HDLC-type transfer mechanism that ensures error-free transmission of messages and proper sequencing. It enables extensions of ISDN PBXs to act essentially as workstations, communicating over Britain's System X telephone exchange, which integrates speech with data, text, facsimiles, and graphics. The signaling standard is compatible with the International Standards Organization's seven-layer Open Systems Interconnection network model.

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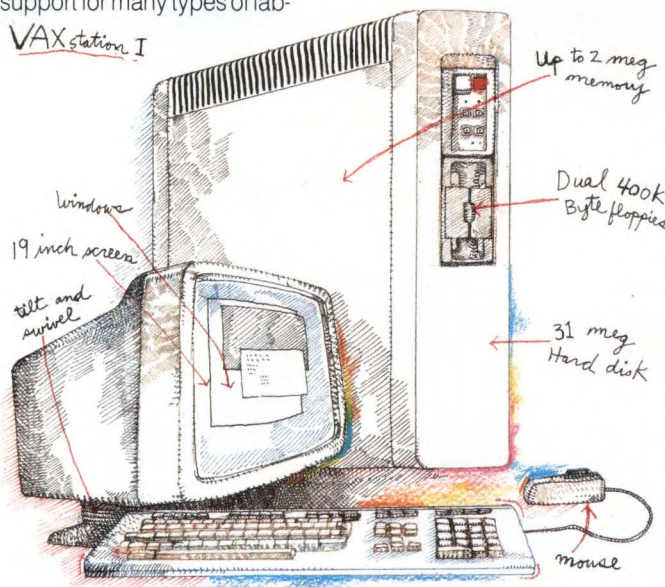
You can do a lot more with a lot less effort when you have a comfortable working environ-

ment. That's why the VAXstation I workstation comes with such an impressive list of ergonomic features.

The monitor, for instance, not only tilts, swivels and minimizes glare – it gives you a large working area with its 19-inch bit-mapped black and white display. What's more, it provides exceptional image clarity with its 960 by 864 pixel resolution. The refresh rate is 60 hertz and the display is non-interlaced, so it's virtually flicker free.

Windowing software lets you view and control multiple processes at the same time. You can overlay windows and move between them easily. You can even create highly integrated applications that dedicate multiple windows to a single process, and scale windows up or down in size.

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the VAXstation I workstation supports a "mouse" pointing device.

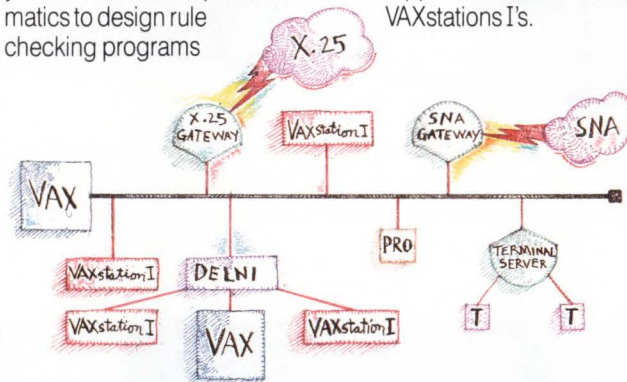
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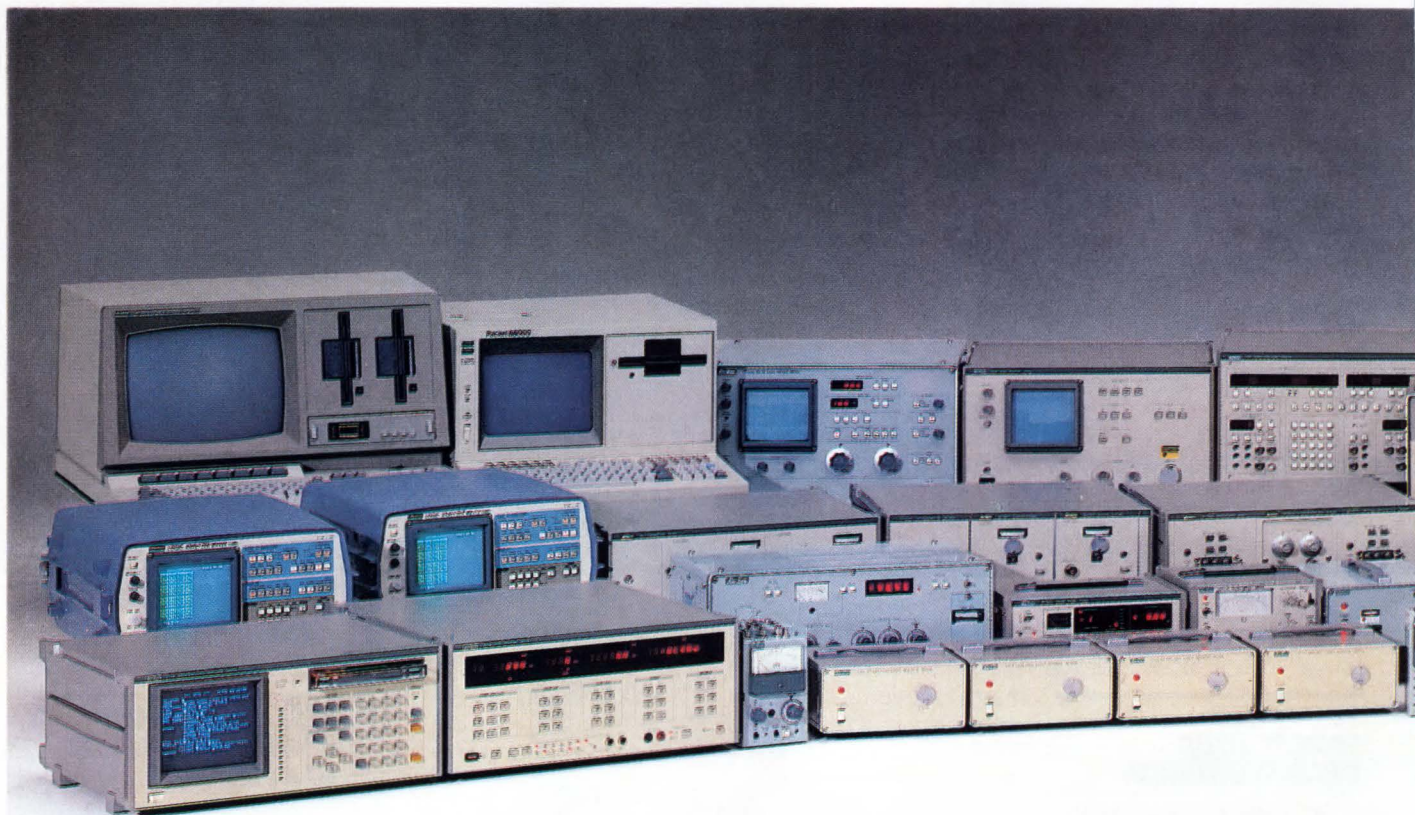
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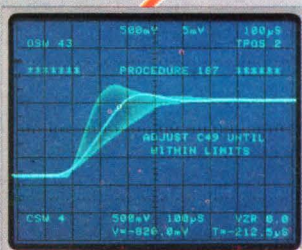
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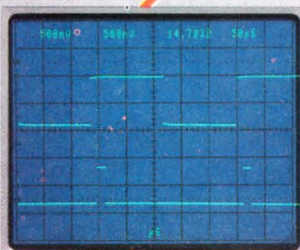
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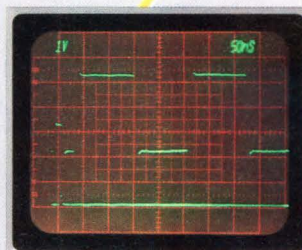
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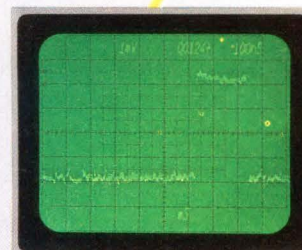
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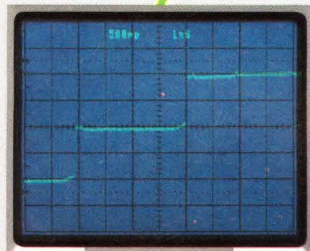
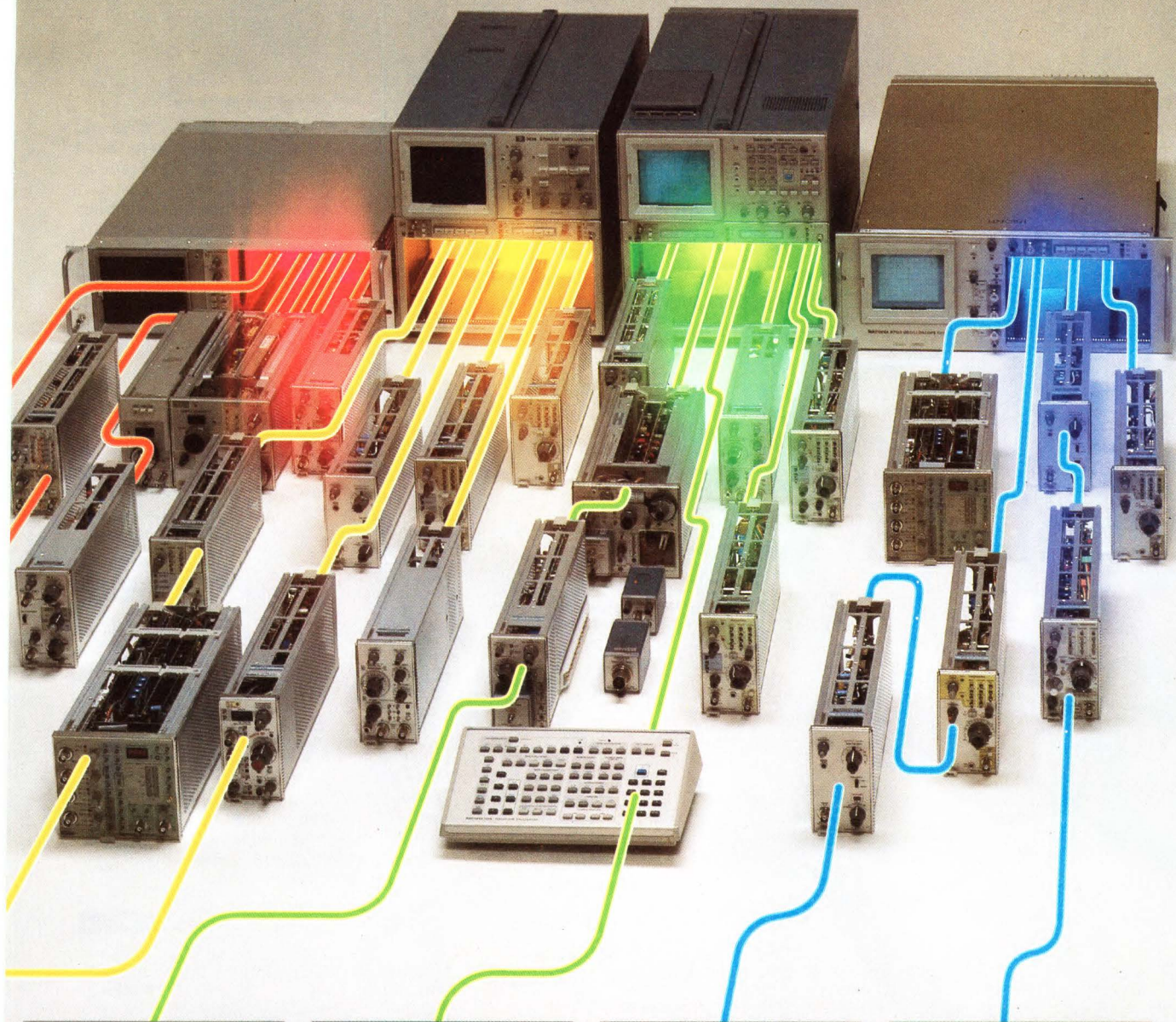


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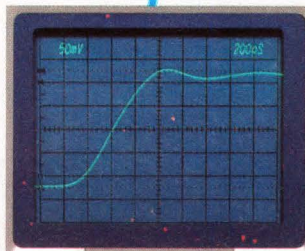
THE ANSWER
BY ANY MEASURE



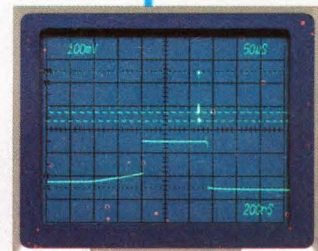
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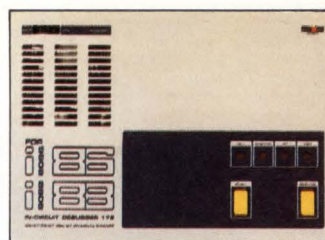
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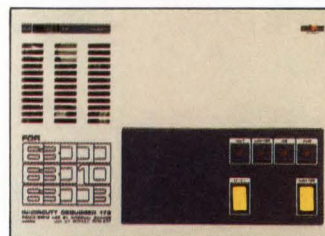
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i8086/88

i8086
i8087
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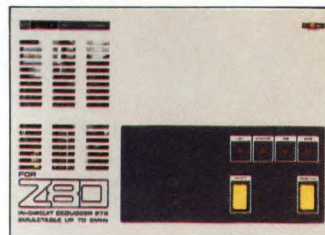
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68000

68000
68010
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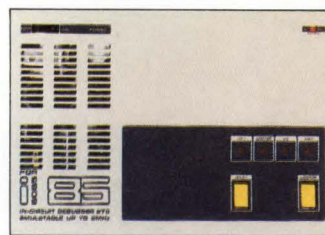
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Z80

Z80
Z80B
Z80H

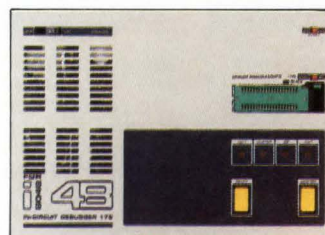
Emulates Z80B microprocessors to 6 MHz and Z80H to 8 MHz. Features; 64K byte user emulation memory, 2K deep x 32 bits wide realtime trace buffer, 29 different debugger commands.



i8085

i8085A
i8085A-1
i8085A-2

Emulates 8085 processors up to 6 MHz. Features; 64K byte user emulation memory, 2K deep x 32 bits wide realtime trace buffer, 29 different debugger commands.



i8048

i8048
i8049
i8050
i8748
i8749
i8039
i8035
i8040

Emulates entire 8048 family in one unit to 11 MHz. Features; 4K emulation memory, 2K deep x 32 bits wide realtime trace buffer, 29 different debugger commands. 8748 and 8749 units feature a built-in EPROM programmer.

NEWSFRONT

Floppy-disk drive stores an unparalleled 6.6 Mbytes and records 384 tpi

A pair of stepper motors handle the coarse and the fine head adjustments for a record-breaking 5¼-in. floppy disk.

A 5¼-in. floppy-disk drive now in the final stages of development will deliver 6.6 Mbytes of unformatted storage, twice that of its nearest competitor. But that is not the only record it shatters. Its two stepper motors—one for coarse and the other for fine adjustments—enable the drive to lay down 384 tpi, doubling the 192 tpi that previously passed as top of the line performance.

Both the current and former record holders are built by Drivetec Inc. (San Jose, Calif.). The track width of the latest drive is roughly 3 mils, compared with the approximately 4.7 mils of its predecessor.

Each drive uses its pair of stepper motors to turn individual lead screws: The coarse motor controls the head carriage directly, and the fine motor—with a 5:1 mechanical advantage—moves the primary lead-screw assembly (Fig. 1).

The tighter track densities and narrower track widths of today's drive are the result of

doubling the number of threads on the prototype's main lead screw. Thus the screw must be very precisely machined.

Working together

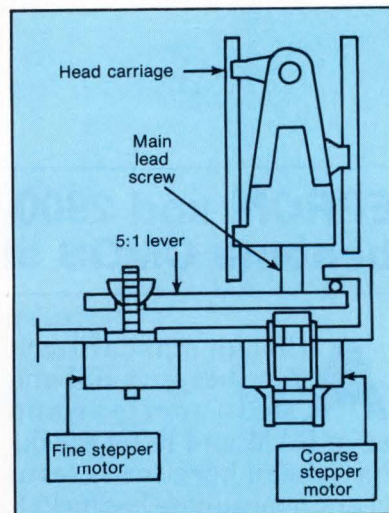
The drive is expected to have a packing density of 10,000 bpi, which is the equivalent of 9908 MFM-encoded flux changes/in. It will transfer data to its controller at 500 kbits/s. That rate makes the unit theoretically compatible with older 8-in. floppy controllers (using the SA400 interface), as well as with the 1.6-Mbyte 5¼-in. floppies now coming on stream. The high density does, however, restrict the drive to 600-Oe floppy disks in place of the 300-Oe coatings used on most lower-density dishes. This is necessary to avoid the possibility of "fringing" (overlapping and difficult to read bit domains) resulting from the tightly packed tracks. While these are currently in relatively short supply, the company expects them to be available as the demand emerges.

Alternatively, a bit density of 20,000 bpi or more could have been chosen by going with a faster data-transfer rate. That, of course, would have made the drive incompatible with existing floppy-disk drive controllers.

As mentioned, both units rely on two stepper motors. The first shifts the head from track to track, and the second fine-tunes the movement, keeping the head to within 100 μ in. of the center of a track (Fig. 2).

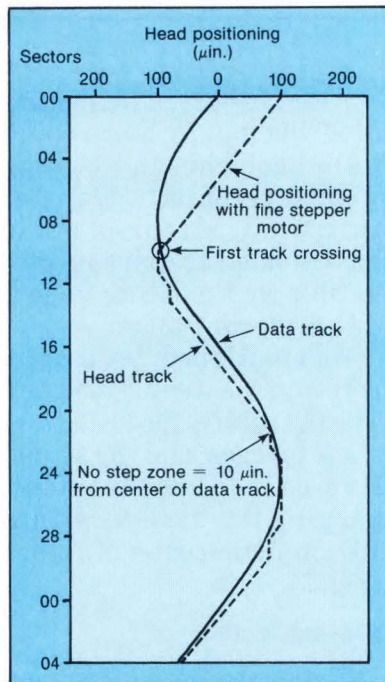
Staying in line

The correcting action taken by the fine stepper motor is in response to servo-tracking information that appears as two 5-byte, 80- μ s servo bursts within each sector of the



1. The 6.6-Mbyte floppy-disk drive being developed by Drivetec will work with two stepper motors. One will handle coarse adjustments, moving the head from track to track. The other will fine-tune the positioning to keep the head to within 100 μ in. of its specified location.

NEWSFRONT



2. The embedded servo mechanism controls the head position to within $\pm 100 \mu\text{in.}$ of the center of the data track. Each track will be approximately 3 mils wide.

track. An amplifier at the front end of the servo mechanism gauges the tracking accuracy according to the relative amplitudes of the signal bursts. If the amplitude ratio is greater than one, the head is off track in one direction; if it is less than one, the head is off the track in the opposite direction.

A capacitor-charging mechanism records the bursts that are read from the disk and performs a sample-and-hold function for the servo. In the meantime, two comparators examine the charging level. If they detect that the head is off course, they trigger the fine-tuning stepper motor. The comparators must make their decision within $25 \mu\text{s}$ so that the motor can move a full $200 \mu\text{in}$ within 3 ms. In addition, the motor can correct a full step within each sector as often as 32 times a track.

Stephan Ohr

EPROM and 2900 bit-slice blocks become CMOS standard cells

Although standard-cell families with SSI and MSI functions and even RAM and ROM blocks have been here for several years, none to date has included a UV EPROM cell and only a few have any cells that approach LSI-levels. Thus this week's introduction of a family of CMOS standard cells represents a sizable step in semicustom technology.

The family, created by

WaferScale Integration Inc. (Fremont, Calif.), is the first to incorporate not only EPROM, but also a set of five building blocks based on the 2900 bit-slice family. These include the bit-slice processor, a carry-look-ahead generator, and a microprogram sequencer.

What's more, even though the cells are fabricated in CMOS, they match the performance of their bipolar

counterparts. A design using the CMOS equivalents of the bipolar chips will yield operating speeds that rival the fastest version of the 2901, the 2901C.

Working conditions

At room temperature and with a 5-V supply and a fan-out of 2, the family's inverter has a delay of just 0.7 ns. A two-input NAND gate exhibits a delay of 0.85 ns, and a signal propagates through a two-input NOR gate in 1.2 ns. For flip-flops, a D-type counter can operate at a maximum clock rate of 125 MHz.

The speed is due to a high-performance $2\text{-}\mu\text{m}$ process that uses n-well CMOS structures built on an epitaxial layer. (Interconnections are accomplished with a single level of metal and one or two polysilicon layers, but late in 1985 the process will go to two levels of metal, further increasing its speed.)

The double-polysilicon CMOS approach is also well suited for analog functions such as switched-capacitor filters, and sometime next year analog standard cells will be added.

A change of plans

Incorporating EPROM required the development of a new memory cell, the details of which the company is not ready to disclose. Its density, however, matches that of a ROM cell, which is not available as part of the library.

Fabricated with a double-polysilicon split-gate structure, the EPROM cell eliminates the need for an

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NEWSFRONT

area-consuming dedicated ground line through the use of a virtual ground line (gated ground). That scheme permits geometries to be relaxed and still achieves a very compact cell. According to the company, the only drawback is the learning curve, since the structure has not seen volume production.

The EPROM can be programmed with just 12.5 V, thereby reducing the circuit stress due to high voltages. Programming time averages about 1 ms per word, and reliability studies thus far show no signs of data loss under severe and accelerated tests involving voltage variations and elevated temperatures.

Well protected

Additionally, the epitaxial layer and I/O protection circuits make the chip highly resistant to latch-up and to electrostatic discharge. In fact, the forcing current for latch-up is well over 100 mA, and circuits can withstand ESD voltages of up to 6000 V.

EPROM blocks can be used instead of ROM blocks, and since the cell uses the same process technology as the other cells in the family, they can be incorporated anywhere on a chip (the programming circuitry of course must be included). However, for now, the EPROM can be implemented only in fixed-size blocks.

In a possible design, a chip 250 mils on a side would require only 20% of its area to accommodate a 64-kbit EPROM block. Just a single

pin need be dedicated to the 12.5-V programming supply. (The company plans to produce the EPROMs as stand-alone chips with a capacity of 64 to 256 kbits in the coming year.)

In addition to the typical SSI and MSI cells, ranging from gates to flip-flops, the library offers five macrocells that are functionally equivalent to the 2901, 2902, 2904, 2909, and 2913 members of the bipolar 2900 bit-slice family. All cells are characterized over the full military temperature range and at 5 V $\pm 10\%$.

Keeping a lid on power

In a typical 16-bit-wide system, power consumption would be roughly 300 mW when operating with an 8-MHz clock. In comparison, the bipolar equivalent would consume about 5 W and require about five times the printed circuit board space.

Other notable functions are full and half adders; an arithmetic and logic unit; programmable shift registers; and user-configurable RAM building blocks (built from six-transistor cells), including a dual-port cell structure. Compilation routines for both the RAM and EPROM cells are being created.

Software for the family will consist of cell library overlays for workstations like those from Daisy, Mentor, and Valid and a package that can run on a VAX. Simulation software will also be available for the workstations; the VAX package will offer a more detailed simulator and a

program that can compare simulators run on the VAX and a workstation.

Dave Bursky

Selective plating strengthens bonds, raises lead density

As IC lead counts increase beyond 100 contacts, laboratory designers are looking for techniques to mount chips directly to pc boards. In doing so, they can eliminate the bulky packages of pin-grid arrays, chip carriers, DIPs, and so forth. Tape-automated bonding (TAB), using selective plating, is emerging as one of the most viable methods.

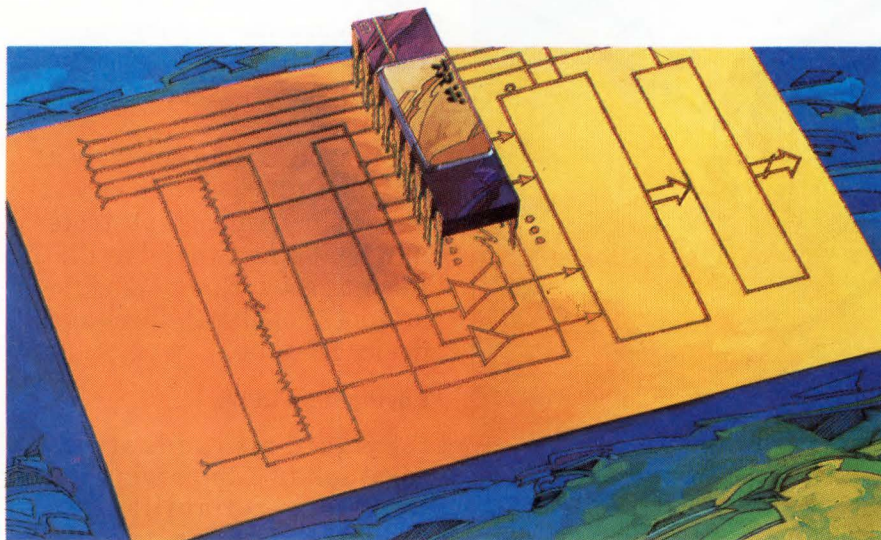
Until now, soldering the leads of TAB chips to circuit boards posed a problem. In the past, the chip's copper leads were gold-plated, so that the IC could be bonded to the board with ultrasonic or thermal compression. However, the gold plating is a contaminant that weakens the solder bond to the copper traces on a pc board. The weaker material, coupled with the short length of the leads (10 to 50 mils), made it difficult to mask around the plated areas.

A simple solution

Now, a selective plating technique from the Interconics unit of BMC Inc. (St. Paul, Minn.) eliminates that problem. The process masks all but the critical area of the TAB leads, the point where

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With the TDC1046, design costs are lowered because sample-and-hold circuitry is not required. All digital inputs and outputs are TTL compatible, and the TDC1046 is simple to interface with low analog input capacitance (30pF). The low, low price of \$29 (U.S. price in 1000s) makes it possible to lower your design costs even further—and without sacrificing performance.

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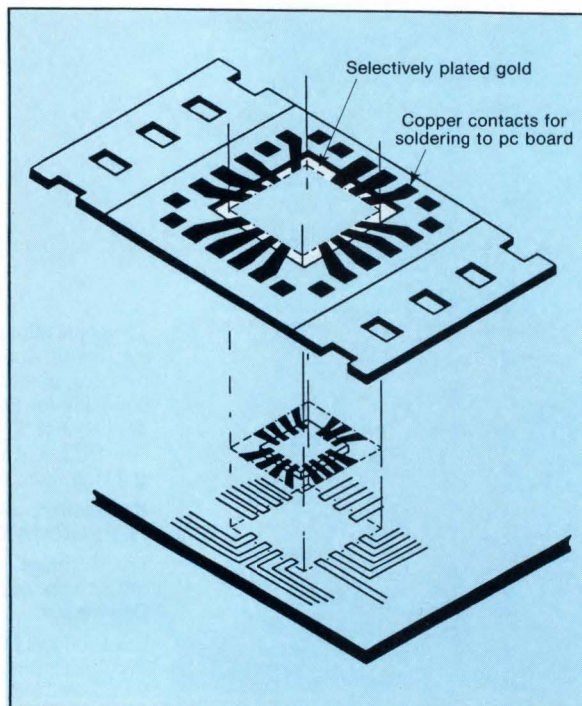
LSI Products Division
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NEWSFRONT

they actually bond to the chip (see the figure). It then plates only that extremely small section, leaving the lead's remaining length bare copper, which can be easily soldered to a circuit board.

In addition to the impressive savings in board or hybrid substrate real estate, tape-automated bonding can also raise the density of chip interconnections. The wire

bonds currently used for high-density connections do not allow the center spacing between pads to go below 5 mils, with 8 mils accepted as the most common dimension. TAB mounting, on the other hand, permits center spacings of 4 mils or less, letting chip designers shrink the area required for bonding pads and thus saving space for active circuitry. *Terry Costlow*



In Interconics's selective plating process, the edges of tape-automated bonding (TAB) contacts are plated with gold, permitting conventional ultrasonic or thermal compression bonding to the die. Meanwhile, the untreated copper ends can be conventionally soldered to a printed circuit board.

Silicone adhesive can be applied without a primer

The first silicone adhesive that can be laid down without a primer coat furnishes a flexible bond that minimizes the chances of cracking when thermally mismatched materials are joined together. By doing away with the primer, the Sylgard 577 adhesive, from Dow Corning Corp. (Midland, Mich.), can be put to work in hybrid circuits and packages like pin-grid arrays. Until now, such applications generally used epoxy to bond aluminum heat sinks to substrates. Further, eliminating with the primer slashes labor and process time.

Silicone, unlike epoxy, is a flexible adhesive that serves as a cushion when a substrate and heat sink expand at different rates. Epoxy is rigid and does not absorb shock as a device heats up.

Laying it on thick

Sylgard also adds structural solidity, improving the long-term reliability of a package. It has a tensile strength of 800 lb./in.², far greater than other silicone adhesives. Although this figure is lower than that of most common epoxies and of some other adhesives, the material can be applied more thickly, hence making for a stronger bond. The material is cured at high temperatures, so the curing cycle is not much different than that of other ad-

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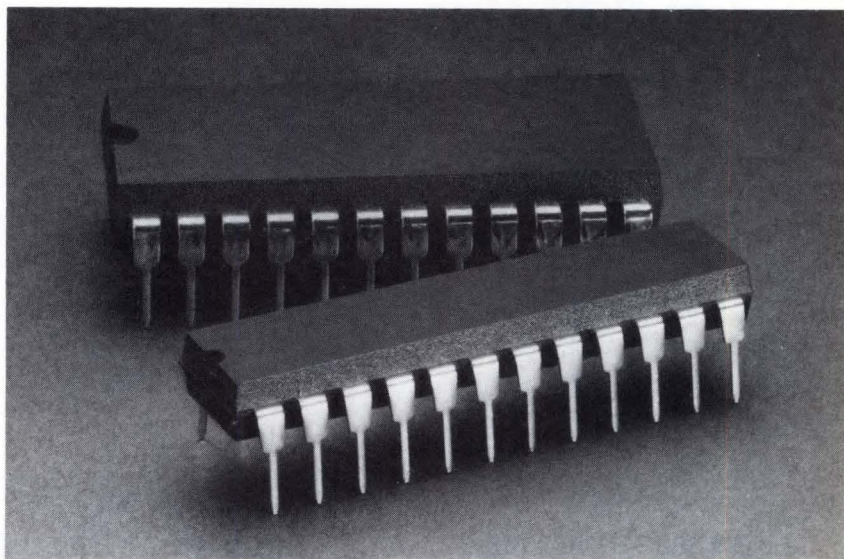
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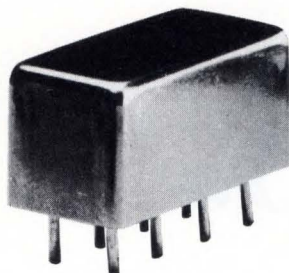
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CONTROL	DC-0.05		
INSERTION LOSS, dB			
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total range	1.4	2.0	
	1.6	2.5	
ISOLATION, dB			
1-10 MHz IN-OUT	TYP.	MIN.	
IN-CON	65	50	
	35	25	
10-100 MHz IN-OUT	45	35	
IN-CON	25	15	
100-200 MHz IN-OUT	35	25	
IN-CON	20	10	
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The adhesive contains no solvents or conductive materials, and is thus clean enough for a range of uses. Other silicones not only require primer coats, but they also release contaminants that can cause corrosion.

The primerless silicone is also used in a potting material, called Sylgard 567. This compound, used in high-voltage power supplies, transformers, coils, and other large packages, cuts time and labor costs by 10% to 15%. What's more, the absence of any solvents eliminates the formation of bubbles during curing, a frequent cause of electrical breakdown in other potting materials.

Terry Costlow

80-MHz chip set comes on the heels of IPI announcement

The first chip pair dedicated to the newly announced Intelligent Peripheral Interface (IPI) level

2 will transfer data between a host computer and its peripherals at up to 80 MHz. Produced jointly by Emulex Corp. (Costa Mesa, Calif.) and Simulex Corp. (Tustin, Calif.), the two chip set comprises a drive interface and another chip that serializes and deserializes data and formats control bytes on the IPI bus. Both are managed by an 8051 microcontroller. The interface executes the IPI data-transfer sequences.

The IPI level 2, a development of the X3T9.3 American National Standards Committee, will replace the SMD interface currently used in high-performance minicomputers and mainframes (ELECTRONIC DESIGN, Oct. 31, p. 45). In addition to transferring data faster, it will be able to drive longer cables. The SMD makes possible a 24-MHz transfer over 50 ft of cable; the IPI works at frequencies up to 80 MHz over as much as 400 ft of cable.

The new chips, which are to be fabricated in CMOS, should be released sometime next year.

Stephan Ohr

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XASM51	8051	200.00	250.00
XASM65	6502/65C02	200.00	250.00
XASM68	6800/01, 6301	200.00	250.00
XASM75	NEC 7500	500.00	500.00
XASM85	8085	250.00	250.00
XASM400	COP400	300.00	300.00
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EPROM: 2758, 2716, 2732, 2732A, 2764, 2764A, 27128, 27128A, 27256, 2508, 2516, 2532, 2564, 68764, 68766, 5133, 5143. **CMOS:** 27C16, 27C32, 27C64, MC6716. **EEPROM:** 5213, X2816A, 48016, I2816A, 5213H. **MPU (w/adaptor):** 8748, 8748H, 8749, 8749H, 8741, 8742, 8751, 8755.

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	150	240	IMS2630-15
16Kx4	100	160	IMS2620-10
	120	190	IMS2620-12
	150	240	IMS2620-15
64Kx1	100	160	IMS2600-10
	120	190	IMS2600-12
	150	230	IMS2600-15

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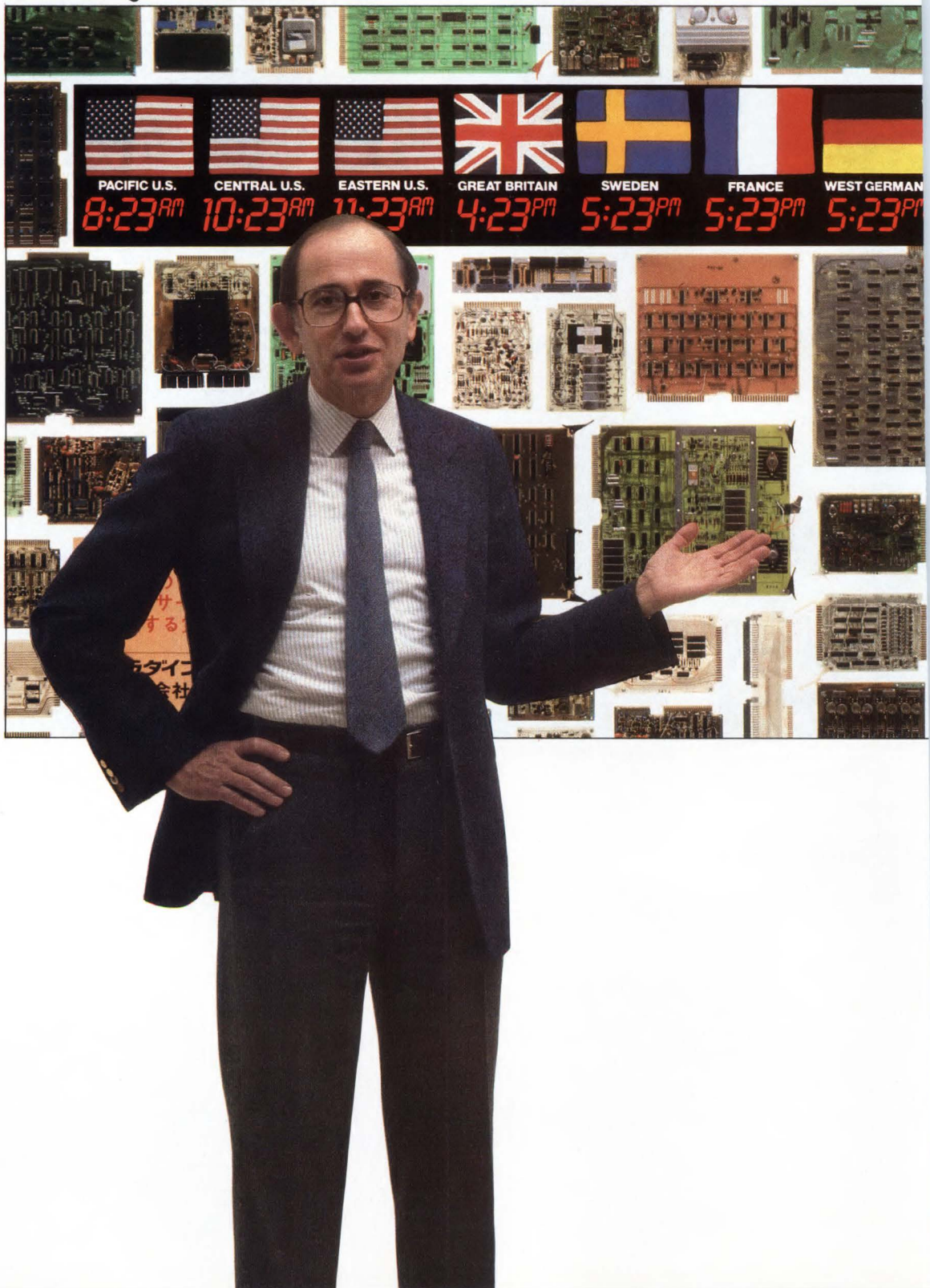
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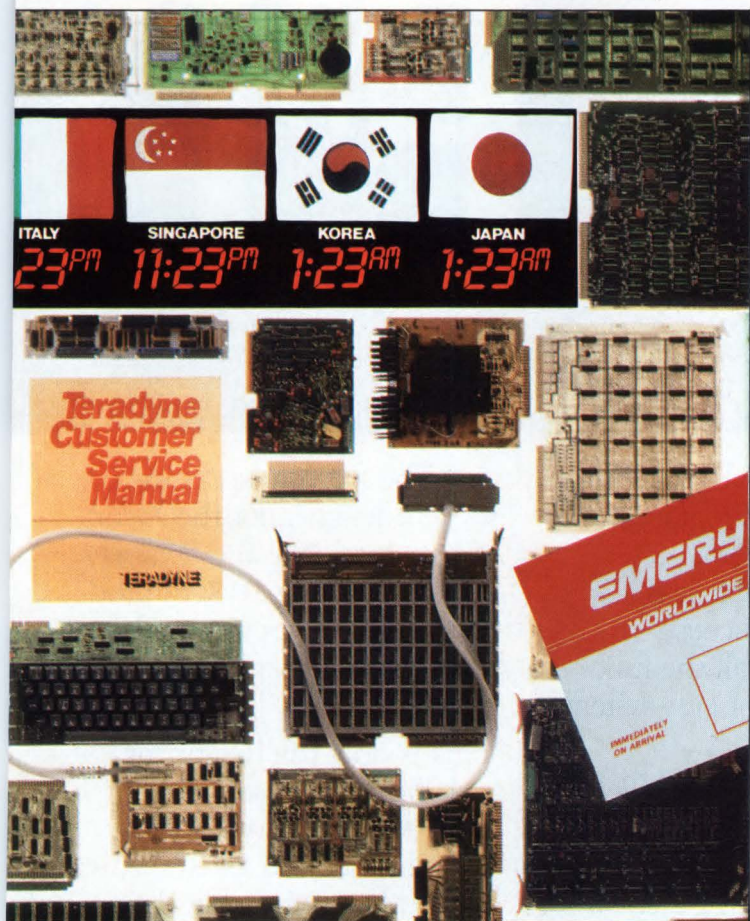
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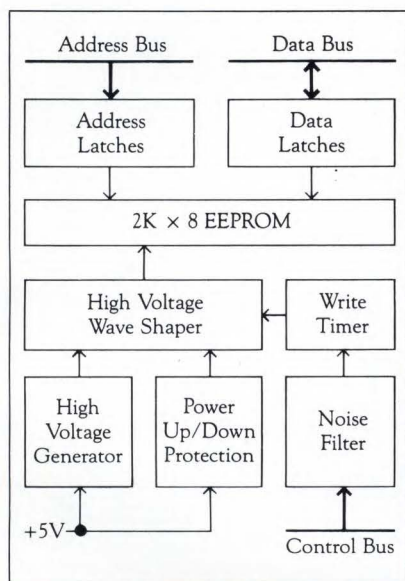
And the erase/write cycle is completed within 10 ms, during which the system buses are free for other tasks.

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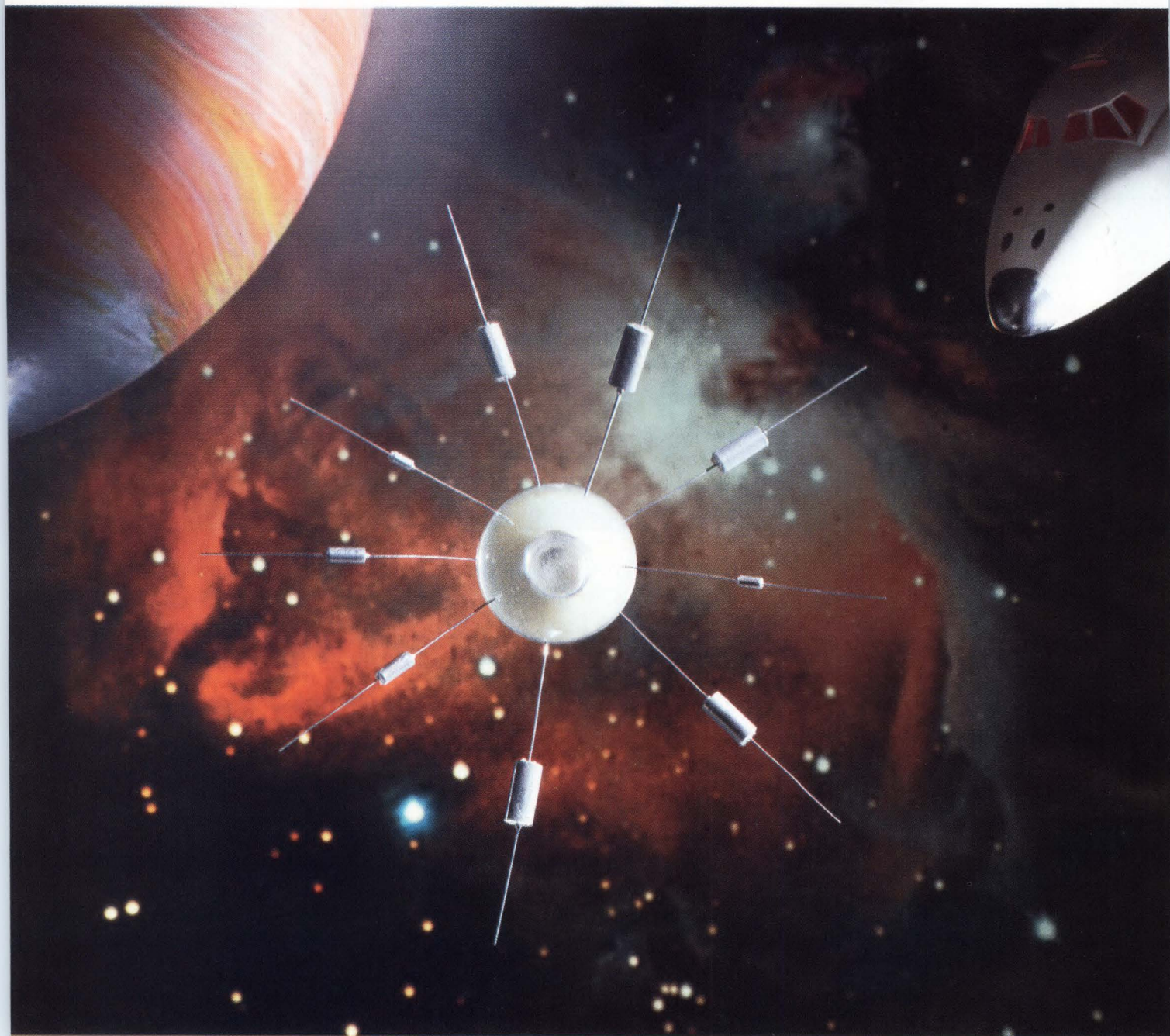
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CIRCLE 35

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VIEWPOINT

Despite stiff competition from other technologies, bipolar will keep growing

Robert A. Stehlin

Senior Member, Technical Staff
Design Manager
Bipolar Logic and Memory
Texas Instruments Inc.
Dallas, Texas

Bipolar is far from dead," insists Robert Stehlin, who bristles when he hears how everything will be built with CMOS. "Some functions will always be better served by bipolar, others by CMOS."

"For instance, bipolar processing is a wiser choice for 'small logic' and TTL equivalents than is the high-performance CMOS now in favor. Similarly, CMOS proves more appropriate for LSI and VLSI circuits."

In memories, too, bipolar and CMOS will carve out their own niche: The former will be applied to fast caches and FIFOs, the latter to dynamic and static memories.

Sadly, Stehlin explains, the industry tends to forget that bipolar technology has not stood still over the past few years. The novel structures, new processes, and high-resolution photolithography that give added speed and

density to MOS devices often prove equally valuable for bipolar circuits, and they will continue to push them to new highs in the future.

As examples of MOS-borrowed techniques, he cites the emergence of oxide isolation in low-power Schottky. In addition, ion implantation in lieu of the customary diffusion has produced bipolar devices with shallower junctions, greater control, and

ultimately better performance. Of course, photolithography is managing to scale down bipolar devices, holding out the promise of greater density.

Together those MOS-based techniques have already slashed power dissipation so low that it is no longer a concern for bipolar ICs. "With such momentum," Stehlin assures, "the technology can only get better."

Density gains have been impressive. "Back in 1980," Stehlin recalls, "the smallest transistor took up 4 mils² from the middle of the isolation region. Today we need only 1 mil². By 1988 bipolar density will be four to five times greater than is possible today."

No doubt, the speed of bipolar circuits has something to gain from new processes. Today's 8-bit-slice processors have internal gate delays of 1 to 1.2 ns compared with TTL's 3 ns of a few years ago. "For the future, we have only to look at the research labs," Stehlin advises. "Work in I²L is producing internal gate delays of 200 ps. In addition, Japanese companies are talking about isolation techniques that could tighten spacing



Since 1965 Robert Stehlin has been designing circuits with bipolar, MOS, and CMOS, and developing processes for them, giving him an excellent background in all three. He holds a dozen patents, all related to circuit design or processes. He earned an MSEE and a post-master's degree in electrical engineering, both from Southern Methodist University.

Heather Bryce

and lower collector-to-base capacitances. Reportedly Hitachi has built ECL circuits with gate delays as short as 84 ps." Though those figures may seem inconceivable in light of today's bipolar speeds, Stehlin feels confident that they will characterize the bipolar circuits of the future.

As it is with CMOS, gallium arsenide will probably be a chief competitor of bipolar technology. Today the real debate is whether silicon—bipolar or CMOS—can reach

the GaAs level. Already, Stehlin points out, the speed difference between GaAs and laboratory silicon has dropped to less than two to one. "Though gallium arsenide's features are indeed attractive," he admits, "from a pure speed standpoint it is not attractive as it once was."

"Furthermore, the rule of thumb dictates that at least half the internal delay be attributed to the interconnections. With greater degrees of integration, that problem will remain the same for both gal-

ium arsenide and silicon. Naturally, I'm talking about conventional interconnections here, not optical laser links.

In an industry that can produce the best on one day and then beat it the next, Stehlin has one big complaint. "People generally compare high-performance CMOS and gallium arsenide with the bipolar of the 1970s. To be realistic—and fair—they really should compare them with the bipolar technology of the mid-1980s. It's getting stronger every day."

Multiple buses form the route to computational flexibility and power

Rattan L. Dhar

CAE Marketing Manager
Masscomp
Westford, Mass.

In designing a computer system for the highest performance, Rattan L. Dhar believes that the most vital factor to consider is flexibility. Technology never stays in one place for long, and a truly performance-oriented system must be designed in such a way that it is "positioned to take advantage of new developments as soon as they happen."

Gary Elinoff



Rattan L. Dhar was previously the director of electronics marketing at Applicon and earlier the vice president of engineering at Adage Inc. He received MSEE from the University of Washington.

For workstations and supermicrocomputers, the key to that flexibility is multiple buses. According to Dhar, it is the actual computational elements—CPUs, array processors, floating-point processors, and the like—that are now undergoing the most rapid evolution. Manufacturers must link these vital components via special-purpose, proprietary buses, not only so that they can communicate as efficiently as possible, but also because such an approach allows the fastest engineering response time possible to changes in these dynamic system elements.

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VIEWPOINT

such as printers and mass-storage devices, change is slower and more predictable. For these more sedate subsystems, often characterized by moving mechanical parts, standard buses, such as Multibus or the STD+ bus, are more suitable.

Workstations and supercomputers, he continues, will continue to divide into two basic types: those with limited computational power and those with more powerful number-crunching capability.

"In 10 years," he explains, "every scientist and engineer will have some form of computational power at his desk. However, it is not necessary

for each of them to have the very best that money can buy. For some, machines that employ only one system bus will suffice."

For these machines, cost-effectiveness will be more important than high performance. Dhar emphasizes that "there will be a place for them, as long as they can communicate, via networks, with the more powerful number crunchers." That, of course, requires software that enables the various workstations and computers to communicate effectively with each other.

As for CAE software, Dhar believes that more and more semiconductors will be de-

signed using standard-cell libraries.

Each manufacturer maintains his own library on his own CAE system. It is very difficult to "mix and match," because of the difficulties involved in getting standard cells from divergent sources to "play together" on the chip designer's computational system.

For that reason, Dhar predicts the "emergence of a new industry devoted to maintaining data bases—composite libraries—of standard cells, available to anyone who can pay for them." This industry will benefit from the standard-cell producers, as well as designers. □

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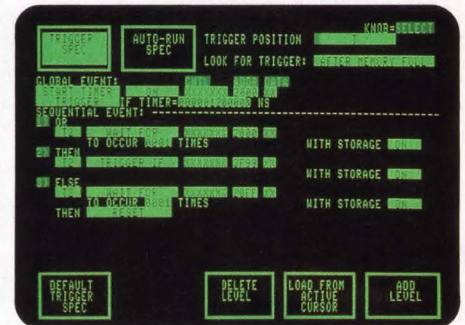
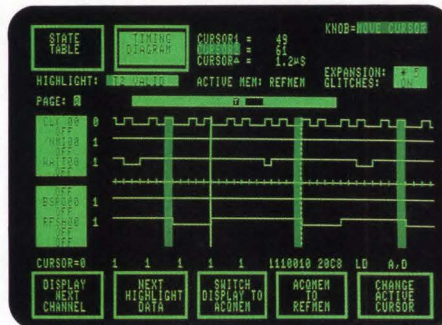
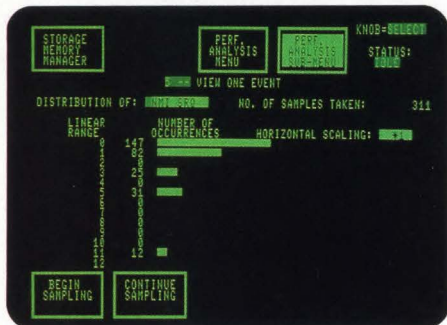
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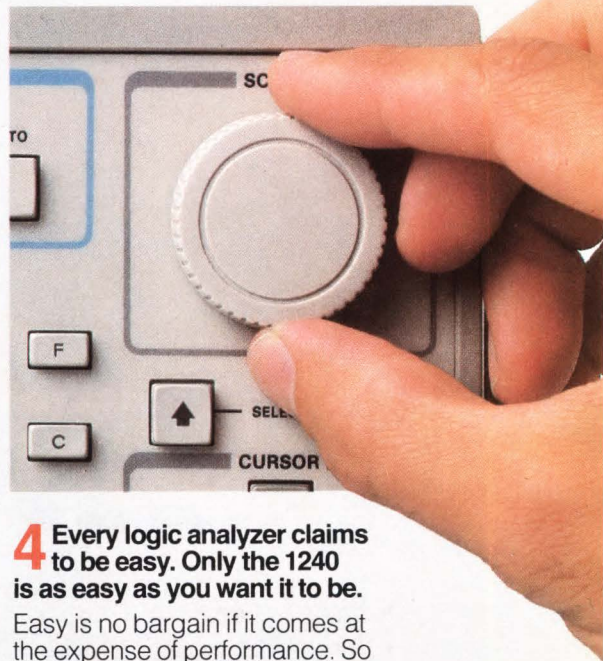
compare and graph the event distributions.

3 Only the Tek 1240 offers so much triggering capability for both hardware and software analysis.

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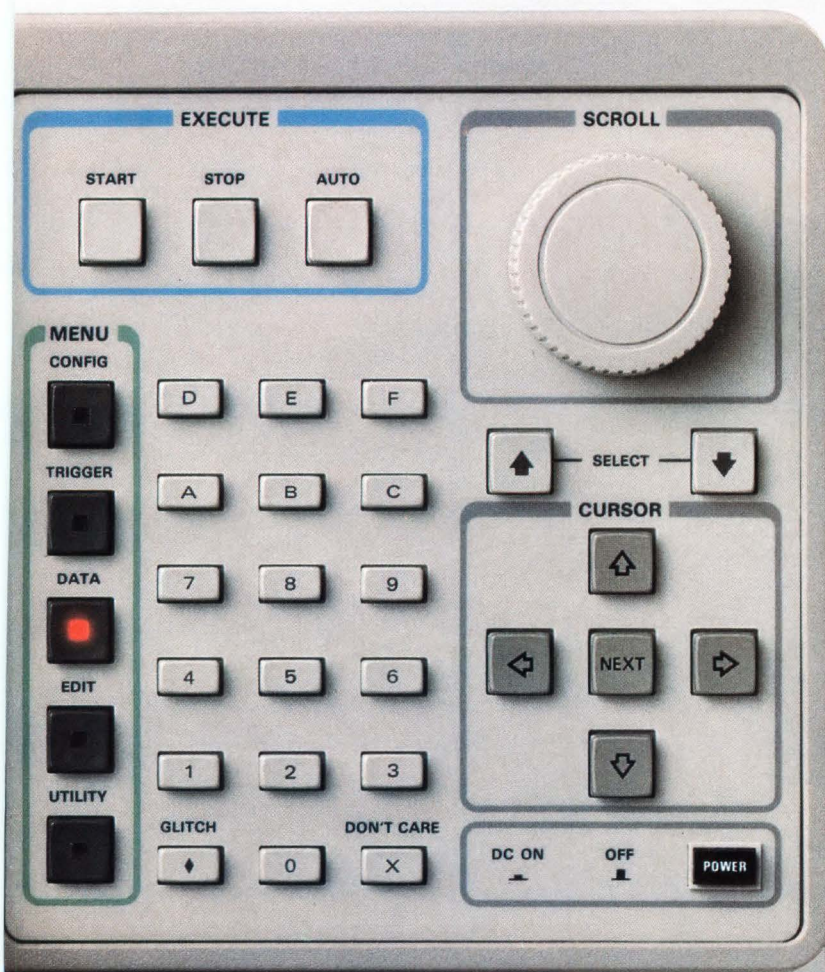


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(Continued next page)



5 No other logic analyzer is as modular, expandable or versatile, to keep your costs low and compromises few.

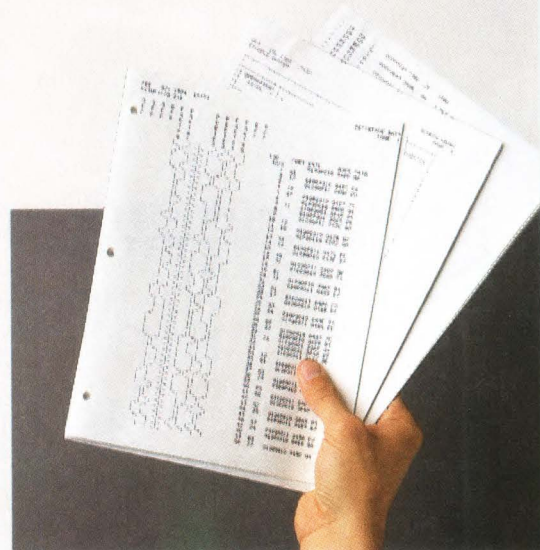
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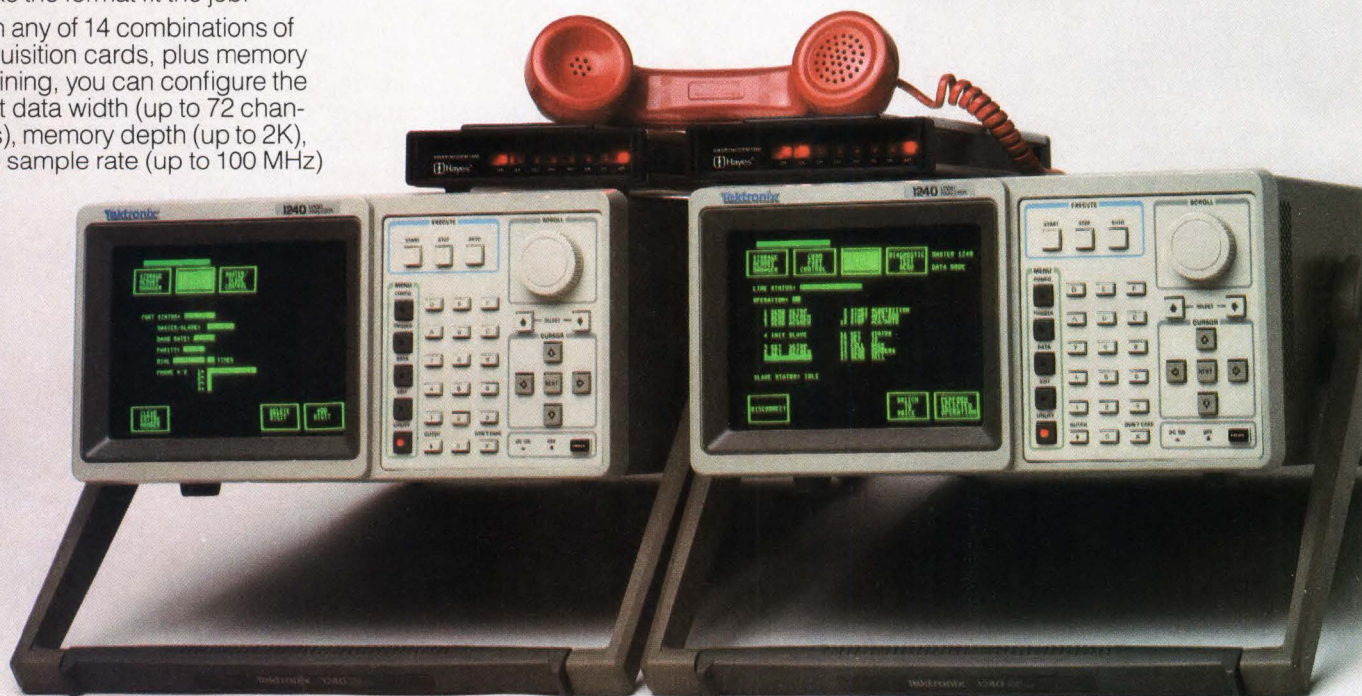
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CONFERENCE PREVIEW

Advances in processing grab most of the attention as IEDM's program unfolds

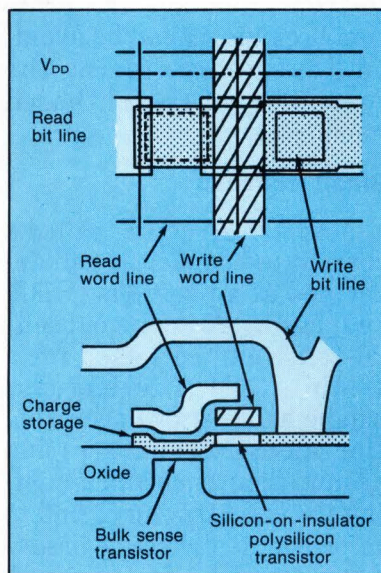
A wealth of new and modified techniques spell a change for memories, semiconductor sensors, bipolar circuits, and high-voltage ICs.

Though the electronics industry continually hears about the digital IC specialist's never-ending quest for smaller transistors and thus faster memories, other frontiers are abuzz with activity. Nowhere do these developments assume greater importance than at the annual International Electron Devices Meeting, held this year in San Francisco, Dec. 10-12.

Not only memories benefit from these new processes, but also semiconductor sensors, power, and voltage-control devices. And, silicon on insulator techniques forecast new levels of performance.

It is almost axiomatic that memories are often the first circuits to reap the benefits of process improvements, because their regular cell structure permits rapid layout and evaluation. Already, researchers have fabricated 1-Mbit RAMs, and many manufacturers have developed some of the concepts necessary to raise densi-

ties to 4 and even 16 Mbits. An experimental silicon-on-insulator cell structure, for instance, is suitable for 1-Mbit and larger dynamic memories. The cell, developed by Texas Instruments Inc. (Dallas), employs a polysilicon



1. Putting the pass gate control transistor in the polysilicon layer above the storage cell, Texas Instruments has developed a dynamic RAM cell that could lead to 1-Mbit-or larger-memories.

transistor fabricated in the layer above the substrate as a pass gate to control the potential of an EPROM-like storage node (Fig. 1).

Thus far, only small arrays of cells have been implemented. But results indicate that the structure would be practical at 1 Mbit and beyond. The company's first commercial 1-Mbit chips, expected in 1986, will be built with a more conventional cell.

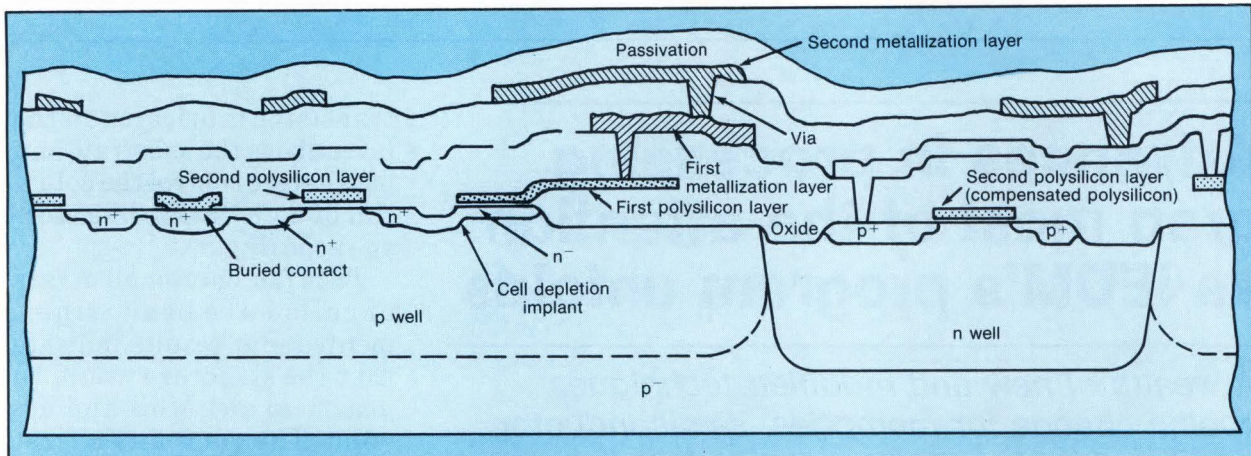
Another experimental dynamic RAM, in CMOS, combines two levels of metal interconnections and 1.2- μ m features. It avoids the need for complex silicon-on-insulator or trench structures. The RAM, from Mostek Corp. (Carrollton, Texas), weds two composite levels of metal, a structure that prevents irregularities from forming. Two layers of polysilicon are used as well. (Fig. 2). Between the metal layers, the company works with a proprietary technique to ensure a relatively smooth surface over which the aluminum-copper-silicon layer can be deposited.

Three levels

Features of 1.2 μ m turn up again in a 1-Mbit RAM that goes with two levels of polysilicon and of metal, selective tungsten deposition for contacts, and a buried-oxide isolation process. The memories, from Toshiba Corp. (Kawasaki, Japan), are built on a p-type wafer.

The same-sized features are found on another 1-Mbit

CONFERENCE PREVIEW



2. A combination of two metal layers and two polysilicon layers, along with 1.2- μm features has yielded the first 1-Mbit dynamic RAMs at Mostek Corp.

RAM fabricated on a wafer coated with an epitaxial layer of silicon. Designers at Mitsubishi Electric Corp (Itami, Japan) turned to a titanium silicide gate electrode to cut gate resistance and an aluminum-silicon-titanium metallization scheme to minimize electromigration.

Keeping it smooth

The buried-oxide isolation scheme permits a small, high-capacitance cell (greater than 40 fF) to be fabricated and also yields flat surfaces so that the multiple levels of metal are readily deposited. In contrast, the epitaxial-based design enables the cell's plate-bias voltage to be considerably reduced, thus reducing the electric field stress to the gate dielectric. That, in turn, permits the use of a thinner dielectric, and hence a higher-capacitance cell.

Trench capacitor structures, which save lateral chip area, are a growing research trend. Although no commercial dynamic RAMs have been made with the technology, a

number of manufacturers feel it is the only road to achieving densities of 4 Mbits and more. At TI, for example, modeling of the trench structure has indicated that for a trench spacing of 0.75 μm or more, a range of substrate doping concentrations can be established in which trench-to-trench leakage and junction breakdown can be avoided, thus guaranteeing the feasibility of trench-based memories.

Small trenches

A trench structure called a corrugated capacitor cell described at a previous IEDM reduces by 25% the current 20-to 25- μm^2 cell used for a 1-Mbit RAM. The decrease can be had just by optimizing the impurity concentration around the trench and adjusting the cell structure. And to improve the dielectric breakdown strength, Hitachi Ltd. (Kokubunji, Japan) is investigating an edge-rounding technique to eliminate sharp corners and bring the dielectric breakdown up to

19.5 V—very close to the 20.5 V of a planar capacitor.

Now that the concept of trenches has had some time to mature, improved structures such as a folded capacitor cell, an isolation-merged vertical cell, and a buried-isolation capacitor cell have emerged. All promise to help boost chip capacities to the 4-Mbit mark, but it will probably be several years before any of them are used commercially, since they require extremely complex processing steps.

In the folded capacitor cell, from Toshiba, the silicon substrate is first etched, forming the trench, and then a field oxide is created at the bottom of the trench. The side walls of the trench, as well as its flat upper surface after filling then form the capacitor. The capacitance is effectively increased because peripheral length is largest at the edge of the top surface. Additionally, the structure has a high punch-through voltage (more than 10 V) for a cell-to-cell spacing as small as 0.5 μm , making even 16-Mbit memo-

ries feasible.

The isolation-merged structure proposed by Nippon Telegraph and Telephone Public Corp. (Atsugi, Japan) surrounds the single-transistor cell with a vertical capacitor. Each capacitor is isolated from its neighbor by a common cell plate and from the substrate by an insulator formed on the trench surface. The cell delivers a high capacitance (more than 70 fF), a low soft-error rate, no punch-through between adjacent elements, and an improved oxide-dielectric breakdown.

Key to fabricating the cell are several factors: the ability to form an oxide window at the upper part of each cell island's sidewall, thus permitting the n^+ layer to connect to the capacitor electrode (first polysilicon level); the formation of a high-reliability thin oxide on phosphorous-doped silicon is as essential as optimization of the impurity concentration and oxide thickness on the trench surface to prevent parasitic channel formation.

4 Mbits and above

The cell could be a primary factor in memories that come in at more than 4 Mbits. Cell size could be reduced to just $10 \mu\text{m}^2$ with $0.8 \mu\text{m}$ features, and still yield a capacitance of 70 fF with a 20-nm-thick oxide and a $3\text{-}\mu\text{m}$ deep trench. Also aimed at 4 Mbits and beyond is the buried-isolation capacitor cell, developed by NEC Corp. (Sagamihara, Japan). It can result in a cell just $7 \mu\text{m}^2$ when fabricated using submicrometer lithography.

The approach merges the capacitor and isolation regions into a buried capacitor formed within a trench. The sidewall of the trench and the buried polysilicon layer form the two plates of the capacitor, and the boron-implanted p^+ layer at the bottom of the trench isolates the cell from its neighbors.

CCDs: still in the running

Dynamic RAMs, which assign a single transistor to each cell, make the most efficient use of chip area thus lead the density race. Even though most companies abandoned the even more area efficient charge-coupled-device memory as a viable commercial approach, some research continues for specialized applications such as video frame memories.

A novel CCD structure takes advantage of a single level of polysilicon. The simplicity of the CCD, from Philips Research Laboratories (Redhill, England), makes possible exceptionally small cells (2 to $5 \mu\text{m}^2$), built using $0.6\text{-}\mu\text{m}$ gate lengths and $0.4\text{-}\mu\text{m}$ spaces between gates.

Dynamic RAMs, however, are not the only memories hitting the million device per chip level. For example, an experimental 256 Kbit CMOS static RAM with a four-transistor cell structure employs both n - and p -type polycide gate electrodes. They link the n - and p -type FET drains through buried contacts to keep the cell size small. And dual-depth trench isolation promises reasonable chip sizes for memories of 256

kbits and larger.

From NEC, the RAM cell occupies just $104 \mu\text{m}^2$, which extrapolates to an area for the memory array of just 27.35 mm^2 for 256 kbits. And although the design rules are not submicrometer, they are close— $1.2 \mu\text{m}$ —thus permitting today's lithography equipment to handle the features.

Etching, however, may be an entirely different problem, since $4\text{-}\mu\text{m}$ deep trenches are needed to suppress latch-up and permit p - n junction separations of just $1.3 \mu\text{m}$. Also, shallower trenches ($2 \mu\text{m}$) are used to isolate p - and n -type diffused lines, making possible minimum pitch of $2.1 \mu\text{m}$.

Moving CMOS technology over to EPROM structures requires some extra caution, since the high internal programming voltages can cause circuit latch-up. To overcome that obstacle on both a 512-Kbit and 1-Mbit CMOS EPROM, now in development, designers at Advanced Micro Devices Inc. (Sunnyvale, Calif.) have decided to use double guard rings around the EPROM cells and single guard rings around the high-voltage circuits. Additionally, the circuit will contain special sequencing logic to control the voltages on the gates and the drains of the peripheral transistors during programming.

Megabit EPROMs at hand

Experimental 1-Mbit CMOS EPROMs have been fabricated by working with a deep ion implant in combination with a self-aligned dual-

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gate transistor. Lightly-doped drain transistor structures are employed by Toshiba to make sure that the transistor breakdown voltages remain high. The self-aligned structure could drop programming voltages to about 10 V, while programming times could improve by almost an order of magnitude (from 10 ms a word to just 1 ms).

Taking the single-transistor-to-a-cell approach to EPROM and bringing it over to EEPROMs, Toshiba has created what it calls a Flash EEPROM cell. It is programmed similarly to an

EPROM, using hot carriers in the channel. To erase the charge, it uses a field emission of electrons from a floating gate to an erase gate. Since the cell uses only a single transistor, a 256-kbit EEPROM could be built very close to the size of an equally dense EPROM.

Three polysilicon layers are employed in the Flash EEPROM. The first serves as the erase gate; the second, as the floating gate (as in standard EPROMs); and the third as a word selection line during programming and reading (Fig. 3). When 2- μm design

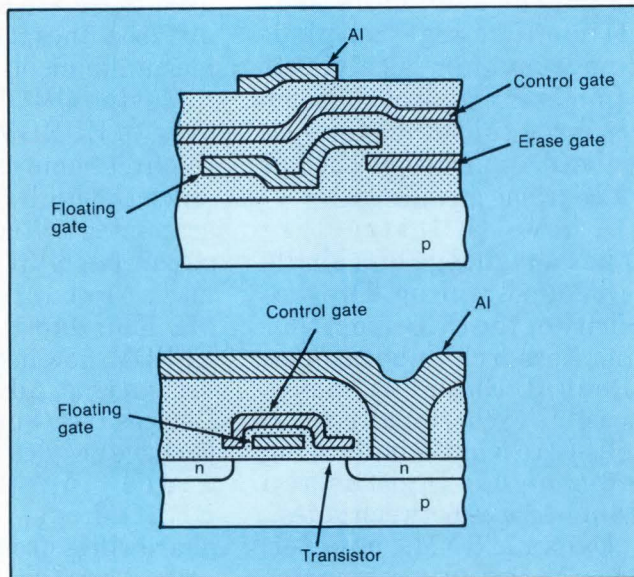
rules are used, a cell area of 8-by-8 μm can be obtained, but the cell can be scaled down to 5.4 by 5.4 μm with 1.2- μm rules.

In small packages

A combination of 1- μm features and step-and-repeat lithography has led to a two-transistor EEPROM cell that is only 7 by 13.5 μm . Designed for high-density EEPROMs, the cell from Intel Corp. (Santa Clara, Calif.) uses an oxide and nitride dual-layer dielectric to obtain the best polysilicon-to-polysilicon insulator capacitance. The tunnel oxide is defined in the drain region of the floating-gate transistor to ensure the best layout, and a special implant, aligned to the first polysilicon layer, results in a higher performance floating-gate transistor and lower process sensitivities.

The move to lower programming voltage has brought about a shielded substrate injector structure. Programmed using Fowler-Nordheim tunneling, the cell, which was devised at RCA Corp.'s Laboratories (Princeton, N.J.), can be written with just 16 V and erased with only 12 V (a 20-ms pulse). The lower voltages are possible because of the structure, which interposes the first polysilicon layer between the substrate and the floating gate, which is itself formed in the second polysilicon layer. The resultant cell has an area of just 135 μm^2 when drawn with 3- μm design rules and just 57 μm^2 when 2- μm rules are chosen.

Dave Bursky



3. Triple layers of polysilicon are used by Toshiba to squeeze an EEPROM cell into 64 μm^2 . Only a single transistor (with two gates) is used for the cell.

Interconnection materials and device isolation lead process enhancements

As designers push to shrink circuits below $2\text{ }\mu\text{m}$, many new isolation schemes, interconnection material combinations, and device structures are emerging. In many of the memory and regularly laid out logic products, trench isolation may play an important role in reducing well-to-well spacing, latch-up, and chip size. However, as Hewlett-Packard Corp. (Corvallis, Ore.) points out, it is a very complex process, which adds about 25% to the process cost and may result in yield problems and crystal damage.

These impediments have not slowed the research, however, Texas Instruments Inc. (Dallas) has just studied CMOS trench isolation as a way of suppressing latch-up. Researchers used both the usual trench, with sidewall oxidation and polysilicon refilling, and a trench with a deposited insulator (the sealed sidewall trench process).

The results for several trench depths indicate that structures incorporating a $7\text{-}\mu\text{m}$ trench with oxide refilling require almost 100 times more trigger current than CMOS without a trench on an epi structure. The sealed sidewall process eliminates some problems associated with trench processing—namely, sidewall oxidation of the trench surface prior to polysilicon refilling and poly-

silicon cap oxidation during field oxidation.

With $1\text{-}\mu\text{m}$ -wide and $5\text{-}\mu\text{m}$ -deep trenches, an experimental submicron CMOS process has shown operation that is free of latch-up and has minimal n-to-p separation (Fig. 1). The process is being developed by the Corporate Solid State Laboratory of Honeywell Inc. (Plymouth, Minn.). It uses an epitaxial layer and creates lightly doped transistor drain structures in the layer to minimize the hot electron problems in the short-channel transistors. Circuits designed with this process operate from a 3-V supply and offer gate switching speeds of 200 ps and a gate speed-power product of 28 fJ.

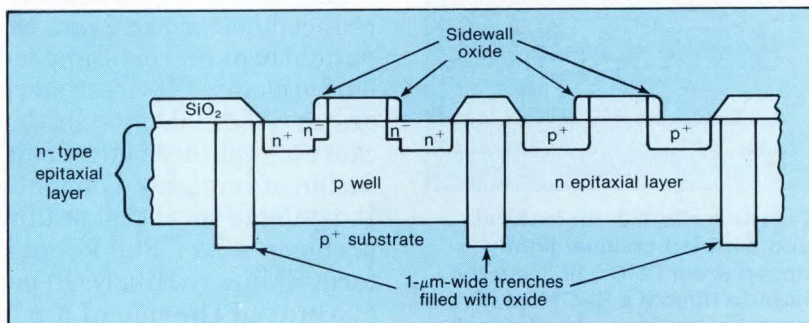
But it will take quite a while for trench structures to replace local oxidation schemes, even though the latter result in undesirable lateral oxide growth. However, hoping to overcome the problems in creating trenches, engineers at

the NEC Corp. (Kanagawa, Japan) are already examining a flexible trench structure. This can be formed in an arbitrary width—from submicron to several microns—and it is free from crystal defects during polysilicon oxidation. It also has minimal parasitic channel leakage.

Small trenches

The combination of a small trench and self-aligned guard rings is the path some researchers are headed up at the Stanford Electronics Laboratory (Stanford, Calif.). High-performance structures that are free of latch-up can be achieved when self-aligned, diffused lateral guard rings are created around PMOS FETs that have Schottky source and drain contacts. The PMOS transistors use a unique contact scheme that is laterally ohmic, but Schottky-like, in the vertical direction.

To form the hybrid contact structure, researchers modified a $2.5\text{-}\mu\text{m}$, n-well CMOS process so that the source and drain regions were slightly etched prior to the deposition of the platinum silicide con-



1. Working with trenches just $1\text{-}\mu\text{m}$ wide experiments at Honeywell devised lightly doped drain transistor structures that switched at speeds of 200 ps when operated from a 3-V power supply.

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tact material. Latch-up triggering currents in excess of 100 mA were required.

Epitaxial layers on silicon wafers are still the most common solution to the threat of latch-up. Studies at the 1- μm level by both IBM Corp. (Yorktown Heights, N.Y.) and Siemens AG (Munich, West Germany) show that CMOS structures free of latch-up can be built at 1- μm .

IBM's researchers built an n-well CMOS structure in a thin (4.5 μm) p-epitaxial layer deposited over a p^+ starting material. The structure requires a sustaining voltage that is larger than the supply voltage, thus eliminating the possibility of latch-up.

Siemens researchers have minimized channel doping, and thus the possibility of latch-up, by use of a dual-well structure and a tantalum silicide gate material. With effective gate lengths of 1.2 μm and a fanout of 1, experimental 27-stage ring oscillators have achieved gate delays of

120 ps (p-well) and 190 ps (n-well).

Additional work by Siemens in conjunction with the Technical University of Munich has led to a structure that resists latch-up and does not require epitaxial material. Instead the process tailors the well profiles in a dual-well structure by reducing the p-well depth and modifying the local oxidation step for generating the self-aligned well. The optimized well arrangement permits a reduction in the n-to-p spacing from 12 μm to 6 μm , with no deterioration of latch-up resistance.

Selective growth

The selective growing of epitaxial material where needed on a chip is the goal of work being done by Mitsubishi Electric Corp. (Itami, Japan). The company has developed an experimental process that permits selective epitaxial growth and local oxidation to isolate regions of the silicon. In the process, the active areas of the MOS devices are surrounded by a narrow oxide wall that has a constant width of 2 μm .

As feature dimensions are reduced below 1 to 2 μm , the punchthrough resistance of buried channel devices deteriorates rapidly. This occurs because of undesired lateral diffusion of implanted dopants. In trying to solve that scaling problem, AT&T Bell Laboratories (Murray Hill, N.J.) has evaluated the use of a p^+ -doped polysilicon with a silicide overcoat, instead of the typical n^+ based combination.

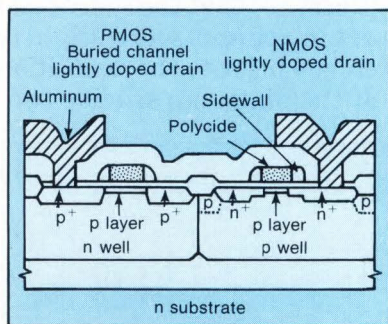
The arsenic dopant in the p^+ poly moves a lot slower through the silicon than the boron used for n^+ poly. This permits a more shallow and more optimized n-type transistor junction.

Third generation CMOS

A combination of n^- epi on an n^+ wafer, together with 1.5- μm lithography, are the key features of CHMOS III, a third-generation process developed by Intel Corp. (Santa Clara, Calif.). The process, well-suited for the fabrication of VLSI random logic, will be used for the company's next generation of 32-bit microprocessors. By using 250-Å gate oxides, 1- μm effective channel lengths, and two levels of metal interconnections, the process gives gate delays of less than 250 ps.

The use of the lightly doped epi layer permits n^+ to p^+ spacing of 5.5 μm with minimal latch-up sensitivity. And a self-aligned field implant that uses polysilicon as the implant barrier works in conjunction with the other steps in the manufacturing process to minimize the number of mask steps.

The use of a blanket implant instead of an epitaxial layer is being explored by the department of electrical engineering and computer sciences at the University of California at Berkeley. By exposing the wafer to a moderate dose, high-energy blanket implant after the well diffusion, a 2- μm -thick p^+ layer can be created 5 μm below the wafer's surface. That layer, in turn, guarantees a very sharp



2. Twin wells, 1.3- μm features, and a buried-channel lightly doped drain PMOS FET are the keys to Hitachi's Hi-CMOS III process. It will employ the technique to fabricate 256-kbit static RAMs and 32-bit microprocessors.

transition between the p^+ and p regions, hence thus better latch-up resistance.

A third-generation process dubbed Hi-CMOS III joins 1.3- μm lithography with a twin-well, nonepitaxial-based structure (Fig. 2). The technique, created by Hitachi, employs a self-aligned approach that permits the p -well, n -well, and field-implant layer to be formed with just a single mask. In that way, the overall process flow can be considerably simplified. A polycide combination is used to reduce gate resistance, and lightly-doped drain structures are employed for n -channel devices.

During development, the company found that in the optimum concentration range for the lightly doped drain structure, drain saturation current depended little on the length of the spacer (the doped isolation area). A length of 0.35 μm was selected. That permitted a new structure, called a buried-channel lightly doped drain p -channel FET, to be created. The shallow buried channel layer in the transistor enhances the effective electron mobility and effectively works like the lightly doped drain region under the spacer.

The common touch

Almost every scaled MOS circuit now incorporates the lightly doped drain or double-doped drain structure as a means of minimizing hot electron effects and improving the transistor voltage breakdown. Just those benefits have been realized for some

sub- 0.5- μm MOSFETs that have been created by Hughes Research Laboratories (Malibu, Calif.). PMOS transistors with gate lengths as short as 0.3 μm and gate oxide thickness as narrow as 100 Å have been created.

Several manufacturers believe that supercooling CMOS chips down to 77K will bring major speed improvements. Tests conducted at both Honeywell and the Semiconductor Devices Laboratory of Fujitsu Ltd. (Atsugi, Japan) show a decrease in propagation delay of roughly 40% when running 77K. Both evaluations were done using ring oscillator test circuits, and the speed-limiting factor turned out to be the velocity saturation effect of the silicon.

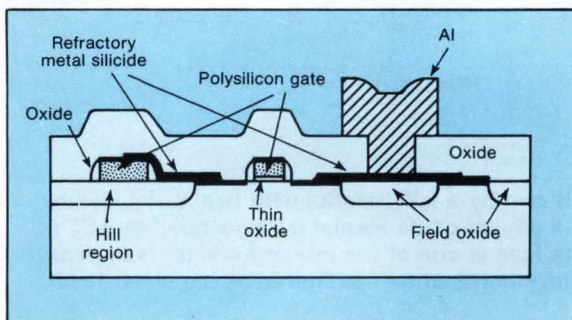
Opposites can attract

One interconnection scheme permits n^+ and p^+ diffusions and n^+ and p^+ gates of a CMOS circuit to be directly connected—without aluminum. Devised by Hewlett-Packard Co.'s Laboratories (Palo Alto, Calif.), the ap-

proach also obviates the need for a contact to be established over the source and drain regions (Fig. 3). Consequently, since the source and drain contacts can extend over the field oxide, the size of the diffusion regions can be kept to a minimum, making the chip very dense.

After the polysilicon gate is formed, as in a normal CMOS process, a sidewall oxide region is etched, and the source and drain regions are formed. A thin layer of a refractory metal and a level of amorphous silicon are deposited next. The amorphous silicon is then patterned, while leaving the underlying metal untouched. Any underlying polysilicon or oxide is thus kept from being exposed to the etching process.

The surface is now annealed, and the metal reacts with the regions of amorphous silicon to form silicided regions. The unalloyed metal is then eliminated with a wet etching step. Finally, the conventional steps for depositing oxide forming contacts, depositing second metallization



3. Any diffusions can be directly linked using a refractory-metal silicide process developed by Hewlett-Packard. The scheme employs an annealed combination of amorphous silicon and metal to form the silicide that is used as the first-level interconnection material.

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layers and etching patterns are completed.

One of the major problems being addressed in the depositing metal silicides is aligning the silicide to the region on which it is to be deposited. A number of self-alignment schemes are being examined, such as the method used to form titanium silicide developed by Mitsubishi Electric Co. (Itami, Japan).

Basically, the process starts by depositing a layer of silicon and then one of titanium. After that, a flashlamp is used to anneal the materials and to form the silicide. The method creates an oxide-free layer of titanium silicide and permits devices with gates as small as $0.8\text{-}\mu\text{m}$ to be had.

A combination of molybdenum and titanium-tungsten forms double-layer source and drain contacts

that supply good ohmic properties and eliminate spiking. The process, being developed by General Electric Co. (Schenectady, N.Y.), permits the formation of $1\text{-}\mu\text{m}$ contacts with very low resistances—less than $20\text{ }\Omega/\mu\text{m}^2$ for n^+ contacts and 20 to $50\text{ }\Omega/\mu\text{m}^2$ for p^+ .

Flattening the hills

As narrower interconnections are used, electromigration causes a problem called hillocks. Small hills of metal are formed, usually on the narrower, lower level, because of the electrical pressure, and these hills push up to the next level and cause a short circuit. In examining layering techniques, researchers at Stanford University found that a composite film of aluminum, silicon, and titanium offered a substantial reduction in hill-

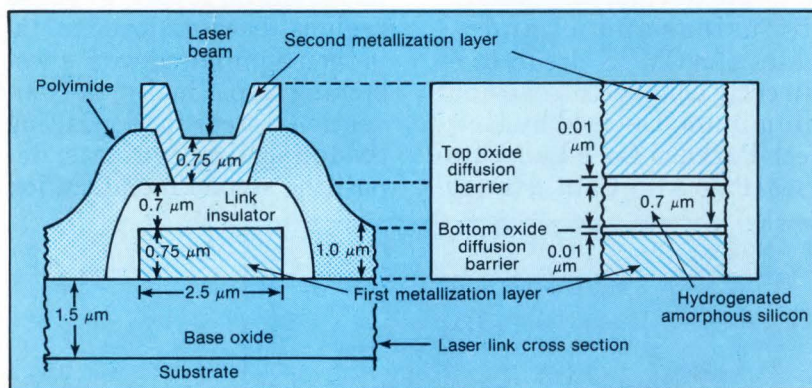
ock density and permitted smooth films with no more variation than $20\text{ }\text{\AA}$.

Arsenic ion implants can also be used to suppress hillock formation in multiple-level metalization systems, researchers at Ricoh Co. Ltd. (Osaka, Japan) found. The method developed not only solves the hillock problem and the shorts it causes, but also the opens caused by electromigration on the upper metal layer.

Looking toward wafer-scale integration, researchers are currently hunting for ways to find enough usable sites on the wafer for interconnections. Lincoln Laboratory of the Massachusetts Institute of Technology (Lexington, Mass.) has developed a laser-link shorting scheme that uses amorphous silicon and a $100\text{-}\text{\AA}$ silicon-dioxide insulating layer (Fig. 4). When the laser beam hits the top layer of metal, the metal melts and short-circuits the thin insulating layer. Aside from the fuse regions, the two layers of metal are insulated from each other by a layer of polyimide.

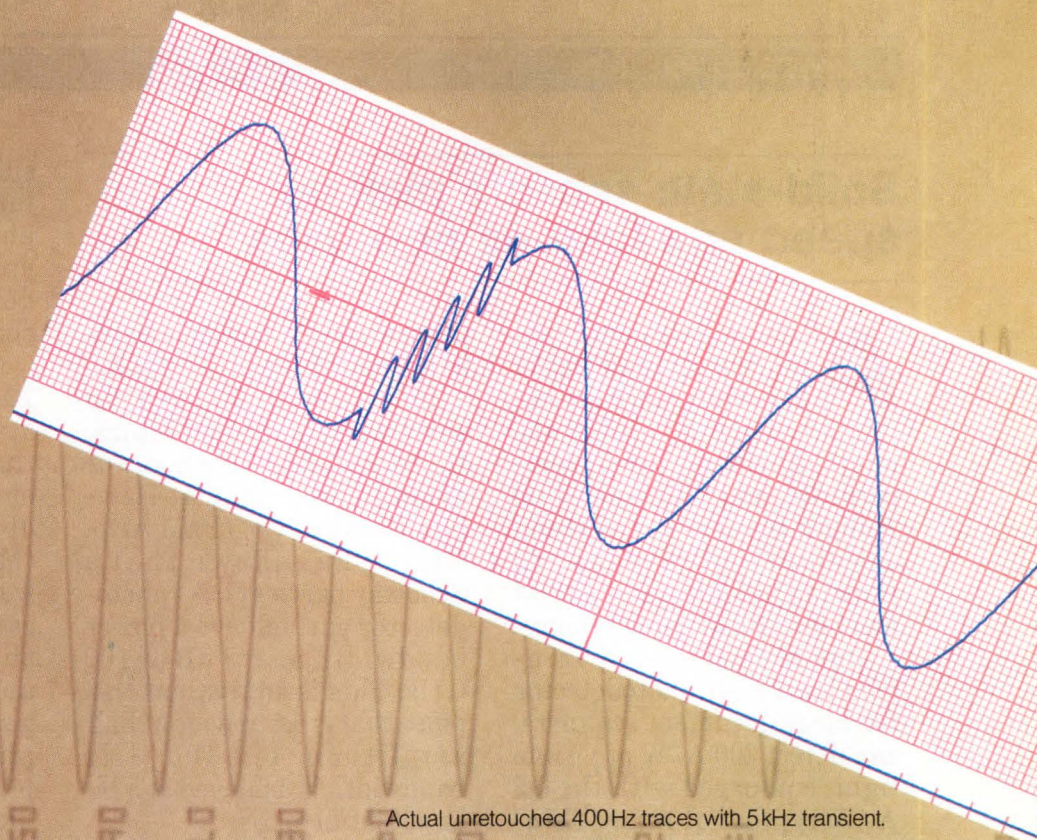
In this wafer-level project, sponsored by the Air Force and the Defense Advanced Research Projects Agency, both the shorting of fuses and the opening of metal links has been demonstrated to interconnect and to disassociate parts of the wafer. The scheme has been implemented with an array of logic cells to form a digital integrator in a 24-cm^2 area. The device operates at a 25-MHz data rate.

Dave Bursky



4. A fuse that can be blown by a laser works with two metal layers that are separated by a $0.7\text{-}\mu\text{m}$ oxide insulator. Developed by MIT's Lincoln Laboratory, the fuse is one of the integral elements in experiments related to circuitry that can be configured at the wafer level.

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Solid-state sensors pick up speed and take on new uses

Advanced levels of integration and new peaks in performance are being achieved in solid-state photo, pressure, vapor, temperature, and tactile sensors. Many of the devices have been developed in response to growing military, industrial and biomedical applications.

One such sensor, a thin-film transistor photodetector for large document scanners, can detect 300 A/W of visible light, compared with the 0.5 A/W typical of many thin-film photodetectors. Developed at Xerox Corp.'s Palo Alto (Calif.) Research Center, the n-channel, depletion-mode device has been fabricated from laser-crystallized thin films on a fused silica substrate (Fig. 1). Its performance is expected to allow vast system improvements in photodetector speed, resolution, and the integration of other circuits on a chip.

To make the photodetector, Xerox counterdoped the upper half of the channel region of an enhancement-mode, thin-film transistor with phosphorous ion implantation, thereby forming a shallow n-type conducting channel and a pn junction parallel to the substrate. When visible light is shone through the detector's substrate, responses of 300 to 900 A/W become possible. The researchers speculate that the high photosensitivity may stem from the spatial separation of photo-

generated electron-hole pairs in the detector's pn junction.

For truly high speeds in solid-state photodetectors, GaAs devices get the nod. For example, research at Hewlett-Packard Co. (Palo Alto, Calif.) has shown that a Schottky barrier GaAs photodetector can achieve a power bandwidth at -3 dB of 100 GHz. This is equivalent to a pulse that is 5.4 ps wide at half amplitude. The 100-GHz bandwidth is achieved at a bias potential of 5 V.

Transparent platinum

The device consists of a semitransparent platinum film that forms the Schottky barrier on an n^- layer. The layer is grown atop an n^+ GaAs epitaxial layer, and the entire assembly sits atop a semi-insulating GaAs substrate. The resulting device has less than 15 fF of para-

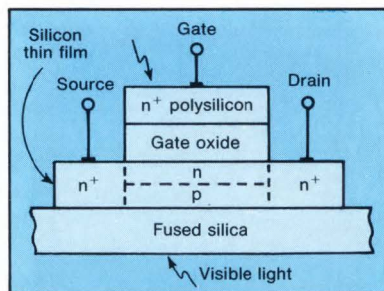
sitic capacitance and 20 fF of junction capacitance, with a photosensitive area of 5 by 5 μm . Plans are to integrate the detector with a FET on one chip.

GaAs also figures in a 1 by 12 compound semiconductor array of p-i-n photodiodes that achieves full optical and electrical interfacing. Developed at Bell Laboratories (Murray Hill, N.J.) for long-wavelength optical communication systems (those of less than 1.65 μm), the linear array consists of indium-gallium arsenide/indium-phosphide (InGaAs/InP) p-i-n photodiodes. The photodiodes are processed from a wafer of undoped InGaAs grown by vapor-phase epitaxy on an n^+ InP substrate. The p^+ n diodes are formed by diffusing zinc through openings in a silicon-nitride mask. N and p contacts are made to the InGaAs surface, and the diodes are illuminated through the substrate.

The array's optical-fiber interface uses multimode fibers placed in etched silicon blocks, making the array compatible with currently used fiber-splicing techniques.

Getting down to the infrared

Work on photodetectors is not just limited to the visible light region. Solid-state infrared detectors are also of much interest, particularly for military imaging. A favorite approach is to integrate NMOS detectors and CCD signal-processing elements on the same intrinsic mercury-cadmium-telluride



1. By ion-implanting the enhancement-mode, thin-film transistor region of a photodetector structure, Xerox has developed a photosensor that can detect 300 A/W of visible light—up to 900 A/W is possible when visible light shines through the device's substrate.

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(HgCdTe) chip.

That is what the Santa Barbara Research Center (Goleta, Calif.) did in building a front-illuminated linear HgCdTe array of 100 photo-detectors for the infrared region. The array is on a 2.1-by-5-mm chip, which also contains two 55-bit, four-phase CCD shift registers. Charge-transfer efficiencies of greater than 0.995 have been achieved at temperatures from 70 to 100 K.

At the University of California at Berkeley, researchers have integrated a 64-element infrared array of zinc oxide on a silicon substrate. The thin-film pyroelectric detectors are deposited on a planar-processed NMOS substrate that is anisotropically etched on the back. The array consists of a matrix of 8-by-8 pyroelectric capacitors, each 70 by 70 μm . The entire chip measures 800 by 800 μm . Because of their high pyroelectric coefficients of $1.5 \text{ by } 10^{-9} \text{ C/cm}^2\text{K}$, the capacitor detectors show promise as infrared imagers of low-contrast scenes at room temperature.

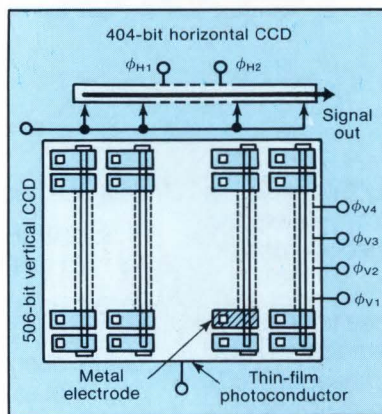
The Berkeley researchers point out that although lithium-tantalum-oxide (LiTaO_3) crystals, PZT ceramics, and polyvinylfluoride (PVF_2) polymers have been used as infrared pyroelectric detectors with similarly high sensitivity, ZnO-on-silicon detectors also have other advantages. They include compatibility with NMOS planar processing, low-cost fabrication of dense mosaic arrays, and ease of coupling of the

detected signal into CCD processing elements.

Beyond the infrared region, CCDs have been put to use as X-ray imagers by researchers at Texas Instruments Inc. (Dallas). They obtained the necessary spatial and spectral resolution in the imager by minimizing charge diffusion below the depletion region into the channel. To do this, they designed a CCD depletion region width that is comparable to the absorption region length of the highest energy X-ray to be detected.

CCDs scoring in visible light

It is in the visible light spectrum that CCD imagers are making their biggest impact. In fact, if researchers at the Central Research Laboratories of Matsushita Industrial Co. Ltd. (Osaka, Japan) have their way, CCD imagers will replace the much larger vidicon camera on a wide scale.



2. Four-phase transfer pulses in the vertical columns of CCDs allow Matsushita's 1/2-in. imager to handle more signal charges and increase its operating characteristics. The device has 404 horizontal by 506 vertical pixels, overlaid with a hydrogenated thin film of amorphous silicon.

They have fabricated a 1/2-in. CCD imager, overlaid with a hydrogenated thin-film layer of amorphous silicon, and have obtained good results.

At a low bias potential of just 3 V, the researchers have obtained a quantum efficiency of 0.75 to 0.8 in the visible light region, a smearing signal below 5% at a light intensity 5000 times that of saturation levels, and complete suppression of blooming and highlight lagging effects. The interline-transfer, buried-channel device has 506×404 cells, each 17 by 10 μm . To increase the imager's ability to handle signal charges, the vertical CCDs are operated by four-phase transfer pulses (Fig. 2). Two-phase pulses are used for the horizontal CCDs.

The imager also features a saturation signal current of 300 nA and signal-to-noise ratios of 71 and 68 dB for random and fixed pattern noises, respectively.

Resolution and chip size in CCD imagers are often conflicting goals. Increasing the number of pixels without changing pixel size comes at the expense of a larger silicon chip. Now, however, with a new clocking method for a frame-transfer CCD imager, the number of pixels in the vertical direction on a CCD chip can be doubled without changing the size of the silicon chip. The method was developed by Philips Research Laboratories (Eindhoven, the Netherlands).

The Philips researchers used an accordion-like layout of the CCD elements to come

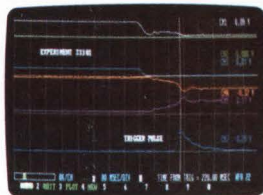
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up with a 5.46-by-7-mm (horizontal times vertical) chip, or an area 38.22 mm^2 . On the chip are 588 interlaced lines, with 604 pixels on each line. Each pixel measures $7 \mu\text{m}$ horizontally by $11 \mu\text{m}$ vertically, and all are on $3\text{-}\mu\text{m}$ centers. According to the researchers, if the same number of pixels were put down on a CCD imager with conventional layout rules, a chip area of 66.5 mm^2 would be required. Because of the doubling of resolution without change in chip size, smearing effects are cut in half and the drive electronics are more compact and simplified.

Although optical sensing with solid-state devices is receiving considerable attention in the laboratory, other forms of solid-state sensing are also making headway. They include pressure, vapor, temperature, and tactile.

One sensor, a stable absolute-pressure silicon type for use in the human body, comes with signal-processing circuitry on the chip. It was developed at the Integrated Circuits Laboratory of Stanford University in California. The piezoresistive device measures 1 by 0.6 by 5 mm and is designed for mounting in a catheter tip. It employs a novel lead attachment structure that gives it strength, resistance to corrosion, and a small cross-sectional area.

The structure includes three V grooves, each 0.1 mm wide by 0.07 mm deep and created within the silicon wafer during fabrication within the V grooves and covered by glass through an anodic bonding process. The grooves thus become tunnels into which chip-wire attachments can be soldered.

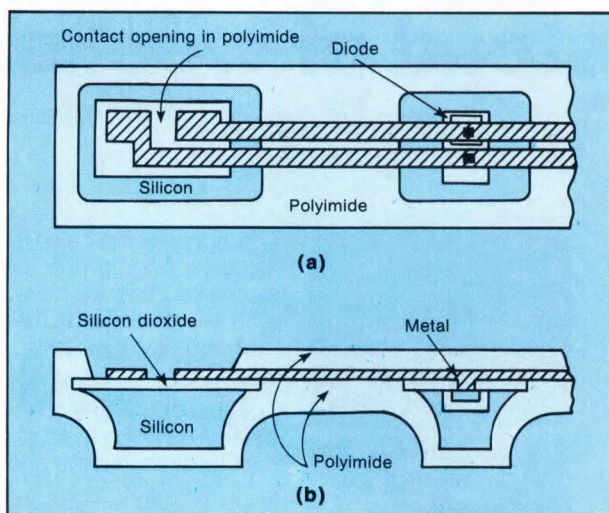
Circuitry is fabricated at

the bottom of a $5\text{-}\mu\text{m}$ -deep well that is hermetically sealed by the same anodic bonding process. The circuit sealing occurs at the same time that a shallow cavity is sealed over the 0.5-mm^2 silicon sensing diaphragm. The process creates an absolute pressure reference.

A microbridge monolithic vapor sensor has been devised in a joint effort by researchers at the University of California at Berkeley and Carnegie-Mellon University (Pittsburgh, Pa.). The device consists of a polycrystalline silicon microbridge $1.35\text{-}\mu\text{m}$ thick by $153\text{-}\mu\text{m}$ long by $15\text{-}\mu\text{m}$ wide, an underlying electrode for electrostatic excitation, and an integrated NMOS circuit for capacitive pickup of the vibration of the resonating microbridge.

Organic vapors are detected when they are absorbed by a thin polymer film on the microbridge. The absorption increases the microbridge's mass loading, causing it to break into resonance. At the first harmonic, the phase difference between the sensor's excitation voltage and the detection circuit's output voltage is the output signal.

Saturated xylene vapors cause a phase shift of -8° when the microbridge is first excited at its nominal first-harmonic resonant frequency of 244 kHz. The response time is less than 7 minutes. Any further changes in xylene concentration cause an addition phase shift of $-0.3^\circ/\text{ppm}$, a sensitivity some 20 times greater than with SAW (surface acoustic wave) vapor



3. The plain view (a) and cross-sectional view (b) of Stanford University's batch-fabricated silicon thermometer array show how a polyimide layer covers both the p-n diode sensors and their connecting gold wires. Designed for use in the human body, the array is 3.5 cm long by 1 mm wide by 0.4 mm thick. It has 20 diodes.



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sensors which are coated with polymer films of the same thickness.

At Stanford University, batch-fabricated silicon thermometer arrays have been developed for measuring a patient's temperature profile during hyperthermic treatment of cancer (Fig. 3). Twenty silicon islands, each containing a p-n diode to measure temperature, make up a linear array that is 3.5 cm long

by 1 mm wide by 0.4 mm thick. The diodes are connected by gold wires and are embedded, along with the wires, in a flexible polyimide layer.

The researchers are also fabricating even larger arrays that are 10 and 20 cm long. These, they believe, could prove even more useful for applications related to cancer tumors by being able to measure over a larger area.

Roger Allan

Silicon-on-insulator technology: On a steady path to maturity

As one of the newer kids on the block, silicon on insulator technology has made quite an impression on the semiconductor industry. Not only does it make three-dimensional integration a viable alternative to wafer-scale integration, it could also reduce the expense of dielectric isolation. Transistors will be faster for a given geometry, and isolated power control transistors could plunge in cost.

The industry is already familiar with such silicon on insulator developments as implanted oxygen, recrystallized polysilicon, and FIPOS (full isolation by porous oxidized silicon). Add to those staples a new process in which wafers are "glued" together and then interconnected with vias. In some respects, it turns a wafer into a three-dimensional hybrid.

NEC Corp.'s Microelectronics Laboratories (Ka-

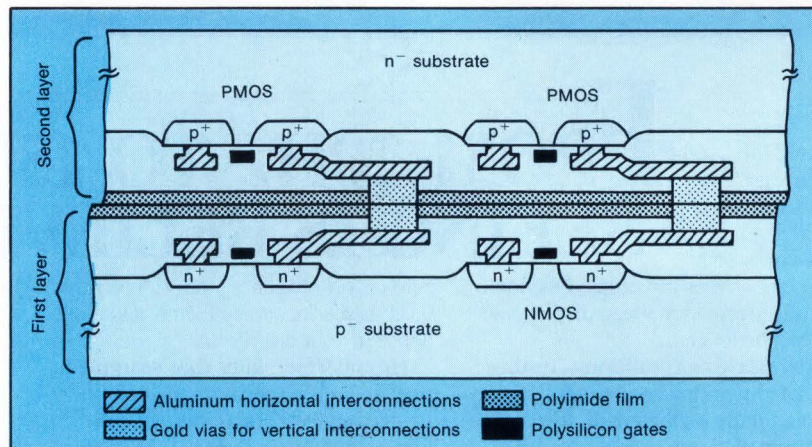
wasaki, Japan) fabricates individual LSI wafers with conventional techniques and then interconnects them physically and electrically. Following those steps, a 2- to 3- μm layer of polyimide is spin-coated on one side of each wafer. That insulating film serves three purposes: It flattens the wafers, bonds

them together during stacking, and acts as a packing material between them.

Next the film is partially cured, maintaining a degree of stickiness, and then selectively thinned until the gold vias are exposed. The polyimide-coated surfaces of the wafers are bonded and aligned so that the vias make contact. The wafers are subsequently thermally compressed to connect the vias. The gold vias themselves are 2 and 3 μm high and form a cross-section of 10 by 10 μm . They can be used for future vertical wafer connections.

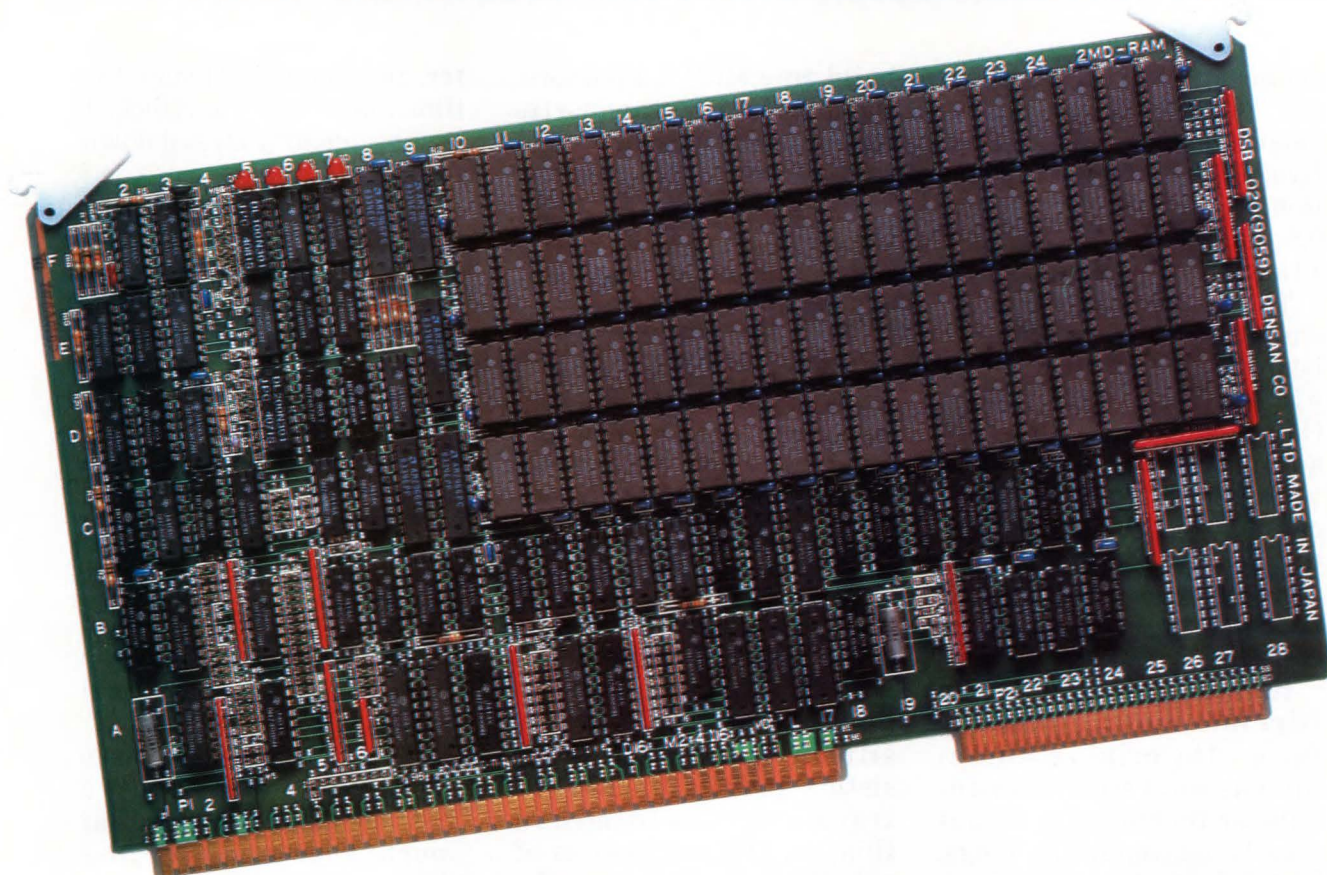
In NEC's experimental versions, 52,000 vias were perfectly connected on each 5-mm² die (Fig. 1), and each pair of mated vias is measured for a tensile strength of 4 mg.

NEC built two 31-stage ring oscillators on the chips: One puts all the p-channel devices on one wafer and the n-channel devices on another. The second alternates inverters



1. A new 3D integration technique, developed by NEC, fabricates two transistor-bearing wafers separately on standard equipment and then "glues" them together with a polyimide film. The wafers are connected with gold vias, which are joined by thermal compression.

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between top and bottom layers. The first approach uses one via per stage, the second five vias per stage. Propagation delays in the circuits are 0.8 and 1.86 ns for supplies of 10 and 5 V, respectively.

The wafer-glue technique should produce a variety of benefits, ranging from a complete mixing of bipolar, CMOS, and even gallium arsenide technologies to high-voltage isolation. Moreover, it can be extended to additional layers, and the production yield should be high because each wafer is tested before stacking.

Recrystallizing polysilicon film into monocrystalline form—the original three-dimensional silicon-on-insulator technology—is not merely waiting in the wings. Though most versions can

build only MOS transistors, scientists at Massachusetts Institute of Technology's Lincoln Laboratories (Lexington, Mass.) have successfully transferred the process to wafers that combine bipolar and CMOS technologies.

The integrated technique starts by growing a layer of oxide on a silicon wafer, depositing polysilicon on top, and then annealing, or zone-melting, the polysilicon. Those steps convert the material into monocrystalline form.

With that approach, the scientists fabricated two silicon-on-insulator structures. In the first (Fig. 2a), the silicon-gate CMOS transistors and the npn bipolar transistors are formed in film, using an extra layer of polysilicon for the gate, emit-

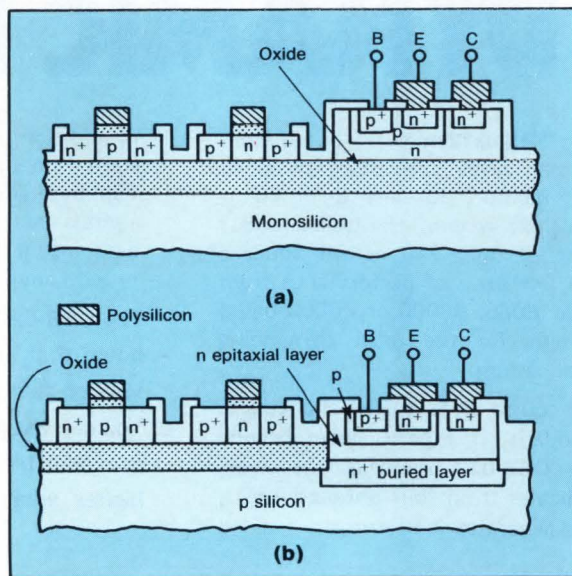
ter, and contacts. Though the film is laid down 1 μm thick, it is subsequently etched down to 0.3 μm .

In the second structure (Fig. 2b), the MOS transistors are incorporated in film, but the npn transistor is in an n-type epitaxial layer that grows on the original p silicon substrate (a window must first be etched in the oxide). The resulting structure is extremely flat, simplifying metal interconnection and passivation. Both npn structures have betas of 100, but the collector resistance of the bipolar film units is higher than that of the epitaxial devices.

The CMOS transistors have already been used in a 39-stage ring oscillator that sports gate delays of just 280 ps at 5 V. The npn transistors on the silicon film achieve a V_{CBO} of 45 V, whereas those on the epitaxial layer reach only 30 V. (The difference is attributed to the oxide layer beneath the 45-V device).

Lincoln Labs has also built silicon-on-insulator MESFETs in recrystallized film, which is laid down on a bulk, fused-silica substrate—that is, quartz. The process resembles silicon on sapphire, but with much less expensive material. The device's gates are 1.4 μm long and exhibit a transconductance of 45 mS/mm at a gate voltage of +0.3 V. The maximum oscillation frequency is 9 GHz, and the gain reaches 14 dB at 2 GHz.

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2. At MIT's Lincoln Laboratories, the recrystallization of polysilicon film has built bipolar (as well as MOS) transistors with two versions of the same process. The first version builds npn transistors in the film, as with FETs (a). In the second the transistors are built in the p substrate through a window etched in the oxide (b).



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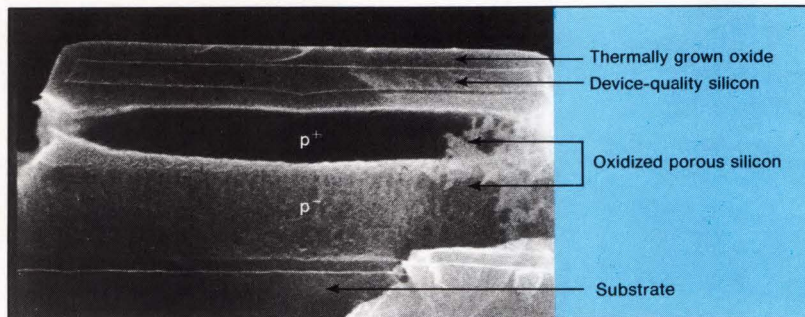
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3. IBM's modified FIPOS process (full isolation by porous oxidized silicon) produces islands of silicon completely surrounded by a layer of dense, thermally grown oxide. Transistors, dielectrically isolated from each other, are then fabricated in the silicon islands.

heaters for recrystallization of silicon-on-insulator film. In this technique a continuous-wave argon laser scans the polysilicon, melting it in the process. The Commissariat à l'Energie Atomique (Grenoble, France) has taken that approach to build 1- μ m CMOS devices, which when incorporated in a 101-stage ring oscil-

lator produce gate delays of only 93 ps. A comparable circuit in bulk CMOS has delays nearly twice as long.

Starting with device-quality monosilicon proves a big advantage in constructing silicon-on-insulator devices. Whether the process uses full isolation by porous or oxidized porous silicon, it pro-

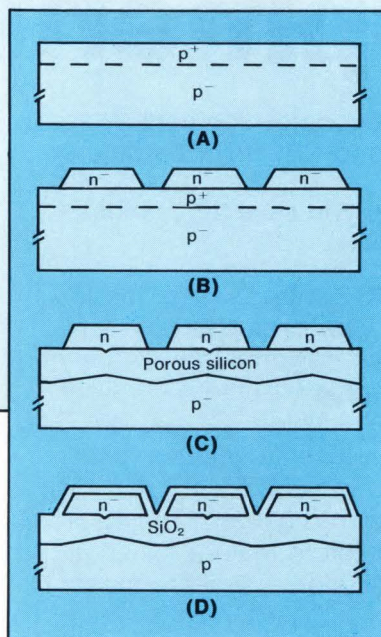
duces islands of silicon that are isolated from each other and from the substrate by dense, thermally grown oxide (see "Creating Silicon Islands," below).

Some unique processing problems have hampered its wide acceptance: The size of the islands is limited; the resulting wafers are excessively warped; and regardless of the quality of the silicon layer, defects develop during oxidation of the porous silicon. However, in modifying the standard technology, IBM Corp.'s General Technology Division (Essex Junction, Vt.) has come up with answers.

IBM puts a layer of p^+ silicon beneath the n^- material in which the transistors are fabricated. Since the p^+ silicon anodizes faster than the p^- silicon, relatively large is-

Creating silicon islands

The familiar silicon-on-insulator process called full isolation by porous oxidized silicon—or FIPOS—creates islands in a sophisticated manner. First a p^+ layer is added to a starting p^- layer (Fig. A) and a thin n^- epitaxial layer is placed on top of the p^+ silicon. A pattern is etched into the islands (Fig. B). The isolated transistors form in this n -type material.



Next the wafer is anodized to form a layer of porous silicon beneath the epitaxial layer (Fig. C). Anodizing renders the p^+ and p^- materials porous, but not the epitaxial layer. Finally the wafers are oxidized, turning the porous silicon into oxide and also growing a layer of dense thermal oxide on the top, the bottom and the edges of the n^- silicon (Fig. D).

DDC NEWS

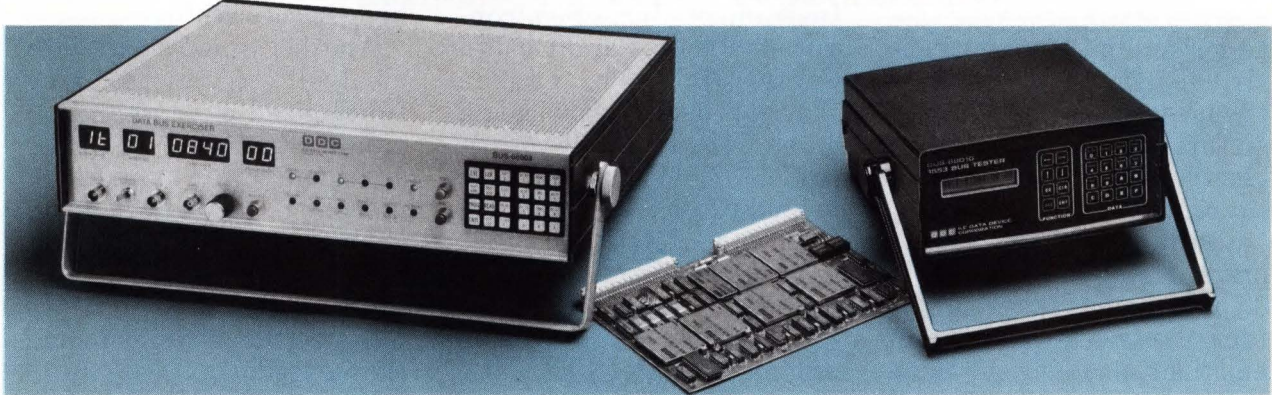
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lands (30 μm wide) can be isolated by porous silicon only 2 to 3 μm thick. Oxidation of the porous silicon at 800°C and a pressure of 10 atmospheres (rather than 1000°C and ambient pressure) together minimize warping and virtually eliminate defects. A cross-section of the transistor, taken by a scanning electron microscope, shows the results (Fig. 3).

Using ion implanters to drive massive doses of oxygen 0.5 to 2 μm beneath the surface of a good silicon wafer and then annealing the material produce a layer of oxide

under the monocrystalline silicon. According to many, that technique will win out for planar silicon on insulator (that is non-three-dimensional). Engineers at Texas Instruments Inc.'s Semiconductor Process and Design Center (Dallas) have taken that approach to fabricate a 4-kbit CMOS static RAM, using 2.5- μm design rules. The buried oxide layer is 0.5 μm thick and located under 1200 Å of silicon. The transistors were built in a 0.5- μm epitaxial layer grown on the original silicon.

Frank Goodenough

Still strong, bipolar circuitry gets new vigor from MOS techniques

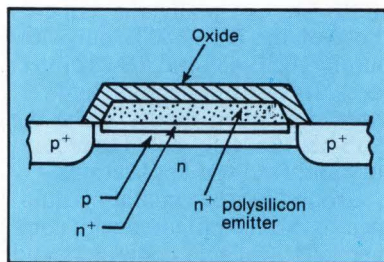
Though the semiconductor industry is rushing madly to adapt MOS processes to everything from high-speed logic to high-voltage ICs, bipolar technology has remained anything but static. In fact, it continues to break into new frontiers, helped along partly by techniques that it, too, has borrowed from MOS technology.

Consider just some of the MOS-like innovations that bipolar technology is now building on:

- Transistors with polysilicon emitters and with structures that resemble p- or n-channel devices.
- Self-alignment techniques that yield a better match between base-to-emitter voltage and speed.
- Polysilicon contacts coated

with a layer of silicide.

A polysilicon emitter contact and a thin layer (3 nm) of thermally grown oxide at the interface between the polysilicon and the monosilicon have produced an npn transistor with a beta of 300. The structure, created by Siemen



1. To improve gain and raise speed, bipolar transistors are picking up the tricks of MOS devices. For instance, Southampton University combines self-alignment with a polysilicon emitter, plating an oxide layer between the emitter and base.

AG's Central Research Laboratories (Munich, West Germany), brings high current gain and low impedance to the shallow junction devices that will be needed for tomorrow's high-speed circuits.

Another group starts with a polysilicon emitter being fabricated with chemical vapor deposition and then adds controlled amounts of nitrous oxide. Those steps characterize a process that creates a layer of semi-insulating oxide at the interface between the polysilicon and the monosilicon.

When properly annealed, say researchers at Stanford Electronic Laboratories (Stanford, Calif.), the oxide will conduct well enough to reduce emitter saturation current from 10^{-12} to less than 10^{-13} Acm^2 . Such gains lend themselves to devices as basic as fast transistors or to applications as sophisticated as increasing the energy efficiency of solar cells.

By moving to a self-aligned polysilicon emitter similar to the one found in MOS transistors (Fig. 1), England's Southampton University not only improves transistor speed but also raises beta by a factor of 10. The latter figure is due largely to the interfacial oxide, which resembles that used in other devices.

These and other MOS-based processes are being used to build more than discrete transistors. For instance, an unusual three-dimensional bipolar process has produced a ECL-based memory cell that boasts read and write times of less than

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15 ns. Designers at Fairchild Research Center (Palo Alto, Calif.) use polysilicon for the 100-M Ω resistors, diodes, and transistor bases and emitters and also put self-aligned titanium silicide on those bases and emitters. The low resistance of the silicide-coated polysilicon layer affords the requisite cross-coupling between transistors, as well as between the V_{CC} and bit lines. The diodes are formed with n^+ and p^+ polysilicon atop the field oxide.

That assortment of techniques has produced the fast ECL-based memory cell, which is designed with 2- μ m rules and occupies a mere 200 μ m² of silicon. Fairchild Research has already built an array of 4 by 4 memory cells and eventually plans to use the cell in 64-kbit ECL-based static RAMs.

To build extremely fast ECL circuits, transistors must be scaled down to the submicrometer level, yet the current must remain at some optimum level, making current density very high. To fabricate these scaled down chips, NEC Corp. (Kanagawa, Japan) takes advantage of

self-alignment, 1.25- μ m lithography, very shallow junctions (0.08- μ m polysilicon emitters and 0.2- μ m collectors), and a 1- μ m-thick epitaxial layer. Their beta runs to 100 and f_T to 9 GHz.

Together these techniques have produced an ECL gate with a delay of under 80 ps at a current density inside the transistor of 350 μ A/ μ m². The four-transistor ECL gate dissipates just 5.8 mW.

CMOS magic

Scaling down devices is particularly important in VLSI devices and circuits. On one hand, the packing density of scaled bipolar devices is limited mainly by power dissipation; on the other, CMOS reduces power consumption, but its low drive capability generally makes it slower than bipolar technology. A bipolar-CMOS process developed at the laboratories of Hitachi Ltd. (Tokyo) solves the problem by putting both types of devices on one chip (Fig. 2).

In the 2- μ m process, the npn transistors have a beta of 80 and a cut-off point of 4 GHz. Collector resistance is

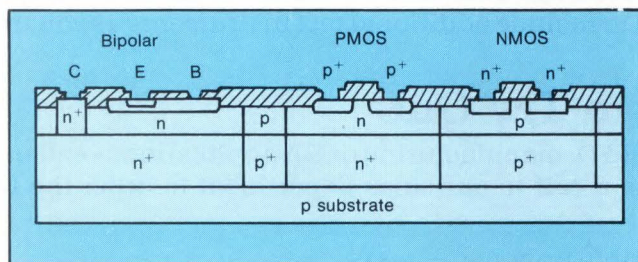
just 100 Ω . When used in a memory cell, a 2-V swing on the data line yields a gate delay of only 2 ns when driving a 6-pF load.

Whereas in most cases bipolar processes are picking up MOS traits, the reverse happens occasionally. For example, to eliminate the alpha particles that cause soft errors in static CMOS RAMs, Toshiba Ltd. (Kawasaki, Japan) interposes a buried p-layer between the storage node and the p well. Experimental results reveal an improvement of 1000 to 1.

Bipolar's promise in digital circuitry does not overshadow its potential in analog circuitry. One process, geared for high-speed data converters, uses self-aligned bases and emitters to produce complementary npn and pnp devices with good matching, wide bandwidths, and viable betas. Matsushita Ltd.'s Central Research Laboratory (Osaka, Japan) pegs the three-sigma deviation in V_{BE} at just 200 μ V, and the frequencies of the pnp and npn transistors are, respectively, 6 and 1.5 GHz. The current gain of the pnp device is set at 100, the npn transistor at 40 to 80. Moreover, their betas remain constant from 10^{-9} to 10^{-4} A.

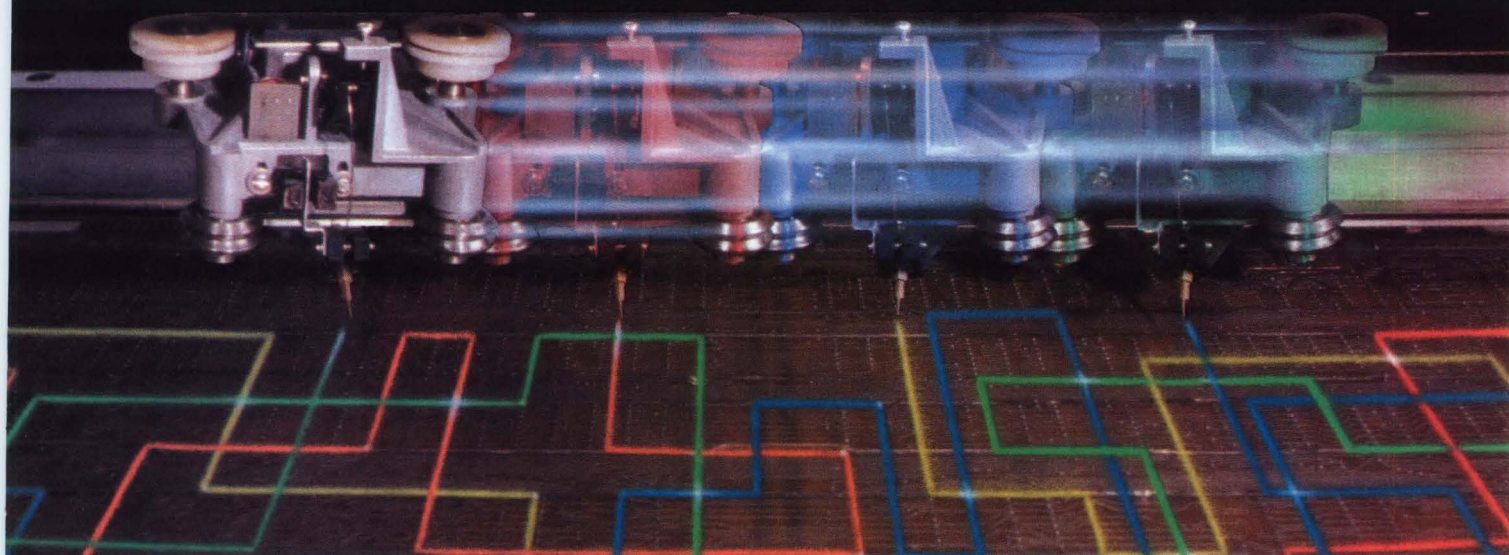
Silicon holds its own

Though many consider gallium arsenide the answer to digital circuits running faster than 1 GHz, silicon may have some high-speed surprises in store. Consider a dual-modulus prescaler that works with input signals of up to 1.6 GHz. Fujitsu Ltd. (Ka-



2. Competing with gallium arsenide, gigahertz performance has been achieved in a combined bipolar and CMOS process. The structure, devised at Hitachi, produces a beta of 80, a cut-off frequency of 4 GHz, and a collector resistance of 100.

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CONFERENCE PREVIEW

wasaki) labels it faster than any similar chip, whether silicon or gallium arsenide. For instance, its 185-ps gate delays are two-thirds the delays of silicon chips running at

only 1.3 GHz.

The company builds the divide-by-64/65 or divide-by-128/129 ECL-based prescaler with an oxide-isolated process that employs two layers

of metal, an n^+ buried layer, and an n epitaxial layer. The chip consumes less than 60 mW, about a third that of earlier silicon chips.

Frank Goodenough

Voltage ratings rise rapidly for ICs and midrange gated parts

Progress in solid-state power and voltage control is forging ahead just as rapidly as the development of ICs for microprocessors—and in many instances faster. TTL shift registers with active 850-V output drivers are showing up, and 180-V TTL-driven gates that hold delays to just a few nanoseconds are here as well. Further, a double-diffused MOS device has been wed to a silicon controlled rectifier, yielding a component that demonstrates gate control superior to that of a gate turn-off thyristor and 1200-V conductivity-modulated devices are starting to appear.

Having three NMOS transistors at each output stage (one full pullup, one for pull-down and one for output protection), a 16-bit shift register with 16 outputs is capable of switching 700 V. It also boasts a 150-V margin for safety and reliability. The output transistors owe their performance to the pair of polysilicon field plates located above the thick field oxide.

When the output is low, the chip can sink 5 mA at 600 V. From the Palo Alto Research Center of Xerox Corp. (Palo

Alto, Calif.), the complete chip, with shift register and gating logic, is just 5.46 by 5.46 mm.

A TTL-compatible IC process can toggle a 180 V push-pull output stage at 20 MHz. Known as semiwell isolation technology, the process can build 180-V npn and pnp transistors, 350-V substrate pnp devices, as well as n-well npn and non-n-well npn and pnp transistors rated at 30 V.

Current gains of all but the low-voltage pnp transistors run from 50 to over 100. And the logic circuitry from the process, devised at Hitachi Ltd.'s Central Research Laboratory (Tokyo, Japan), can be either complementary Schottky transistor logic or I^2L . The first toggles at 80 MHz and can be packed four times as densely as Schottky TTL. The I^2L toggles at 5 MHz. Gate delays have reached 2 ns.

The critical factor

The key to putting high-speed and low-power logic on the same chip is found in the portion of the structure that contains a low-resistance layer of n-type material. The material also is crucial to the

substrate pnp transistor used to build the high-voltage complementary source follower.

Creating ICs with high-voltage output states is usually simplified by going with lateral rather than vertical transistor structures. Several transistor types lend themselves to this purpose, including a lateral DMOS device. Designers at the Phillips Laboratories Division of North American Phillips Corp. (Briarcliff Manor, N.Y.) chose to build three different structures for a comparison.

One was a lateral DMOS device, the second a lateral IGT, and the third a lateral BMOS transistor—essentially a bipolar and MOS device in parallel (Fig. 1). All three were created with a silicon-gate DMOS process with a breakdown voltage of 300 V. The FETs' threshold voltage was 3 to 4 V, and the current gain of the lateral npn transistors was 40.

Food for thought

At low current densities, the chips in which the FETs carry most of the current demonstrate the lowest voltage drop. However, at greater densities the lateral insulated gate transistors (IGT) takes the lead. On the other hand, if switching speed is a prime concern, the lateral DMOS device wins hands down. It

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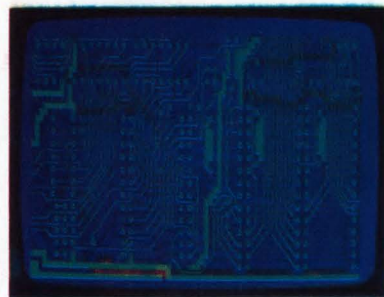
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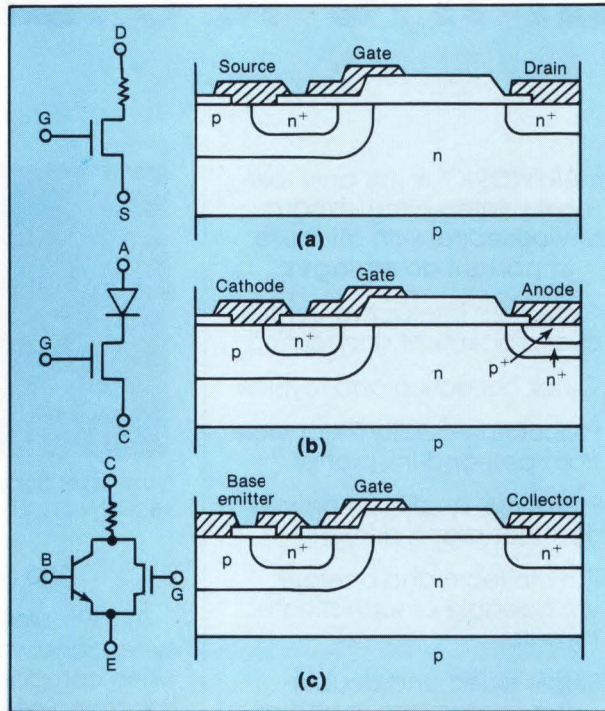
System Requirements

- ☐ IBM PC or XT with 192K RAM, 2 disk drives and DOS Version 2.0
- ☐ IBM Color/Graphics Adapter with RGB color or b&w monitor
- ☐ Epson MX-80/MX-100 or FX-80/FX-100 dot-matrix printer
- ☐ Houston Instrument DMP-41 pen-and-ink plotter (optional)
- ☐ Microsoft Mouse (optional)

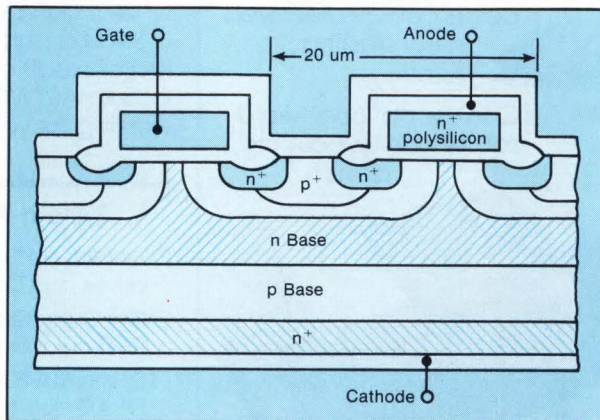


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CONFERENCE PREVIEW



1. For comparison, three laterally structured double-diffused MOS transistors rated at 300 V were constructed: a plain transistor (a), an IGT (b), and a BMOS device (c). The DMOS transistor was the fastest and had the lowest drop at low current densities. The IGT was the most silicon efficient.



2. The MOSTOT, like the IGT, integrates bipolar and MOS power devices. However, when the former's MOS transistor is gated on it runs off the SCR.

turns on and off in a few nanoseconds as opposed to the 1 to 10 μ s needed by the others.

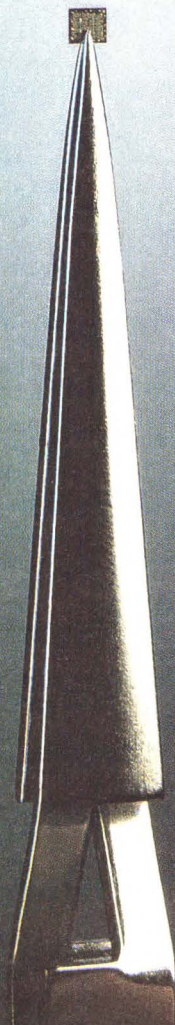
The much heralded conductivity-modulated devices that burst on the scene roughly 18 months ago can still learn a lesson in making the most efficient use of silicon from the SCR and the GTO. The just introduced MOS-controlled thyristor (MOSTOT), though, is simpler to turn on and off than a GTO and is just as efficient. Like the IGT, it integrates bipolar and MOS technologies.

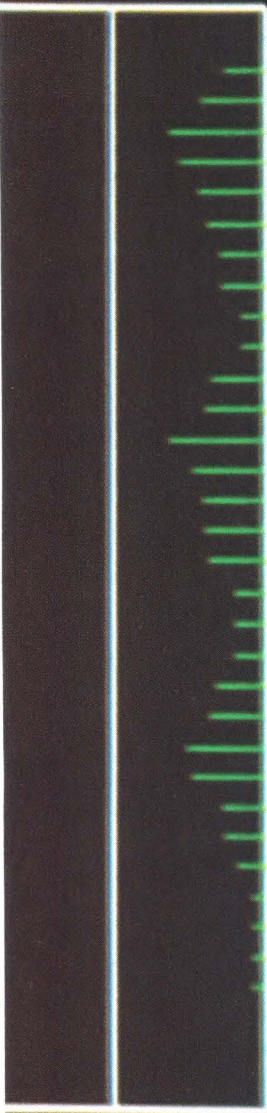
In the MOSTOT's structure (Fig. 2), the FET directly turns off the SCR. From a functional point of view, it does the same job as a GTO, however, it does so by shunting its load current for a short period of time. The MOSTOT's current density runs 50 to 100 times that of an IGT—for the same forward voltage drop. Speed, on the other hand, is comparable with that of the GTO.

The MOSTOT, developed by researchers at General Electric's R & D Center (Schenectady, N.Y.), still has a way to go to catch up with that company's IGT. That efficient power switch has overcome many of its earlier problems. Its latest incarnations include 300-, 600-, and 1200-V n-channel devices and 600-V p-channel units all with switching times in the 4 μ s range. What's more, by controlling electron irradiation of the wafer, speed can be traded off against forward voltage drop.

Frank Goodenough

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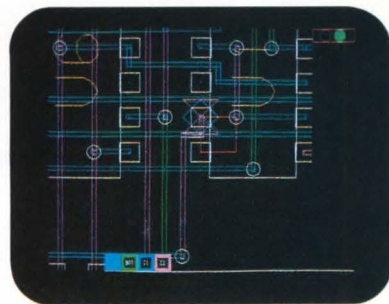
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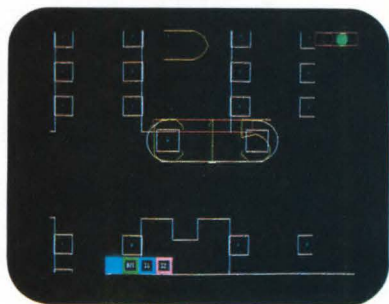
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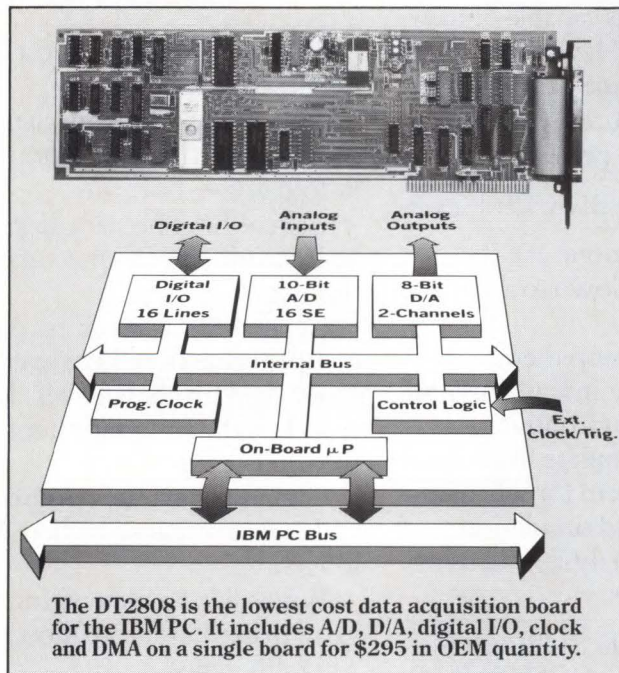
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Motorola Reports

NOVEMBER ISSUE 1984

VMEmodules: valuable system investments



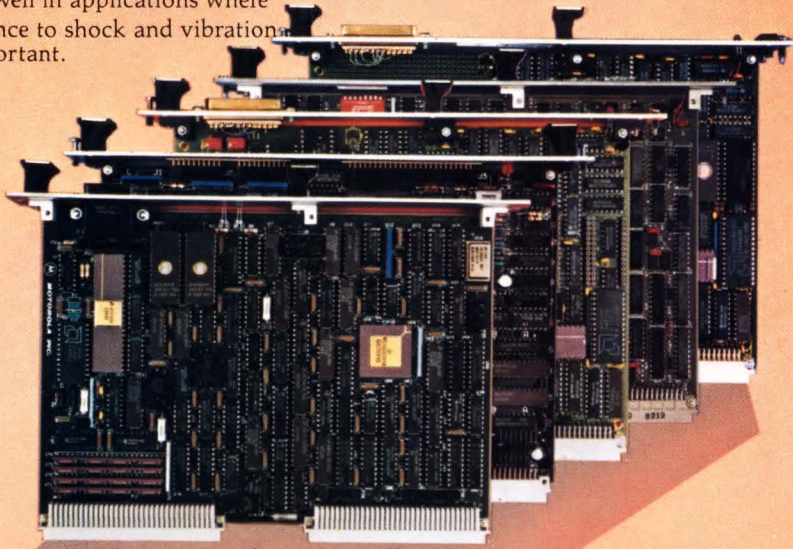
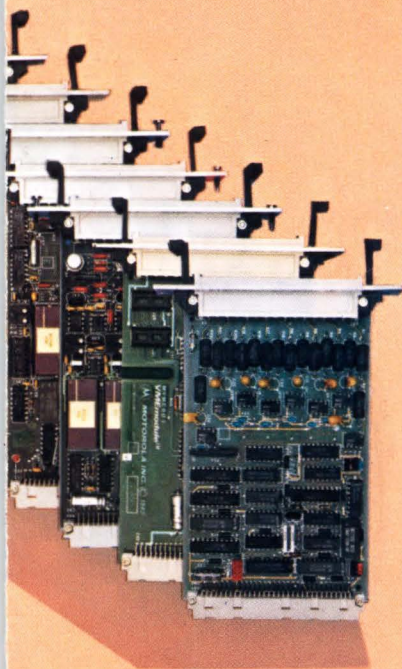
- ☐ RGB encoder generates studio color
- ☐ MC68010 now on VERSAmodule monoboard
- ☐ Evaluate MC68020 with the Benchmark 20
- ☐ Software flood for VME/10 microcomputer



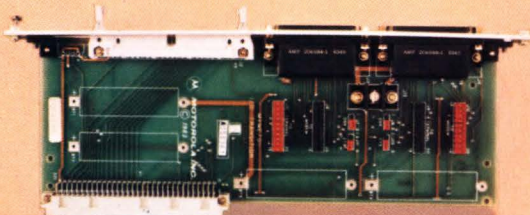
MOTOROLA

Overview

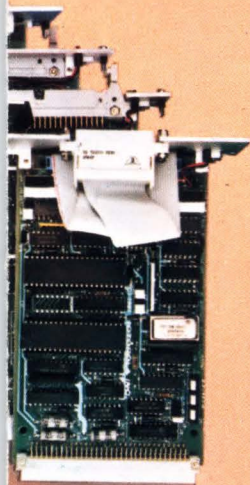
Adopting the popular Eurocard mechanical format, VMEmodules are available in two pin-out compatible sizes. Single high and double high board are used to afford a high degree of space flexibility for system configurations. Pin/socket connectors, card cages, backplanes, and plug-in power supplies all meet rigid DIN and IEC standards, and perform especially well in applications where resistance to shock and vibration is important.



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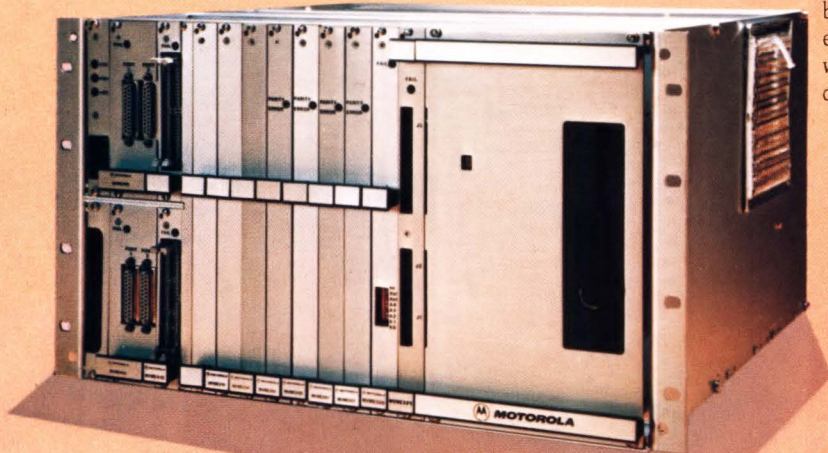


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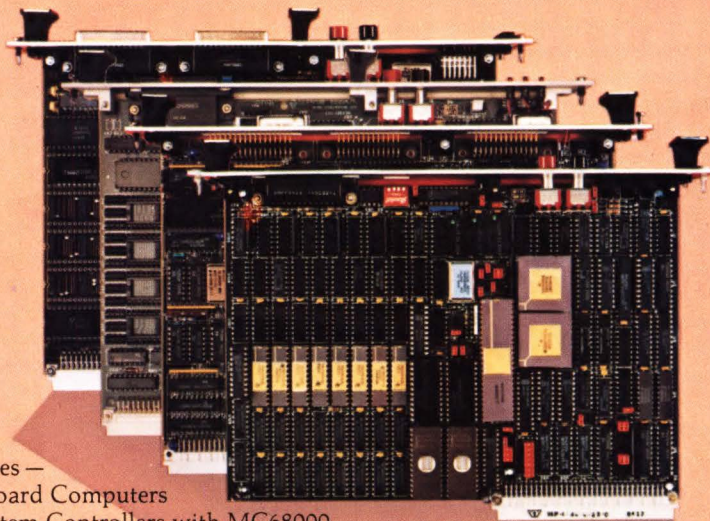
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900 Series — Packaging Hardware
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 extender boards
 wire wrap boards
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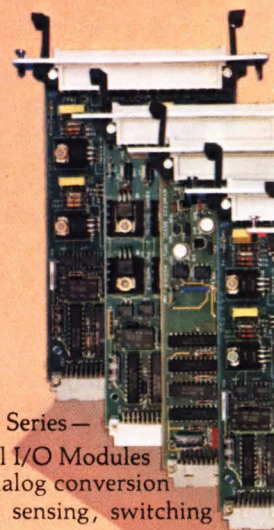




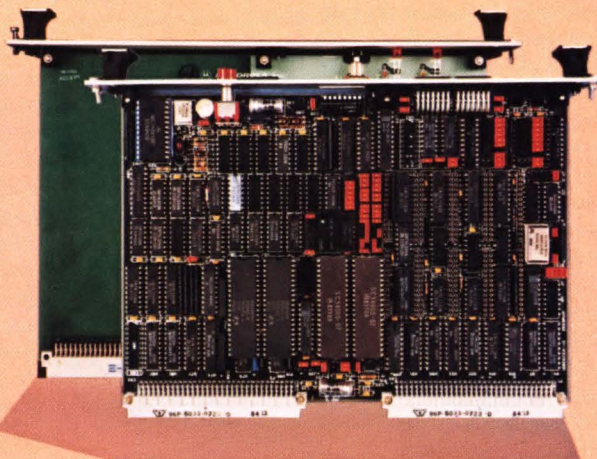
VMESystem Components C



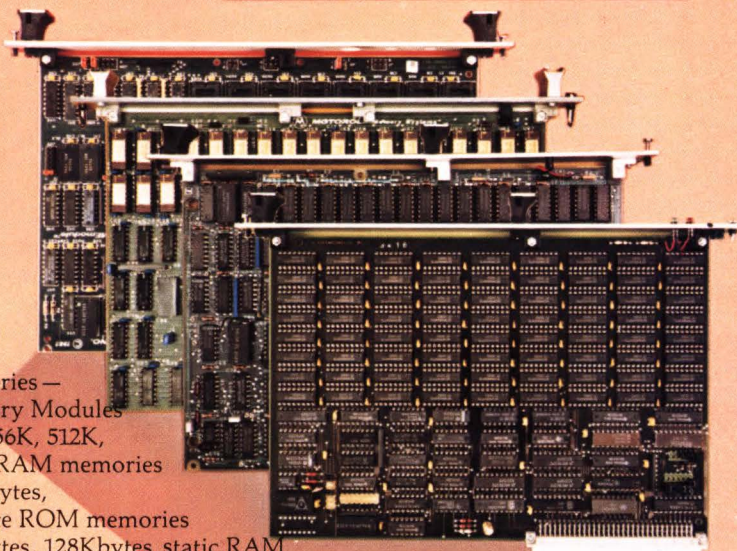
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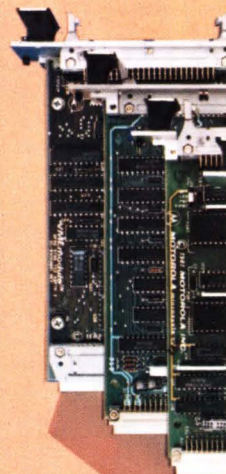
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Readily available cache enriches VMEmodules.

Having cash handy makes good financial sense. Quick access to cache makes good computing sense. With the new VME120 monoboard micro-computer, 4 Kbytes of instruction cache are provided along with a choice of 128 or 512 Kbytes of on-board dual port RAM. The on-board cache memory increases overall system processing speed by allowing faster access and minimizing off-board activity. This is especially important in performance-sensitive applications, such as image processing and high-speed scientific data acquisition.

With an optional 12.5 MHz MC68010 MPU, the VME120 provides throughput of up to 3 million instructions per second.

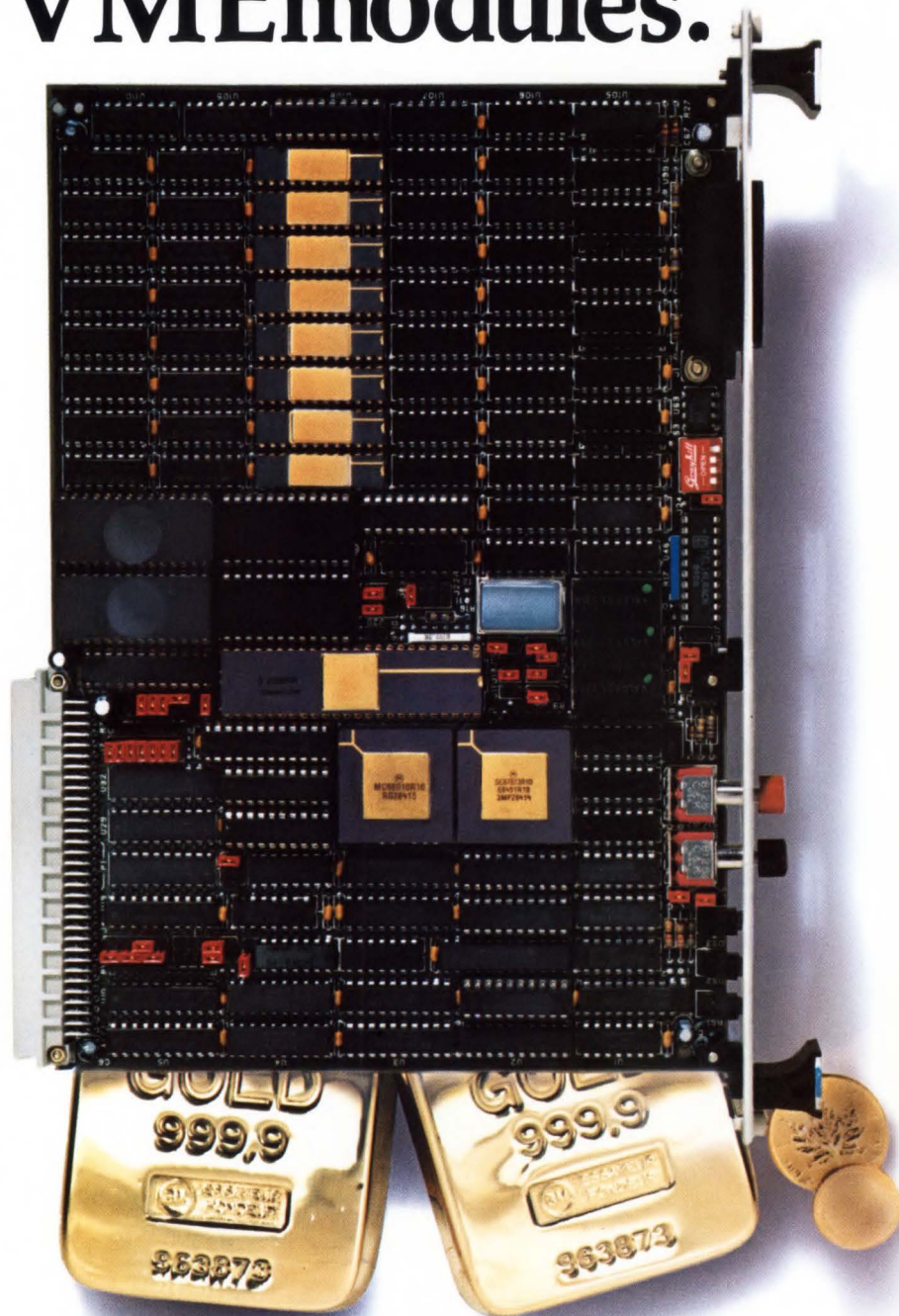
Additional new VMEmodule products allow integration of powerful application systems with a minimum number of system components.

The VME050 system controller may be used with the VME120 processing module to provide global interrupt generator, system clock, serial clock and time-of-day clock functions. It also houses eight 28 pin sockets, two RS-232C serial ports and one parallel port.

The VME320 disk controller is a double-high Eurocard module for adding mass storage capacity to a VMEbus system. It provides high performance DMA data channels between system memory and Winchester hard disk drives and/or floppy disk drives. This disk controller is used in applications having intensive real-time disk I/O or multiprocessing structures to reduce VMEbus traffic and increase system throughput.

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The VME943 chassis provides 9 VMEbus slots and 6 I/O channel slots in the front, with room for 16 I/O channel or 80mm slots provided in the rear. The chassis uses a transverse, mid-chassis 400 watt power supply. It is 19 inches deep and designed for mounting in a standard 19 inch rack.



VMEmodule software support includes VERSAdos, Motorola's real-time, multi-tasking, multi-user operating system that includes M68000 Family macro assemblers, a full screen editor, linker and symbolic debugger.

For efficient software evaluation and debug, VMEbug is one of Motorola's debug/monitor firmware products supporting various processor

modules. VMEbug provides an assembler/disassembler feature, commands to examine or modify memory, and terminal I/O, disk I/O and boot capabilities.

These new boards add additional system building block features to the broadest line of VMEbus compatible boards available.

Check ☐ A for information.

Of special interest...



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- 2 asynchronous ports
- 4 synchronous or asynchronous ports
- all 6 RS-232C or RS-422
- 128/512 Kbyte RAM
- 2 28 pin sockets

VME 050 system controller

- used with VME 115, 120, 128 and 130
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- 2 RS-232C serial ports
- 2 parallel ports
- provides: interrupt handlers
system clock
serial clock, and
time-of-day clock

VME 211 static RAM/ROM

- 16 28 pin sockets
- backed up from +5 standby
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- up to 128 Kbyte SRAM
- mix static RAM and ROM
- selectable access time

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- 1 RS-232C debug port

VME 300 GPIB controller

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VME 316 VMEbus to I/O channel interface

- converts I/O channel interrupts to VME interrupts
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VME 202/222 512K/2M DRAM

VME 203*/223* 512K/2M DRAM with VMXbus

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Winchester/floppy controller

- up to 2 5¼" Winchesters
- up to 4 floppies
- DMA access
- 32 bit ECC code

*To be introduced in 1985.
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VME 128* monoboard microcomputer with cache

- MC68010 (12.5MHz)
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- 1 RS-232C debug port
- triple programmable timer
- VMXbus interface
- uses VME 050 system controller

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- MC68851 PMMU (optional)
- MC68881 co-processor (optional)
- 2 28 pin sockets
- 512 Kbyte dual port RAM
- VMXbus interface
- uses VME 050 system controller

VME 330

Ethernet™ 2.0 LAN controller

- complete transceiver interface
- MC68000 (10MHz)
- LANCE chip and SIA devices
- 128K dynamic RAM
- 32K EPROM
- 1 RS-232C debug port

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You, too, can take high-capability advanced systems to market and be the envy of your industry.

The answer lies in the rich resources of Motorola's M68000 Family of high-performance 8-, 16- and 32-bit microprocessors and system peripheral circuits. Chances are, once you design in the M68000 Family and experience the success that follows, you'll be a family friend for good.

The extensive M68000 Family of compatible, easy-to-use MPUs and peripherals is available from Motorola and the most comprehensive complement of contractual alternate sources.

Data Comm, DMA Control, Local Area Network Control, Parallel, Serial and General Purpose I/O, Memory Management, Bus Control and more are available to help you raise your systems above the competition in a hotly competitive marketplace.

Move data fast.

Moving data around fast with minimal intervention from the processor is the province of the 68440 Dual DMA and the 68450 DMA Controller. The two-channel 68440 is capable of 5 Mbyte/sec transfer and the 68450 offers four independent channels and extensive support for the movement of complex data structures.

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M68000 Family data communications devices link your system efficiently to the outside world, be it terminal, transmission line or another system, and free the processor for other important work in the process.

One of the most popular data comm devices available is the 68661 Enhanced Programmable Communications Interface. It's a universal synchronous/asynchronous chip that interfaces easily to M68000 MPUs and directly to most 8-bit MPUs. Another important available family communications device is the 68681 Dual UART that provides two completely independent full duplex receiver/transmitter channels.

Extensive flexibility is achieved with the 68652 Multi-Protocol Communications Controller. Basic system functions are contributed by the 68901 Multi-Function Peripheral. Other family data comm functions include Intelligent Peripheral Controllers, Polynomial Generator Checker and Parallel Interface/Timer. Additional 68000-compatible data communications parts are available or

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Data-storage device management is the domain of the 68454 Intelligent Multiple Disk Controller. It can control any combination of up to four single- or dual-density floppy and hard disks of various formats. Our 68451 MMU is a seasoned veteran in multi-user, multi-task systems, and now, the requirements of 32-bit demand-paged virtual environments are immediately satisfied by the 68461 Memory Management Controller.

Network and bus control.

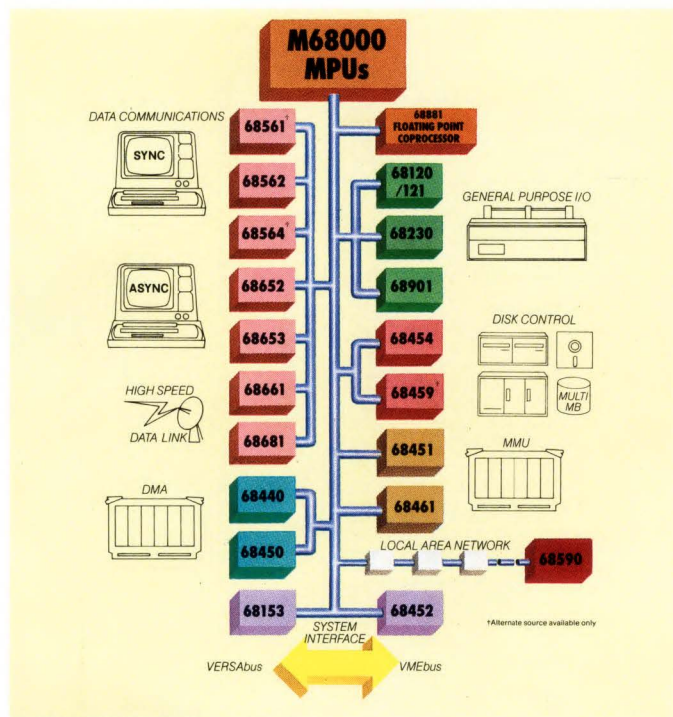
The M68000 Family is growing to meet expanding demands in network and bus control. The 68590 is designed to meet all IEEE Ethernet™ specs for M68000 systems, and a new VME Controller will be added as VMEbus becomes a standard.

Floating point.

A companion processor to the 32-bit 68020 MPU is scheduled for introduction soon as well. The 68881 is designed to support the latest revision of the IEEE specification for floating point high-level calculations. It can also be used with the 16-bit M68000 Family processors.

You can see, now, why M68000 Family systems will make you the envy of your industry. You owe it to yourself and your customers to act now.

Check ☐ C for information. Ethernet is a trademark of Xerox Corp.



☐ ☐ ☐

Think of a DO-41 without leads.

...and you've pictured total flexibility of choice in surface-mount zener diodes.

No one is stronger in zeners than us and you now have easy access to this total capability and sourcing in 1 W surface-mount zeners.

This newest, most sophisticated packaging technology is revolutionizing circuit boards. Cutting cost, increasing density and speeding manufacturing operation, surface-mount is re-shaping boards of the future. And we're leading, not only in zeners but in hundreds of other discrete and IC-packaged types.

We were first with SOTs. And a full line of SOICs. Plus chip carriers.

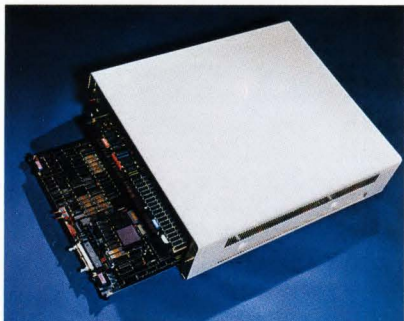
The MLL4728-4764 zener series ranges from 3.3 to 100 V. Tolerance is 10% for the standard version and 5% for the "A" version. It's available in bulk, or in 12mm tape and reel in both T1 and T2 configurations. T1 — Cathode facing sprocket holes. T2 — Anode facing sprocket holes.

Even more practical placement is reflected in the pricing: it's comparable to leaded packages.

Think of them as the right stuff for your PCBs and we'll send you a data sheet and new brochure.

Check ☐ D for information.

Benchmark 20: First to evaluate. First to market.



System integrators thinking about using the new 32-bit MC68020 MPU now have an excellent testbed for system evaluation: Benchmark 20!

This MC68020-based system package provides a variety of hardware and software tools to allow streamlined 32-bit benchmarking, code development and debugging. Packing a lot of power into a small space, the Benchmark 20 system contains a single-board microcomputer with the

MC68020 MPU, plus an auxiliary 1 Megabyte RAM module, all configured with powerful debug/monitor firmware in a 4-slot chassis.

The result? You reduce time-to-market for your new 32-bit system product. Benchmark 20 is configured and ready to use alongside an appropriate software development host to trim your schedule for MC68020 benchmarking and code debugging.

The VM04 VERSAmodule CPU board utilizes the capacity of this new 32-bit performance standard to achieve speeds in the 2-3 million instructions per second (MIPS) category. 4K long words of on-board instruction/data cache reduces off board memory accesses to insure top performance.

The companion VM13 dynamic RAM module provides 1Mbyte of random access memory dual ported with both RAMbus and VERSAbus.

A perfect system mate for the VM04 32-bit monoboard, the VM13 RAM board has error detection and diagnostic capability.

To help you quickly evaluate the MC68020 and the VM04, the Benchmark 20™ system package incorporates the 020bug™ debug/monitor firmware package to allow you to do benchmarking and to debug code. The 020bug resident package allows full speed execution of system and user developed programs operating out of the Benchmark 20 system package. Powerful software and system debug command set allows access to all VM04 I/O, control, and memory facilities plus the full 4 gigabyte direct address range of the VERSAbus system bus.

Benchmark 20, 020bug and VERSAbus are trademarks of Motorola.

Check ☐ E for information.

Turbo-charge operating systems with MC68010 monoboard.

The VERSAmodule line of 16- and 32-bit system components now includes a MC68010-based monoboard just right for hosting today's high-end operating systems including the UNIX™ System V operating system.

The VM03 monoboard utilizes an MC68010 microprocessor running at 10 MHz combined with an MC68451 memory management unit. Your choice of 256Kbytes or 1024Kbytes of on-board dynamic RAM with parity check assures outstanding local high-speed storage needed for "heavyweight" applications in image processing, artificial intelligence and supervisory control.

The optional 1 Mbyte of on-board memory increases operating system efficiency by allowing larger segments of code and data to be accessed, minimizing off-board activity. This performance benefit pays off in applications such as software development where large operating systems are used. An I/O channel interface is also provided for adding off-board resources in incremental amounts.

The VM03 monoboard is complemented by additional new support modules for high-end system applications.

Used for high speed storage in VERSAbus systems, the VM12 is a 4096Kbyte or 1024Kbyte dynamic RAM module with parity. It attains its capacity options and performance using high density HMOS 256K or



64K dynamic RAM chips. The VM12 supports the full 32-bit address of the M68000 family.

For system applications requiring high-capacity rotating mass storage, the VM22 disk controller supports 4 SMD drives and 4 SA400/800 floppy disk drives. Data transfer speeds up to 3 Mbytes/sec between system memory and hard disk drives and floppy disk drives are maintained by the direct memory access feature of the disk controller.

The VERSAmodule line is supported by both of Motorola's M68000 operating systems: the VERSAdos operating system for real-time appli-

cations, and the SYSTEM V/68 operating system where a UNIX™ operating system environment is desired. Full operating system support, including VERSAdos real-time device drivers, are available now for the MC68010-based VM03 monoboard.

Add to all this Motorola's expertise, proven products, training and service support and you can understand why VERSAmodule system components continue to be your best choice for the highest performance board-level applications.

UNIX is a trademark of AT&T Bell Laboratories. SYSTEM V/68 is a trademark of Motorola. Check ☐ F for information.



Time and cost saving E²PROM operates from single +5V supply.



The MCM2833 is a 32K E²PROM, Electrically Erasable Programmable Read Only Memory, that can save time and money in many data-handling applications. And, it operates from a single +5V supply.

Where non-volatile memory and in-system programming are required

the MCM2833 fits perfectly, with in-system erase and reprogram capability that can cut costs and conserve time.

In addition, the MCM2833 derives outstanding data retention and endurance from the technologically advanced Motorola floating-gate

electron tunneling MOS, FETMOS, fabrication. Data integrity is 10 years, and data is protected during power up and power down.

Fast access and low-power operation are characteristic. Maximum standby power dissipation is 35 mW, and max. active P_D is 125 mW. Speeds of 150 and 200 ns are available. Byte erase or write is 9 ms.

A choice of erase modes, bulk, byte, row or column, helps optimize system erase/write time and makes the MCM2833 easier to use. Latched addresses, data and controls create microprocessor-friendly operation, allowing the MPU to work on other jobs while the MCM2833 is erasing or programming.

Not the least of the MCM2833 E²PROM's attractiveness is its relationship as a member of Motorola's industry-standard byte-wide non-volatile memory family, providing opportunities for cost-effective density upgrades.

Engineering samples are available. Check ☐ G for information.

One MC1377P RGB encoder generates broadcast color, pure and simple.

Simple things are best, and nowhere is this more true than video color encoding with the unique new MC1377P.

Just one 18-pin DIP does it all. With the addition of only a crystal and a few external resistors you have what used to be a boardfull of time- and cost-consuming discretes and/or ICs.

Superior phase linearity and well-controlled color vectors provide the purity of color found only in complex, high-level studio broadcast equipment. And you can design the extraordinary performance features of the monolithic MC1377P into a wide variety of color cameras, graphics computers and teletext generators for about one-tenth the cost of the "maze" approach.

A major system simplification leap.

The MC1377 combines red, green and blue video information into a composite signal in either NTSC (U.S.) or PAL (Europe) formats. Used with the MC1374 color-modulated oscillator and a few components to generate a modulated RF carrier, you've actually got a miniature TV station.

Design it with the TDA3300 decoder family and you can separate, modify



or enhance R, G or B for a rainbow of special effects. Simply, easily, economically.

The MC1377P contains a sub-carrier oscillator, voltage controlled 90° phase shifter, two double-sideband modulators, RGB input matrices and blanking level clamps. Its oscillator can be used as the "master" in a system, or it can be driven by an external source. R, G and B inputs are ac-coupled to simplify interfacing. A 1.0 V p-p input level produces full saturation of colors in the output.

The only other input required is a composite sync signal, which is

combined with the encoded video to produce the composite video output. The sync is also used to trigger the generation of color (burst) reference. Both chroma and luma signals are "looped out" of the chip to permit tailoring bandwidth and delay to the designer's taste. This permits very elegant applications as well as very simple ones.

The MC1377P production line is running. Price, in 100-999 quantities, is in focus at only \$2.35.

Check ☐ H for information.

Floodgates open for VME/10 software.



Industry standard operating systems such as the UNIX™ System V allow greater than ever software portability for users of Motorola's VME/10 OEM Microcomputer system.

Software support within the UNIX™-derived SYSTEM V/68 operating system includes 400-plus utilities plus an optional optimizing Pascal compiler, M68000 macroassembler, and facilities to store and update all versions of a source code module.

The SYSTEM V/68 operating system comes with full screen editors and spelling checkers for full screen text processing. The "mm" memorandum macrocommands automatically format standard footnotes; number pages, lists, and paragraphs; and produce headings and footings.

Additional application software availability will grow as agreements between Motorola and Digital Research Inc. bear fruit in coming months. These DRI agreements call for a total of 25 software packages for the M68000 Family in SYSTEM V/68, Concurrent DOS™-68K and CP/M® 68K. Nine of the packages to be developed will be supported under SYSTEM V/68.

Concurrent DOS-68K, which is written in C language, is a multi-

tasking operating system with windowing, LAN support and graphics. It is designed for multiuser or single user microcomputers and includes an IBM PC-DOS™ mode. This means application programs written in standard high-level languages on the IBM PC can be re-compiled on Concurrent DOS-68K without any modification. DRI is developing a system of com-

pilars for a range of machines that operate under SYSTEM V/68, CP/M-68K, Concurrent CP/M and Concurrent DOS-68K.

CP/M is one of the most popular microcomputer operating systems for which hundreds of applications have been written.

Application programs written in any of the covered languages—Pascal, FORTRAN, C, BASIC and PL/I—should then run on any computer in the M68000 Family under CP/M-68K, Concurrent DOS-68K or SYSTEM V/68.

UNIX is a trademark of AT&T Bell Laboratories.

CP/M is a registered trademark of Digital Research Inc.

Concurrent DOS is a trademark of Digital Research Inc.

IBM PC and PC-DOS are trademarks of IBM.

Check ☐ L for information.

☐ ☐ ☐

Sharpen Macrocell Array design skills.

Two new Macrocell Array design manuals are now available from Motorola to assist you in understanding and easily generating optimized semi-custom ECL application specific ICs.

The MCA2500ECL Macrocell Array Design Manual is all new. It covers just about everything a trained MCA designer needs to carry out the design. There's a review of the Macrocell Array concept and technology, and a run-down of MCA features supplemented by an explanation of cell types.

Logic design considerations and performance guidelines are examined in detail. CAD layout, array option development and various hardware subjects are reviewed. A large section is devoted to the Macrocell Library and MCA2500ECL specification plus individual cell descriptions.

The MCA2500ECL Design Manual is available for \$3.50. Order BR165.

MCA600ECL and MCA1200 ECL are Macrocell Arrays similarly served by the eagerly awaited revised design manual, BR107/D R1. This is an updated replacement for a preliminary edition. BR107/DR1 also is available for \$3.50.

Footnote: Check ☐ J to order BR165.

Check ☐ K to order BR107/D R1.

Send check or money order to cover the correct amount of your purchase @ \$3.50 per design manual copy.

Languages to be available on the VME/10

Under CP/M 68K

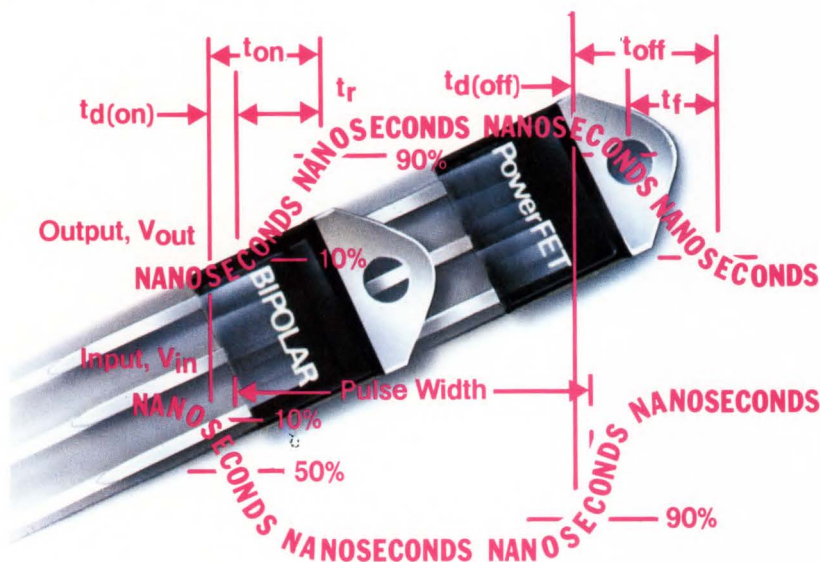
Digital Research C
Pascal MT+
CBasic Compiler

Under Concurrent DOS-68K and SYSTEM V/68:

Digital Research C
Pascal MT+
CBasic Compiler
FORTRAN 77
BASIC Interpreter
GSX Graphics Software



Fastest, highest-voltage bipolar pushes powerFETs.



It may not quite catch them, but it's so close you can virtually ignore the difference in speed.

The complete new MJH16000 series of 850 to 1,500 V Switchmode III bipolar power devices switches big loads in nanoseconds — about 10 times faster than other bipolars — just like power MOSFETs, without sacrificing ruggedness.

Ideally suited for high-frequency inductive switching where high-temperature RBSOA is a major concern, these 5, 8 and 15 A units feature a higher periphery-to-area ratio and hollow emitter structuring to give the designer a needed edge in ruggedness and speed and improve design efficiency and compactness.

The TO-218 packaged units are suitable for both U.S. and European power supply designs. Unique lead-spacing and package dimension features allow regulatory agency approval in both domains enabling you to design one supply accepted for both markets.

Use the 450 V units for line-operated half-bridge, full-bridge and push-pull configurations and the higher-voltage types for single transistor flyback and forward converter topologies.

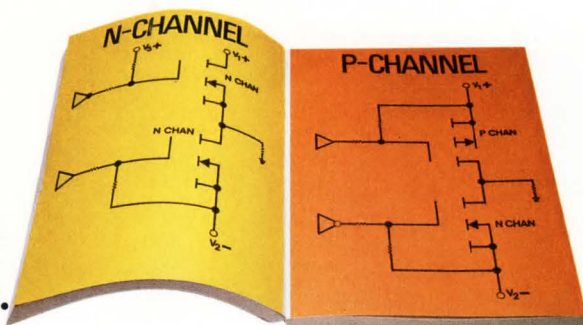
Additionally-packaged in TO-204 (TO-3), the series is 100-uped from \$1.58 to \$6.57...molehill pricing for mountains of performance.

Check ☐ M for information.

P-Channel powerFETs add new chapter to drive circuit applications.

When you want to cut power supply or charge pump requirements to your power MOSFET in bridge cascode or push-pull applications, go Motorola P-Channel.

This extension of the MTM/MTP8PO8, -2P45 family is available from Motorola to make your design job simpler and more cost-effective.



A simple load that requires only one-side grounding to a negative bus can easily be switched with P-Channel technology eliminating extra, expensive componentry. V_{gs} , which biases gate above source to hold the MOSFET on, is no longer necessary.

Schottkys extend efficiency to 12 V.

The world's best Schottky rectifier process introduces an expanded Schottky rectifier voltage — 60 V.

You now have the option of designing 12 V supplies with Motorola devices to improve efficiency and reduce recovery noise associated with other rectifier types.

Packaged in TO-220, the 10 A MBR1060 Schottky offers 0.7 V_F and less than 6% power loss, or 94% efficiency, at 120 W P_O . Ordinarily, you'd lose twice that with a slower rectifier, up to now your only choice for higher output power applications.

With the MBR1060, you gain the same advantages for 12 V supplies as you've enjoyed with Schottkys in 5 V supplies.

And it's just \$1.80, 100-up.

Cool by nature, calm by comparison, Motorola's broad TO-220 Schottkys exhibit lowest correlation of temperature rise vs. forward drop of any other types. You gain more, lose less with Motorola...up to 175°C operating temperature.

Add a guaranteed avalanche surge, built-in PN guard rings, freedom from trace anomalies and virtually perfect working barrier processes and you've got the highest quality going in nanosecond rectification.

Discipline power with efficiency: Motorola Schottkys.

Check ☐ N for information.

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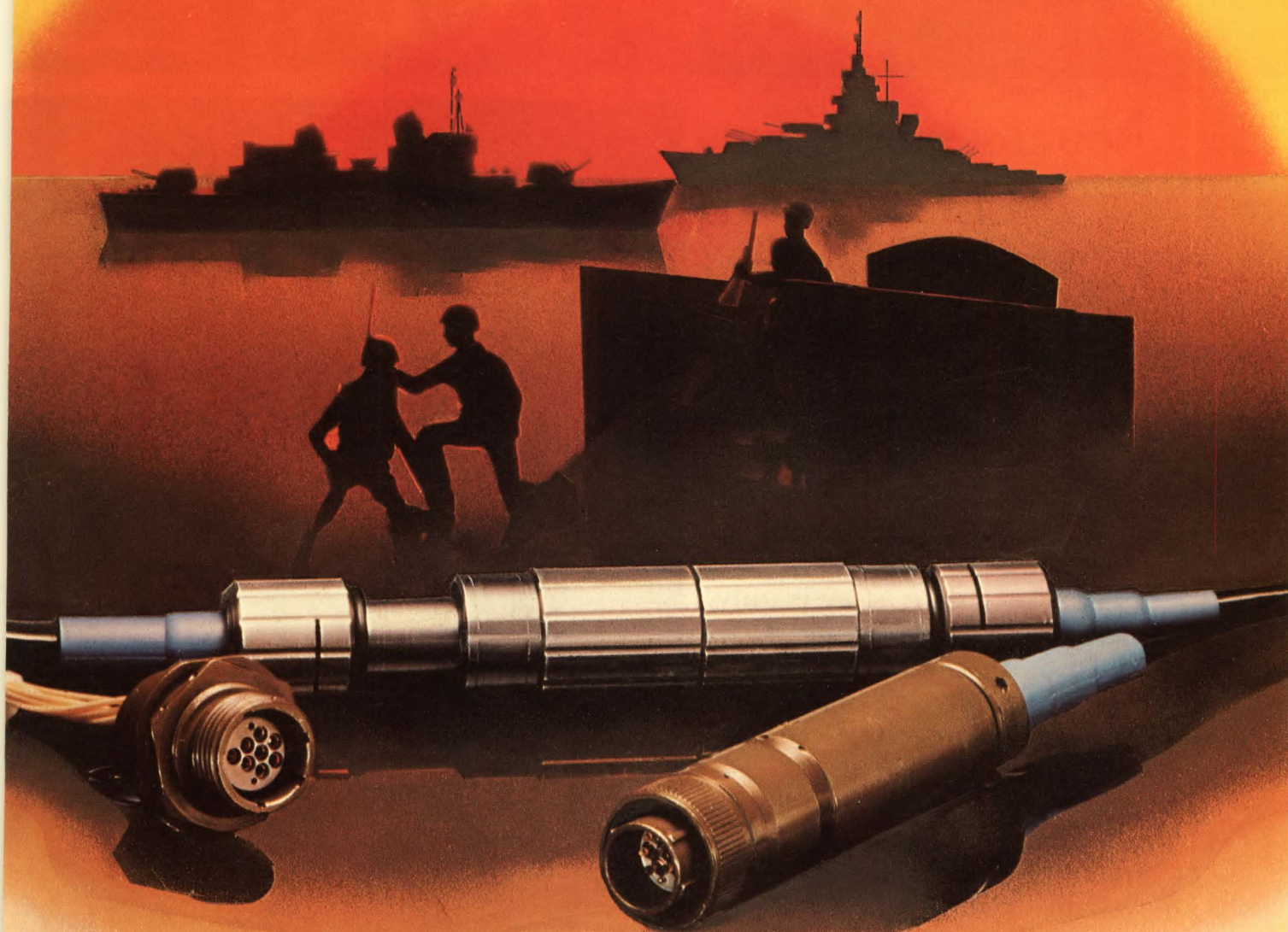
The new nanosecond-switching series is fabricated utilizing the same N-Channel TMOS™ III process that results in optimized cell density and cost factors. It's the best silicon utilization process in the industry and offers you the ultimate design advantage: price.

There's no sacrifice in reliability or performance. AOQ levels measure out at less than 100 ppm, guaranteed. And $r_{DS(on)}$ as low as 0.1Ω is available for very high efficiency operation.

Prices for the 50 to 500 V, 2 to 25 A family are \$2.20 to \$21.00, 100-999 in hermetic, TO-204 (TO-3) or low-cost TO-218 and TO-220 plastic packaging.

We'll send you Designers™ data sheets and a new TMOS brochure.

Check ☐ P for information.



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So if you need the toughest fiber optic connectors in the world, contact your Hughes representative or phone Jack Maranto at 714-660-5759. Or write Hughes Aircraft Company, Connecting Devices Division, 17150 Von Karman Avenue, Irvine, CA 92714. In Europe: Hughes Microelectronics, Ltd., Clive House, 12/18 Queens Road, Weybridge, Surrey KT13 9XD, England.

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Of course, a gate array is only as good as the people behind it. And at NEC, we have some of the best support engineers. Ready to help you take your design from start to finish.

With easy-to-use CAD tools. And sophisticated software capable of simulating up to 20,000 gates. All available at our 18 customer design centers, worldwide.

As for quality, we offer 100% burn-in, standard. At no extra cost. And you won't have to wait long to get it. Our turnaround is as quick as 8 weeks.

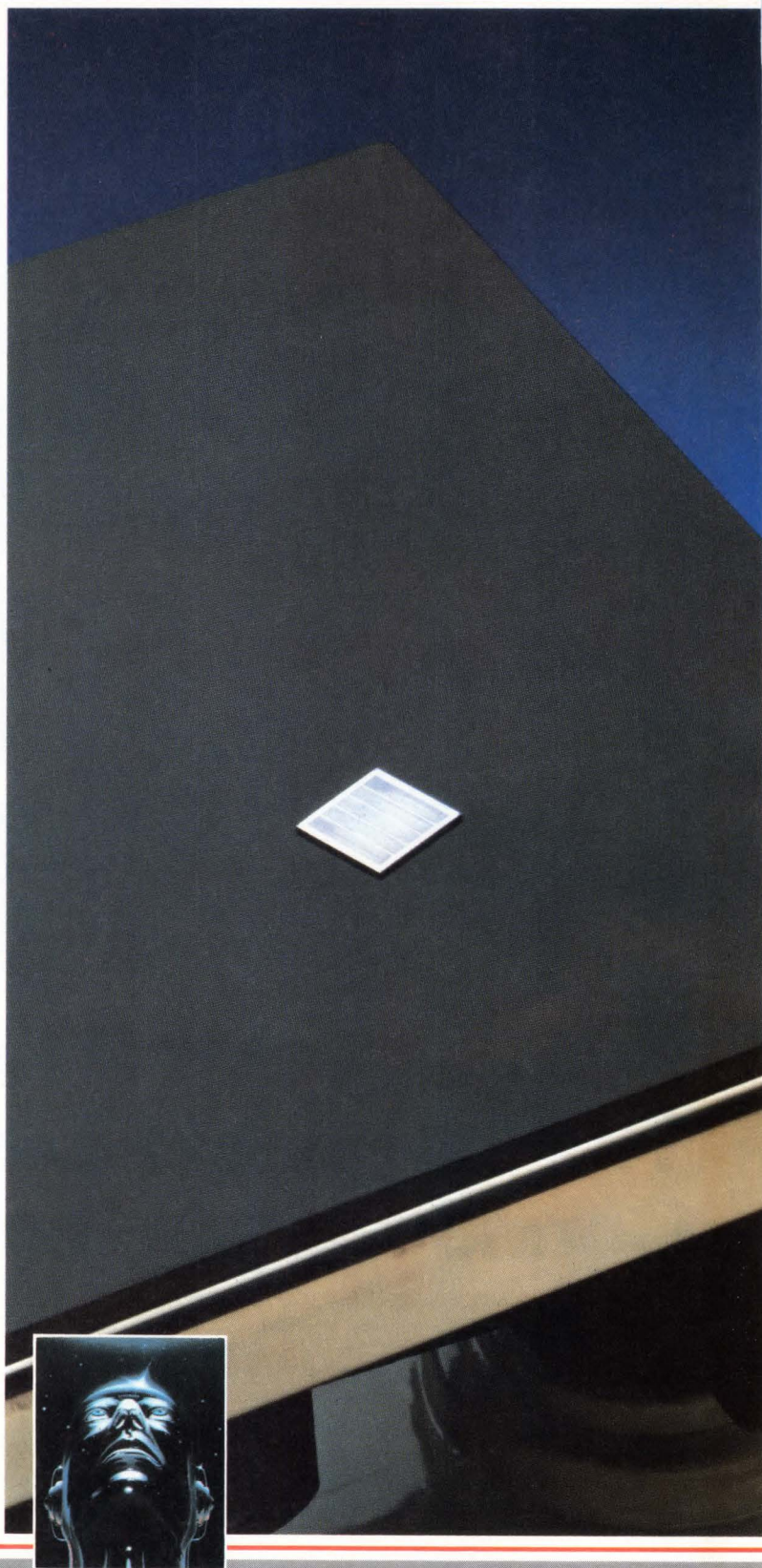
So next time you need a gate array, weigh your alternatives. Then call NEC.

WE'RE TAKING ON THE FUTURE.

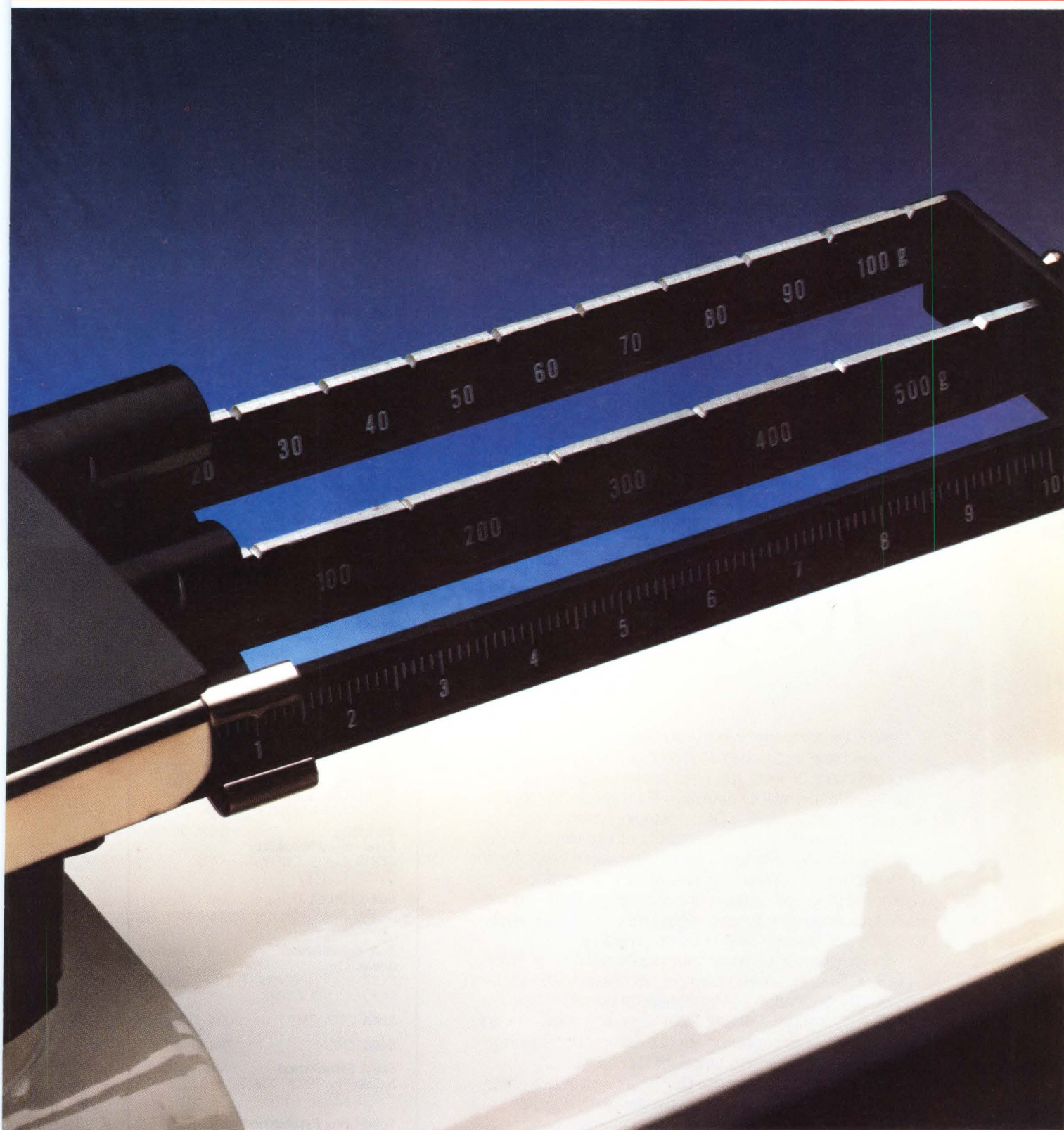
For the fastest response to your questions or for more detailed information, call us TOLL FREE at 1-800-556-1234, ext. 188. In California, call 1-800-441-2345, ext. 188.

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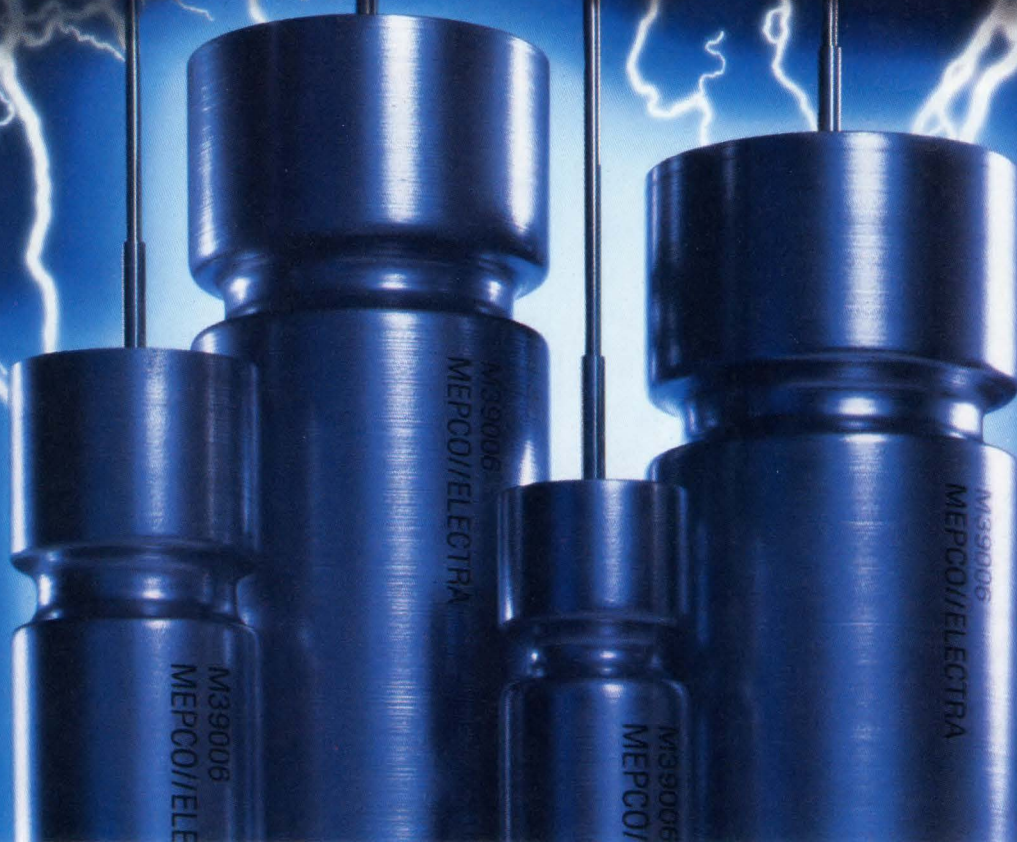


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Why be a 'captive' when you can be selective? Now you have a choice in 'R' level CLR79 capacitors... Mepco/Electra. 'R' level approval, per MIL-C-39006/22, is now effective on all four case sizes (T1 through T4) and all voltages (6 through 125 VDC)...including characteristic 'H'.

A leader in new generation technology, Mepco/Electra offers the broadest Mil Spec Qualified tantalum capacitor line in the industry - each product backed by an advanced, rigorous testing and quality control program. High-volume manufacturing capacity gives Mepco/Electra the capability to supply the quantity you need on-schedule.

So why be tied to single-source fulfillment for 'R' level CLR79's? Tap the proven resources, technological innovation and quality dedication of Mepco/Electra by calling our West Palm Beach facility (305) 842-3201 regarding solid, wet slug and chip tantalum capacitors, or our Columbia, SC facility (803) 772-2500 regarding tantalum foil capacitors.

For complete data on the CLR79, as well as our entire line, send for the 1984 edition of the Resistor/Capacitor Data Book. Mepco/Electra, Corporate Headquarters, Columbia Rd., Morristown, NJ 07960 (201) 539-2000. TWX 710/986/7437.

Tantalum Capacitor Standard MIL Specification Approvals

Wet Slug CL14, CL16-CL18, CL55, CL64-CL67	MIL-C-3965
Wet Slug, Established Reliability CLR10, CLR14, CLR17, CLR65, CLR79	MIL-C-39006
Foil, CL20-CL23, CL30-CL33, CL51- CL54, CL70-CL73	MIL-C-3965
Foil, Established Reliability CLR25, CLR27, CLR35, CLR37, CLR71, CLR73	MIL-C-39006
Solid, CS12, CS13	MIL-C-26655
Solid, CX05	MIL-C-49137
Solid, Established Reliability CSR09, CSR13, CSR23, CSR33, CSR91	MIL-C-39003
Solid Chip, Established Reliability CWR06	MIL-C-55365

Buried oxide wall blocks smearing, blooming on solid-state imager

Burying an oxide wall in an imager lengthens the carrier path, thus holding smearing and blooming in check.

Adding a buried oxide wall to a solid-state color imager cuts back significantly on the smearing and blooming that commonly plague these devices. The wall alters the characteristics of the parasitic transistors that contribute to both problems. Smearing and blooming themselves are caused by carriers traveling between adjoining photodiodes in a photosensitive array.

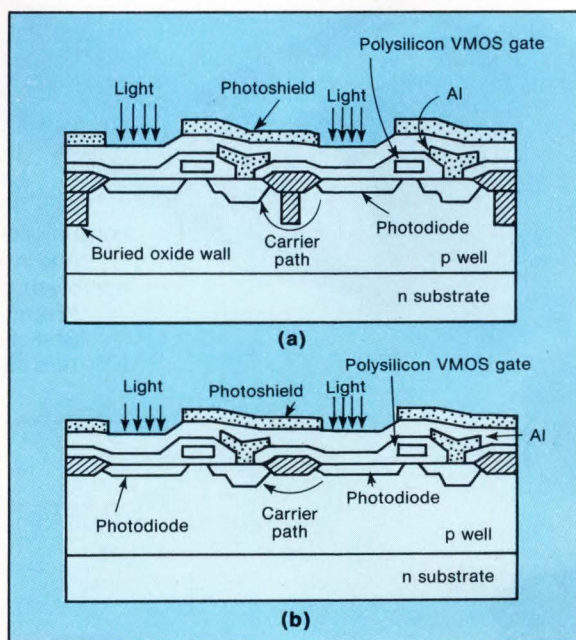
Scientists from the LSI Research and Development Laboratory of Mitsubishi Electric Corp. (Hyogo, Japan) have suppressed the smearing that is the result of the carrier path under the imager's field oxide. The resultant experimental array comprises 384 by 485 photodiodes and employs a monolithic complementary color filter. The buried wall increases the base length of the parasitic npn transistor formed between adjacent photosensitive elements (see the figure). Lengthening the

carrier path decreases the leakage current, consequently reducing smearing and blooming.

To create the buried oxide wall within the imager's MOS structure, the substrate is first oxidized and then etched,

leaving the oxide barriers. Next, a thin epitaxial layer is grown, approximately the same width or slightly thicker than the oxide walls. To prevent grown-in defects along the buried wall, a selective oxidation process is used to flare out its top. The balance of the circuit is fabricated with conventional NMOS processing.

In addition, smearing and blooming were further reduced in the array with a two-line addressing scheme. By addressing two lines simultaneously (as opposed to scanning rows or columns of adjacent pixels while holding one line active) the effective leakage current is further reduced. □



A buried oxide wall effectively lengthens the base of the parasitic npn transistor (carrier path) formed between adjoining elements in an imager (a). In contrast, a conventional device has a shorter carrier path, thus exhibiting greater smearing and blooming (b).

Warren Andrews

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INMOS	yes	yes	yes	no	1.66:1	yes

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INTERNATIONAL MEETINGS

Conference on Computer-Aided Engineering, Dec. 10-12. University of Warwick, Coventry, England. IEEE Conference Services Department, Savoy Place, London WC2R 0BL; (01) 240 1871.

Fifth Generation and Supercomputers, Dec. 11-13. Rotterdam, the Netherlands. Prof. R. P. van de Riet, Free University, Amsterdam, the Netherlands.

Cadcam International Show, Jan. 8-10. National Exhibition Centre, Birmingham, England. Peter Walker or Landy Hashimi, PWA, 32 Fitzroy Square, London W1P 5HH; (01) 388-9871.

Micro-Computer '85, Jan. 29-Feb. 3. Frankfurt, West Germany. Philippe Hans, German American Chamber of Commerce, 666 5th Ave., New York, N.Y. 10103; (212) 974-8856.

Middle East Electricity and Electronics Exhibition, Feb. 2-6. Jeddah Expo Center, Kingdom of Saudi Arabia. Len Bennett, Logistics, 237 Park Ave., 21st floor, New York, N.Y. 10017; (212) 551-3530.

AFIPS-Asia '84, Feb. 14-March 2. m.v. World Wide Expo, Tokyo, Osaka, Kitakyushu, Taipei, Hong Kong and Singapore. AFIPS, 1899 Preston White Drive, Reston, Va. 22091; (703) 620-8926.

Autotech Hong Kong '85, March 7-8. Hong Kong. Autotech Hong Kong '85, Hong Kong Productivity Center, 12th floor, World Commerce Center, 11 Canton Road, Tsimshatsui, Hong Kong; 3-7235656.

Componentes Electronicos '85, March 12-15. Mexico City, Mexico, March 19-22, Guadalajara, Jal., Mexico. Raquel Polo, United States Trade Center, Liverpool 31 Col., Juárez 06600, Mexico, D.F.; or PO Box 3087, Laredo, Texas 73044.

The Scottish Computer Show and Conference, March 12-14. Anderston Exhibition Centre, Albany Hotel and Holiday Inn Hotel, Glasgow, Scotland. Cahners Exhibitions Ltd., Chatsworth House, 59 London Road, Twickenham, London TW1 3SZ, England; (01) 891-5051.

China Tronic '85, March 14-19. Tianjin Exhibition Centre, Tianjin, Peoples' Republic of China. Asdale Exhibition Services, 109-111 Gloucester Road, 21st floor, Wanchai, Hong Kong; 5-8920511.

Comtel '85, March 18-20. Infomart, Dallas, Texas. Comtel '85, International Computer & Telecommunications Conference, 5080 Spectrum Drive, Suite 707E, Box 17, Dallas, Texas 75248; (214) 631-6482.

Automatic Testing and Test Measurement '85, March 19-21. Rhein-Main-Halle, Wiesbaden, West Germany. Network Events Ltd., Printers Mews, Market Hill, Buckingham, MK18 1JX, England; (0280) 815226.

IEEE Infocom '85, March 25-28. Washington, D.C. Celia L. Desmond, IEEE Infocom '85, Room 1855, 160 Elgin St., Ottawa, Ont., Canada K1G 3J4; (613) 239-4510.

Bit '85 Computer Show and Conference, March 26-29. National Exhibition Centre, Birmingham, England. Cahners Exhibitions Ltd., Chatsworth House, 59 London Road, Twickenham, London TW1 3SZ, England; (01) 891-5051.

Comdex In Japan, March 26-28. Tokyo International Trade Center, Tokyo, Japan. Milton Berns, The Interface Group Inc., 300 First Ave., Needham, Mass. 02194; (617) 449-6600.

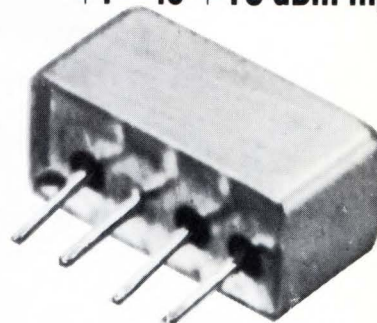
32nd International Electronics, Energy and Aerospace Exhibition (Riena), March 26-31. Rome, Italy. Riena, Via Crescenzo 9, 00193 Rome, Italy; (06) 6569343/4/5.

Internecon/Semiconductor International, March 27-30. Korea Exhibition Center (Koex), Seoul, Korea. Cahners Exposition Group, 7315 Wisconsin Ave., PO Box 7007, Washington, D.C. 20088; (301) 657-3090.

Electronics and Electrical Engineering Exhibition, April 17-24. Hanover, West Germany. Hanover Fairs, PO Box 338, Whitehouse, N.J. 08888; (800) 526-5978 or (201) 534-9044.

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OUTPUT	2-1000		
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100-300 MHz		13.5	15.5
300-500 MHz		14.0	16.5
Spurious Harmonic Output, dB			
		TYP.	MIN.
2-200 MHz F1		-40	-30
F3		-50	-40
200-600 MHz F1		-25	-20
F3		-40	-30
600-1000 MHz F1		-20	-15
F3		-30	-25

For complete specifications and performance curves refer to the 1980-1981 Microwaves Product Data Directory, the Goldbook or EEM.

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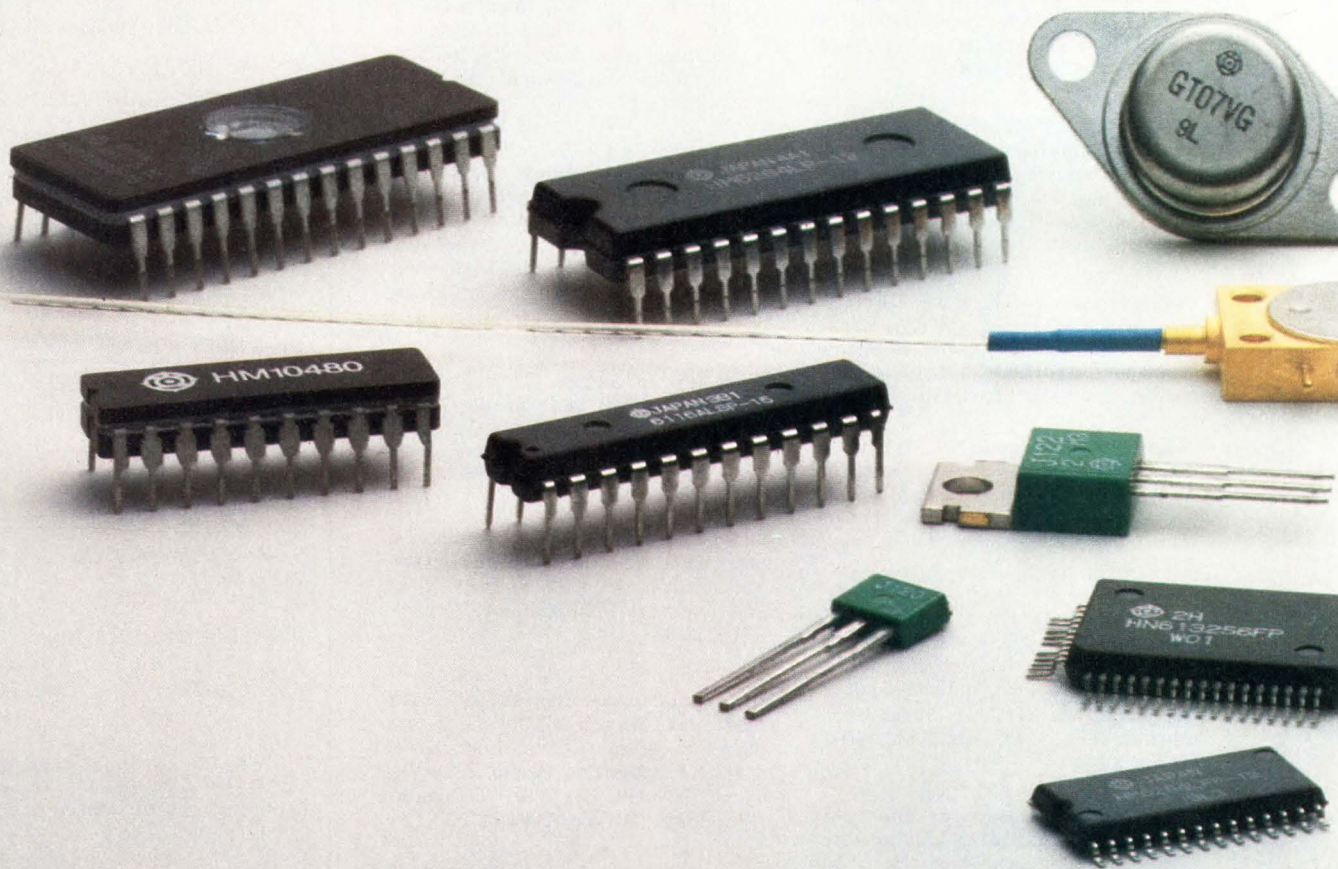
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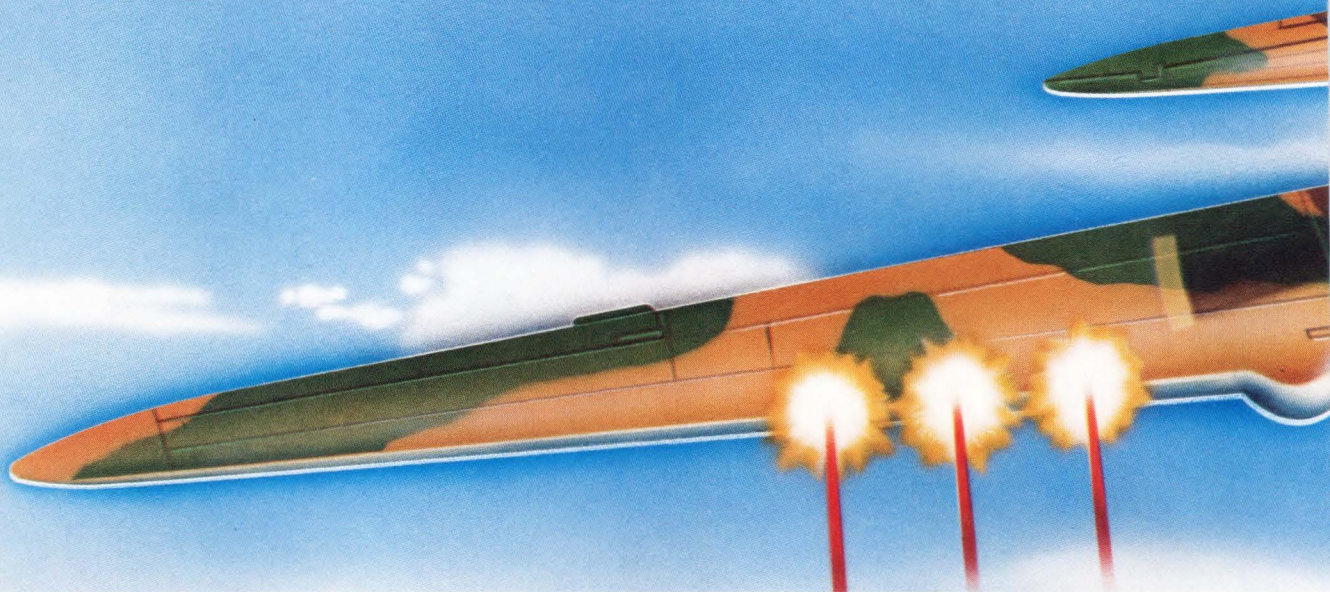


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Realism for your new entertainment



As an entertainment system designer, you know that today's electronics technology permits the generation of CRT-displayed graphics with all the fidelity of a first-quality color motion picture; but until now, not at a price economically feasible for low- and medium-priced entertainment equipment.

High-quality graphics generators have required a stack of printed circuit boards densely packed with SSI/MSI integrated circuits at a cost well beyond sensible budgets for low-cost microcomputer systems. This has caused the majority of graphics displays for popularly-priced entertainment systems to suffer from limited resolution and color selectivity.

New high-quality graphics at a remarkably low cost.

Entertainment systems can be vastly improved now with design-in support and low-cost technologies from Motorola. For colorful, high-resolution graphics in home video and computer games where realistic computer animation is needed, there's Motorola's cost-effective Raster Memory System (RMS). This available-under-\$20 in-production-volume chip set at last makes

professional, quality graphics affordable for your next entertainment system.

Using only two chips, the RMS, under MPU control, converts a graphics program stored in memory into the complex video stream that can produce high-quality displays on the CRT. At an astonishingly low cost. No longer is expensive static display RAM needed. The RMS utilizes system memory comprised of industry-standard DRAM with capacities ranging from 16K to 1M bytes.

With the RMS you can select 32 colors from a universe of 4096 shades to use on a virtual accommodating and smooth scrolling screen.

With the advent of the RMS, graphics quality is now primarily dependent on the sophistication of the software, the amount of memory available and the power of the MPU.

A range of MPUs for every entertainment application.

The RMS chip is designed to operate with a wide range of processors including three of Motorola's powerful MPUs: the 8-bit MC6809, the 8/16-bit MC68008 and the 16/32-bit MC68000.

Motorola's MC6809 MPU has the most complete set of addressing modes available on any 8-bit microprocessor today and

interfaces with over fifty M6800 peripherals. In addition, you're never locked into a specific design with an upward source-code compatible instruction set.

The MC68008 MPU allows the design of cost-effective systems using 8-bit data buses while providing the system throughput benefits of a 32-bit microprocessor architecture. The performance of the MC68008 is greater than any 8-bit microprocessor and superior even to several 16-bit microprocessors.

The industry-leading MC68000 is a fully-implemented 16-bit microprocessor with 32-bit registers, a rich instruction set and versatile addressing modes.

With this line of compatible processors, you'll satisfy all the price/performance tradeoffs in your design requirements.

Modulators and encoders give the big picture.

For supplying signals to color monitors, Motorola supplies a full line of modulators and industry-standard encoder circuits.

The MC1374 is a TV modulator circuit that packs an FM audio modulator, sound carrier oscillator, RF oscillator, and RF dual input modulator all on one low cost chip. It is designed to generate a TV signal

21-6274.

design. Call now for design-in support.



from both audio and video inputs. The MC1374's wide dynamic range and low distortion make it particularly well-suited for applications such as video tape recorders, video disc players, TV games and subscription decoders.

The MC1377 is a color television RGB-to-PAL/NTSC encoder used to generate a composite TV signal from baseband red, blue, green and sync inputs. It is ideal for encoding signals from color cameras and graphics generators.

Opening new markets with AM stereo.

Radio designers are noting the significant advantages AM stereo has over FM in range of coverage and fade resistance.

Motorola's CQUAM® (Compatible Quadrature Amplitude Modulation) AM stereo decoder is a complete one-chip full-feature AM stereo decoding and pilot detection system. It employs full-wave envelope signal detection at all times for the L+R signal, and decodes L-R signals only in the presence of a valid stereo transmission. The MC13020P needs no adjustments, uses no coils and has few peripheral components.

In the absence of a good stereo signal, CQUAM® produces an undegraded mon-

aural output for existing radios. When both channels are modulated the noise increase in stereo is a maximum of 3.0 dB . . . even less on program material.

Years of refinement have made Motorola's CQUAM® the leading contender in the race for a "world standard" in AM stereo systems. Even with four FCC approved competitors, Motorola's CQUAM® has captured more than 140 new AM stereo stations this year and leads in production with over nine major manufacturers.

Talk engineer to engineer.

Motorola has tripled the number of application engineers it has throughout the U.S. and Canada.

Each has the expertise in emerging semiconductor technologies that can electrify your new entertainment design ideas. Call 1-800-521-6274 and discuss your applications. Any time between 9 A.M. East Coast and 5 P.M. West Coast time, weekdays. Toll free. Talk to our specialists. They'll discuss your applications and get you in touch with a field application engineer who'll in person describe in depth

The RMS system can simultaneously display any 32 colors from its palette of 4096 colors in adjacent pixels. The above illustration is a continuous tone artist's representation.

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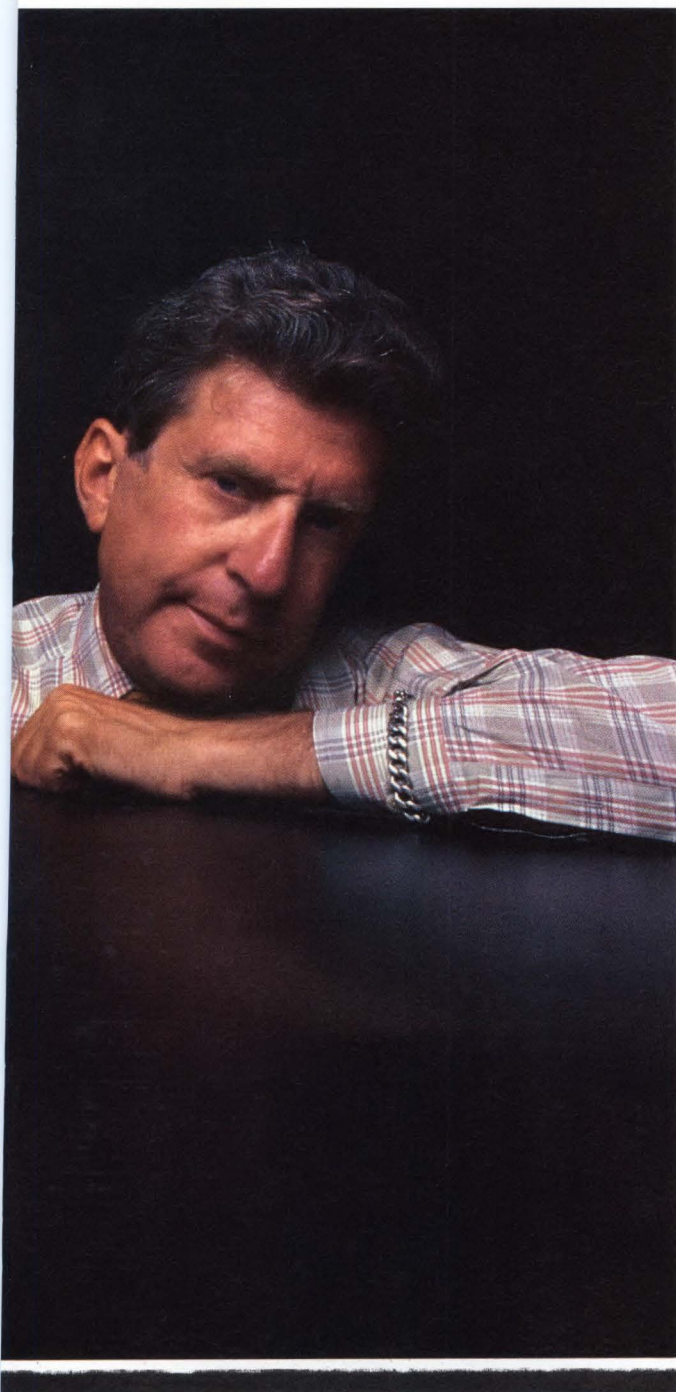


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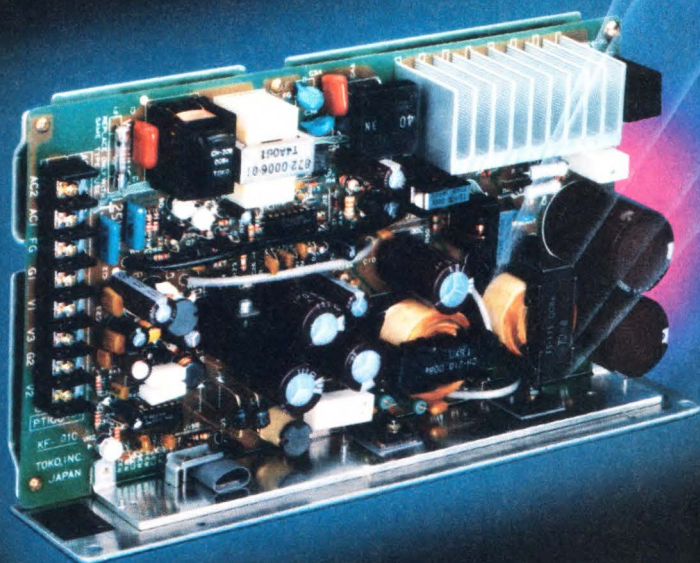
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When you select a switching power supply, your product's reliability and performance are on the line. Will the sample you approve be typical of OEM production? It will if you evaluate Toko. We reinvented the transformer to assure a consistent level of performance not possible with conventional transformer designs.

Unlike ordinary wire-wound transformers, Toko transformers are based on a better idea — inductive copper strips interwound with Mylar* insulation over a high-efficiency iron core. This design** significantly tightens performance tolerance limits and improves transformer reliability. The chances of a shorted winding are greatly reduced and the probability of an open winding is virtually eliminated.

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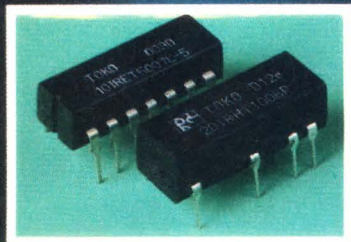


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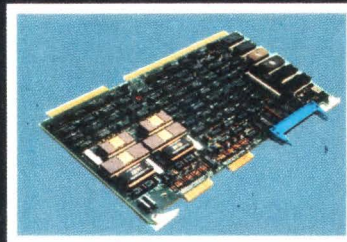
Toko America is the U.S. subsidiary of Toko, Inc., a large Japanese manufacturer of a broad range of high quality electronic products. Here's a sampling...



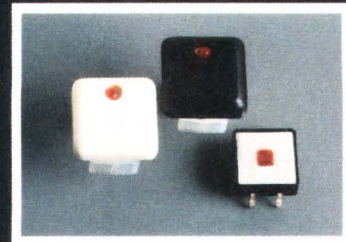
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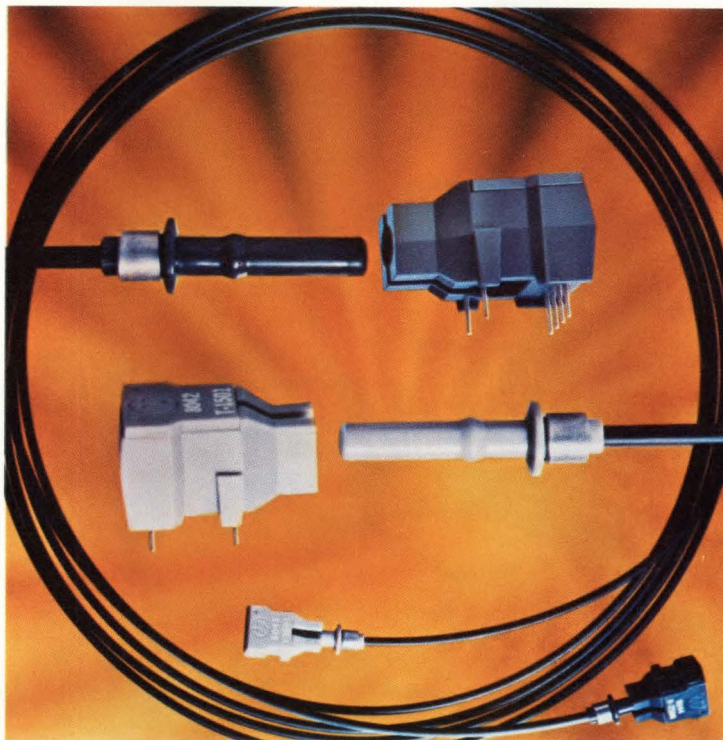
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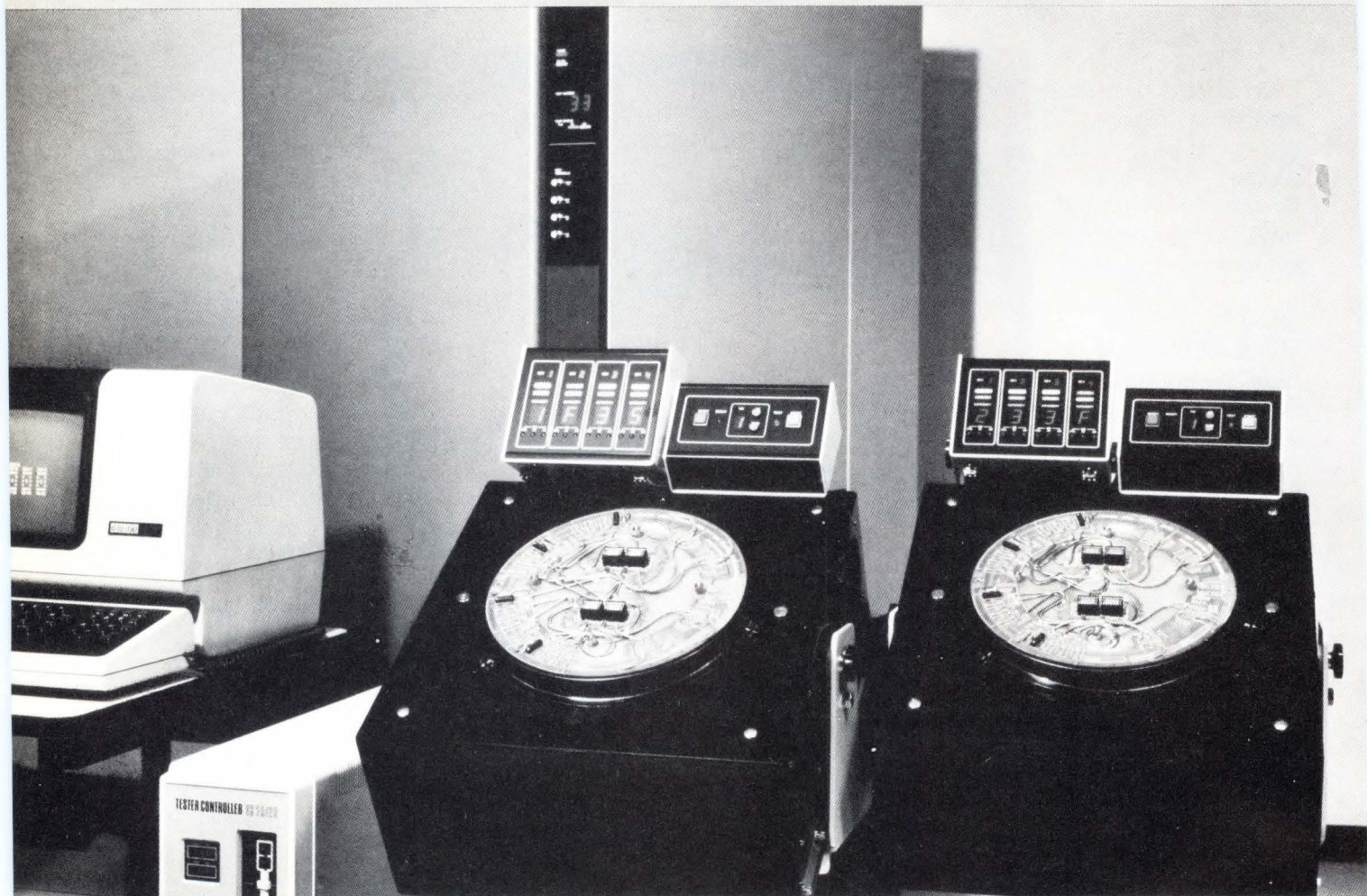
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HP: The right choices for value in fiber optics.



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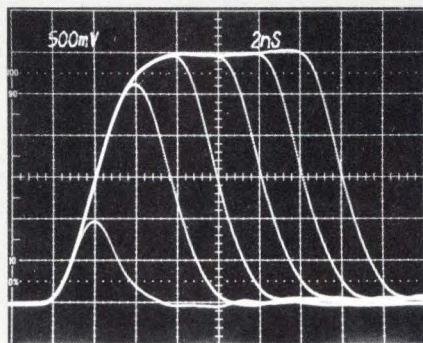
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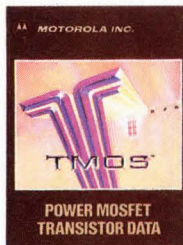
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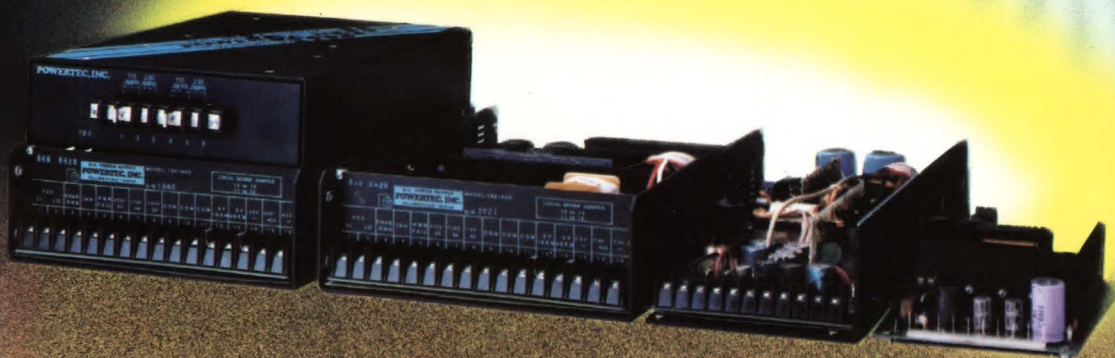
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November, 1984 (VS9)

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Selector Guide-Multiple Outputs

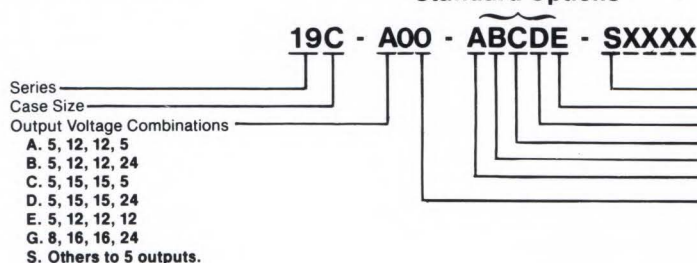
See MultiMod™ Family (Series 6) For Other Multiple Output Switchers To 1200 Watts.

MODEL NUMBER	OUTPUT RATINGS (CONVECTION COOLED) ⁴					LOAD REGULATION (PERCENTAGE)		Initial Output Voltage Tolerance (Adj.) ⁸ (±%) ⁹	
	TOTAL POWER ^{1,2,3,4}	VOLTS/AMPS ^{1,12} @ 50°C ³							
		#1 (MAIN)	#2	#3	#4	#1 (MAIN)	#2-4	#1 (MAIN)	#2-4
TRIPLE OUTPUTS—Use quad output models. Outputs may be deleted from quad output models for volume requirements.									
Quad Output		5	12	12	12	Volts (DC)			
19A-E01	50	+5V/7A	+12V/1A	−12V/1A	+12V/1A	±0.3	±1.0	Adj.	±5
19A-E00	60	+5V/7A	+12V/1A	−12V/1A	+12V/1A	±0.3	±2.5	Adj.	±5
19C-E01	150	+5V/25A	+12V/4A ¹⁸	−12V/4A	+12V/4A ¹⁸	±0.2	±0.2	Adj.	Adj.
19C-E00	170	+5V/25A	+12V/4A	−12V/4A	+12V/4A	±0.2	±2.5	Adj.	±5
6E5-BBB-17 ⁵	300	±5V/40A	±12V/6A	±12V/6A	±12V/6A	±0.2	±0.2	Adj.	Adj.
19E-E00	350	+5V/40A	+12V/6A	−12V/6A	+12V/6A	±0.2	±2.5	Adj.	±5
6F5-BBB-17 ⁵	400	±5V/50A	±12V/6A	±12V/6A	±12V/6A	±0.2	±0.2	Adj.	Adj.
19F-E00	400	+5V/50A	+12V/6A	−12V/6A	+12V/6A	±0.2	±2.5	Adj.	±5
Quad Output		5	12	12	5	Volts (DC)			
19A-A01	50	+5V/7A	+12V/1A	−12V/1A	−5V/1A	±0.3	±1.0	Adj.	±5
19A-A00	60	+5V/7A	+12V/1A	−12V/1A	−5V/1A	±0.3	±2.5	Adj.	±5
19C-A01	150	+5V/25A	+12V/4A	−12V/4A	−5V/4A	±0.2	±0.2	Adj.	Adj.
19C-A00	170	+5V/25A	+12V/4A	−12V/4A	−5V/4A	±0.2	±2.5	Adj.	±5
6E5-BBA-17 ⁵	300	±5V/40A	±12V/6A	±12V/6A	±5V/6A	±0.2	±0.2	Adj.	Adj.
19E-A00	350	+5V/40A	+12V/6A	−12V/6A	−5V/4A	±0.2	±2.5	Adj.	±5
6F5-BBA-17 ⁵	400	±5V/50A	±12V/6A	±12V/6A	±5V/6A	±0.2	±0.2	Adj.	Adj.
19F-A00	400	+5V/50A	+12V/6A	−12V/6A	−5V/4A	±0.2	±2.5	Adj.	±5
Quad Output		5	12	12	24	Volts (DC)			
19A-B01	50	+5V/7A	+12V/1A	−12V/1A	+24V/1A	±0.3	±1.0	Adj.	±5
19A-B00	60	+5V/7A	+12V/1A	−12V/1A	+24V/1A	±0.3	±2.5	Adj.	±5
19C-B01	150	+5V/25A	+12V/4A	−12V/4A	+24V/2A	±0.2	±0.2	Adj.	Adj.
19C-B00	170	+5V/25A	+12V/4A	−12V/4A	+24V/2 & 4A ¹⁷	±0.2	±2.5	Adj.	±5
6E5-BBD-17 ⁵	300	±5V/40A	±12V/6A	±12V/6A	±24V/6A	±0.2	±0.2	Adj.	Adj.
19E-B00	350	+5V/40A	+12V/6A	−12V/6A	+24V/2 & 6A ¹⁷	±0.2	±2.5	Adj.	±5
6F5-BBD-17 ⁵	400	±5V/50A	±12V/6A	±12V/6A	±24V/6A	±0.2	±0.2	Adj.	Adj.
19F-B00	400	+5V/50A	+12V/6A	−12V/6A	+24V/2 & 6A ¹⁷	±0.2	±2.5	Adj.	±5
Quad Output		5	15	15	5	Volts (DC)			
19A-C01	50	+5V/7A	+15V/1A	−15V/1A	−5V/1A	±0.3	±1.0	Adj.	±5
19A-C00	60	+5V/7A	+15V/1A	−15V/1A	−5V/1A	±0.3	±2.5	Adj.	±5
19C-C01	150	+5V/25A	+15V/4A	−15V/4A	−5V/4A	±0.2	±0.2	Adj.	Adj.
19C-C00	170	+5V/25A	+15V/4A	−15V/4A	−5V/4A	±0.2	±2.5	Adj.	±5
6E5-CCA-17 ⁵	300	±5V/40A	±15V/6A	±15V/6A	±5V/6A	±0.2	±0.2	Adj.	Adj.
19E-C00	350	+5V/40A	+15V/6A	−15V/6A	−5V/4A	±0.2	±2.5	Adj.	±5
6F5-CCA-17 ⁵	400	±5V/50A	±15V/6A	±15V/6A	±5V/6A	±0.2	±0.2	Adj.	Adj.
19F-C00	400	+5V/50A	+15V/6A	−15V/6A	−5V/4A	±0.2	±2.5	Adj.	±5
Quad Output		5	15	15	24	Volts (DC)			
19A-D01	50	+5V/7A	+15V/1A	−15V/1A	+24V/1A	±0.3	±1.0	Adj.	±5
19A-D00	60	+5V/7A	+15V/1A	−15V/1A	+24V/1A	±0.3	±2.5	Adj.	±5
19C-D01	150	+5V/25A	+15V/4A	−15V/4A	+24V/2A	±0.2	±0.2	Adj.	Adj.
19C-D00	170	+5V/25A	+15V/4A	−15V/4A	+24V/2 & 4A ¹⁷	±0.2	±2.5	Adj.	±5
6E5-CCD-17 ⁵	300	±5V/40A	±15V/6A	±15V/6A	±24V/6A	±0.2	±0.2	Adj.	Adj.
19E-D00	350	+5V/40A	+15V/6A	−15V/6A	+24V/2 & 6A ¹⁷	±0.2	±2.5	Adj.	±5
6F5-CCD-17 ⁵	400	±5V/50A	±15V/6A	±15V/6A	±24V/6A	±0.2	±0.2	Adj.	Adj.
19F-D00	400	+5V/50A	+15V/6A	−15V/6A	+24V/2 & 6A ¹⁷	±0.2	±2.5	Adj.	±5
Quad Output		8	16	16	24	Volts (DC)			
19A-G00	60	+8V/7A	+16V/1A	−16V/1A	+24V/1A	±0.3	±2.5	Adj.	±5
19C-G00	170	+8V/20A	+16V/4A	−16V/4A	+24V/2 & 4A ¹⁷	±0.2	±2.5	Adj.	±5
19E-G00	350	+8V/40A	+16V/6A	−16V/6A	+24V/2 & 6A ¹⁷	±0.2	±2.5	Adj.	±5
19F-G00	400	+8V/45A	+16V/6A	−16V/6A	+24V/2 & 6A ¹⁷	±0.2	±2.5	Adj.	±5

ORDER INFORMATION

Model/Product Description, Definitions

Standard Options



Custom Options
E: Factory Wired for 230 VAC Input
D: Power Fail—Option
C: Case or Cover¹⁵—Option
B: EMI Filter—Option
A: OVP on Auxiliary Outputs—Option
0: Regulation
0—Full⁷ regulation on main output;
Semi⁶-regulated on all others
1—Full⁷ regulation on all outputs

Powertec Series 19 Specifications

See SuperSwitcher™ Family (Series 9) For Single Output Switchers From 400 To 1700 Watts.

AC INPUT

Nominal—115/230 VAC, field selectable;¹⁴ 47 to 440 Hz¹⁶

Operating range—90-132 or 180-264 VAC.

Brown-out—Below 85 or 170 VAC.

Inrush current—For units that have been off for 0.5 hour, the maximum thermistor-limited inrush current is less than: 15 amps peak for the 19A, 35 amps peak for the 19C, and 50 amps peak for the 19E.

Undervoltage inhibit—Protected against malfunction due to AC undervoltage operation.

DC OUTPUTS

Adjustments—Only the fully⁷ regulated outputs (VDC) are adjustable up to $\pm 5\%$ (except the 19A auxiliaries which are nonadjustable).

Initial tolerance, auxiliaries—Tolerance of all semi⁶-regulated outputs and all 19A fully⁷ regulated auxiliary outputs is $\pm 5\%$ of nominal with all outputs at 50% load and main output set at 5.0 VDC.

Line regulation— $\pm 0.2\%$ over an input range of 90-132/180-264 VAC at 100% of rated load.

Load regulation—All outputs will operate from no-load to full-load. However, proper operation of the auxiliaries requires that the main output be loaded to at least 10% of its 50°C rating. Regulation is measured statically between 20% and 100% of the 50°C rated output. For this measurement, all semi⁶-regulated outputs not under test should have 20%¹⁹ loads. Fully⁷ regulated auxiliaries need not be loaded.

	Main Output			Auxiliary Output			
	19A	19C	19E/F 6E/F	19A	19C	19E/19F	6E/6F
FULL ⁷	$\pm 0.3\%$	$\pm 0.2\%$	$\pm 0.2\%$	$\pm 1.0\%$	$\pm 0.2\%$	N.A.	$\pm 0.2\%$
SEMI ⁶	$\pm 0.3\%$	$\pm 0.2\%$	$\pm 0.2\%$	$\pm 2.5\%$	$\pm 2.5\%$	$\pm 2.5\%$	N.A.

Dynamic response—A step load change of $\pm 25\%$ of rated maximum will cause a regulated output to deviate no more than 2%, with recovery to 0.5% in less than 400 μ sec.

Efficiency—Typically exceeds 75%.

Thermal regulation— $\pm 0.02\%/^{\circ}\text{C}$, fully regulated outputs. $\pm 0.05\%/^{\circ}\text{C}$, semi-regulated outputs.

Cross regulation—Measured with the output under test loaded at 20% of rated max. while the load on any other output is varied from 50% to 100% of rated max.

	Main (Varying auxiliary)	Auxiliary (Varying main)	Auxiliary (Varying auxiliary)
FULL ⁷	$\pm 0.1\%$	$\pm 0.1\%$	$\pm 0.1\%$
SEMI ⁶	$\pm 0.5\%$	$\pm 2.5\%$	$\pm 0.5\%$

Ripple and Noise—Any output, 0.5% max. RMS ripple. Typically 1.0% P-P measured with a 20MHz scope via X1 probe, having 4" max. return lead.

Hold-up time—Fully loaded outputs will remain within regulation for 20 msec. minimum from the last nominal line voltage peak.

OVER VOLTAGE PROTECTION

Main output—Both crowbar OVP and inverter shutdown OVP standard on all models except 19A.

Auxiliary outputs—Inverter shutdown standard on all models. OVP crowbar (Option A): All fully regulated auxiliary outputs except 19A. Standard on 6E/6F auxiliaries. Remove AC input for 30 sec. to restore operation.

NOTES:

- Maximum continuous output power may not exceed the product of rated current and voltage specified in the Selector Guide at indicated temperatures as measured at the output terminals.
- Max. total power of all outputs combined.
- Above 50°C, current and power ratings derate linearly to 50% at 70°C.
- Higher current and power ratings attainable with moving air. Consult Factory. (Excludes 6F and 19F models.)
- Outputs for 6E and 6F are floating (i.e., outputs may be wired for either plus or minus and may be paralleled).
- Semi-regulated outputs. "Semi" have less circuitry in order to improve cost. Load regulation is sufficient for many requirements.
- Fully regulated outputs. "Full" have additional circuitry to assure better regulation than the semi-regulated outputs.
- Output voltage adjustable to $\pm 5\%$ of specified nominal.
- Output voltage non-adjustable. Initial voltage within $\pm \%$ tolerance indicated.

Range—OVP ranges are factory fixed as follows:¹³

5 VDC: 5.5-6.9 VDC	15 VDC: 16-20 VDC
8 VDC: 9.5-10.9 VDC	24 VDC: 25-29 VDC
12 VDC: 13-16 VDC	24 VDC: 31-32 VDC (19E, 19F only)

REVERSE VOLTAGE PROTECTION

Semi-regulated—Protected to rated current.

Fully regulated—Main output protected to rated current. All others protected to 1 amp continuously or full rated current momentarily.

LOADING vs. TEMPERATURE

Convection cooling—100% rated loads from 0°C to 50°C. Derate linearly to 50% at 70°C.

Forced air cooling—100% rated loads at 70°C with 400 LFM air directed along unit (excluding 6F & 19F).

REMOTE SENSING

Standard on +5 VDC output and 6E/6F auxiliaries. Can accommodate 0.25 VDC cable-drop. Open sense protection is provided. (Not available on 19A.)

CURRENT LIMITING

Main output and fully regulated auxiliary outputs are protected against overload and short circuits by fold-back current limiting. Semi-regulated auxiliaries are protected against continuous shorts.

POWER FAIL

Option D: A TTL compatible logic low signal will occur at least 2 ms before the loss of output following the loss of AC input.

LOGIC INHIBIT

All outputs will be shut off by the application of a TTL compatible logic low signal to the inhibit terminal.

SAFETY

Meets the test specifications listed below.

UL submittals are automatic for standard units; check with factory for current status on any model. Powertec has been granted self-certification status by CSA. CSA logo available upon request.

UL 114, UL 478, UL 1012

CSA 22.2-143, CSA 22.2-154

IEC 380¹⁰ IEC 435¹⁰

VDE 730¹⁰ VDE 804¹⁰ VDE 0806¹⁰

Hiprot—3500 VDC Input to Output; 2100 VDC Input to Case; 750 VDC Output to Case for qualification test.

For production test, 1500 VDC, 1500 VDC and 500 VDC respectively.

Creepage/Clearance—3mm primary to secondary. 4mm primary to case.

Leakage—Less than 1 mA input to case.

Grounding—Case ground terminal provided.

Insulation—Exceeds 10 M Ω at 500 VDC.

EMI

Option B allows these units to meet the conducted EMI requirements of FCC Rule 15J (Docket 20780) and VDE 0871 as shown.

	19A	19C	*19E/19F/6E/6F
FCC	Class A	Class B	Class B
VDE	—	Class A	Class A

*Preliminary

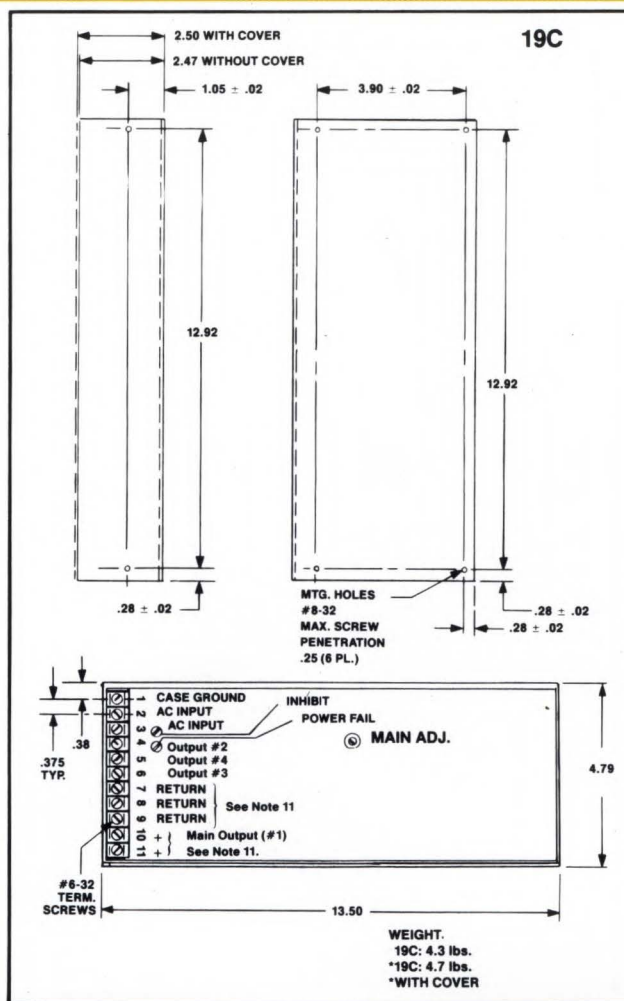
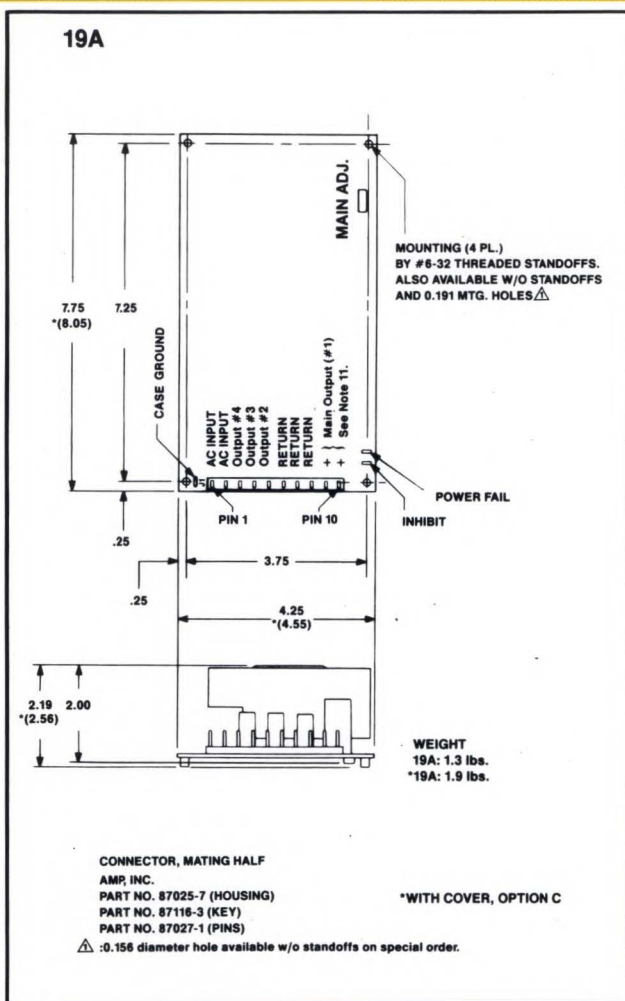
WARRANTY—1 year

- Class 1 non-SELV: Meets European safety requirements except in cases where a system does not provide for grounding, or where the possibility exists that an operator (maintenance personnel excepted) can come into physical contact with the power supply or its load terminals.
- Must be connected (wired) to the load in parallel.
- Higher peak current ratings may be obtained. Contact Factory.
- Trip occurs within the applicable range.
- Units shipped are strapped for 115 VAC input. Customer may change for use at 230 VAC.
- Cover standard with 6F and 19F, optional on all others.
- 6F and 19F operate at 47-63 Hz only, except on special order.
- Line/load regulation, ripple and noise typically double at the higher current rating indicated.
- To increase output current: Outputs No. 2 and No. 4 may be paralleled. Contact Factory for details.
- Outputs will operate at lower load conditions with degraded regulation.

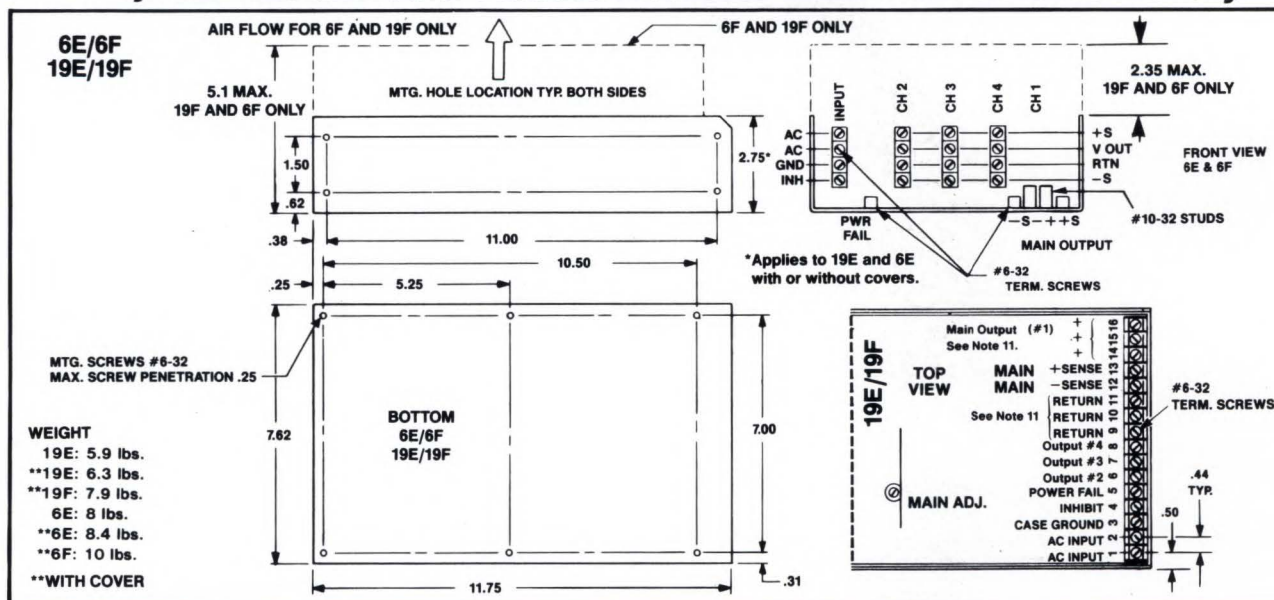
November, 1984 (VS9)

Contact Factory to Obtain Powertec's Free Loose-Leaf Binder/Catalog to Which You May Add This and Other Product Brochures Which Are Published Monthly.

Outline and Mounting Dimensions



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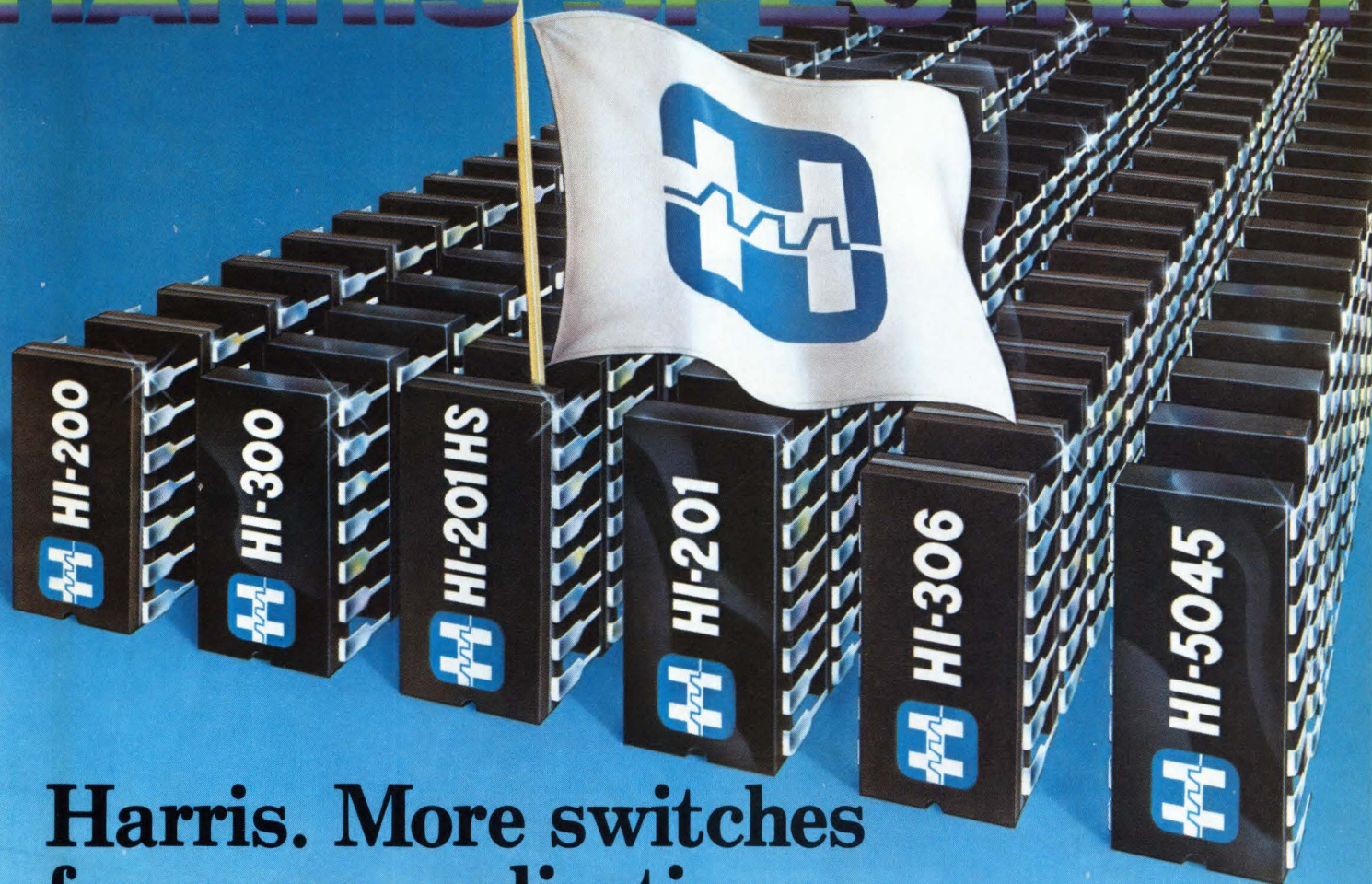
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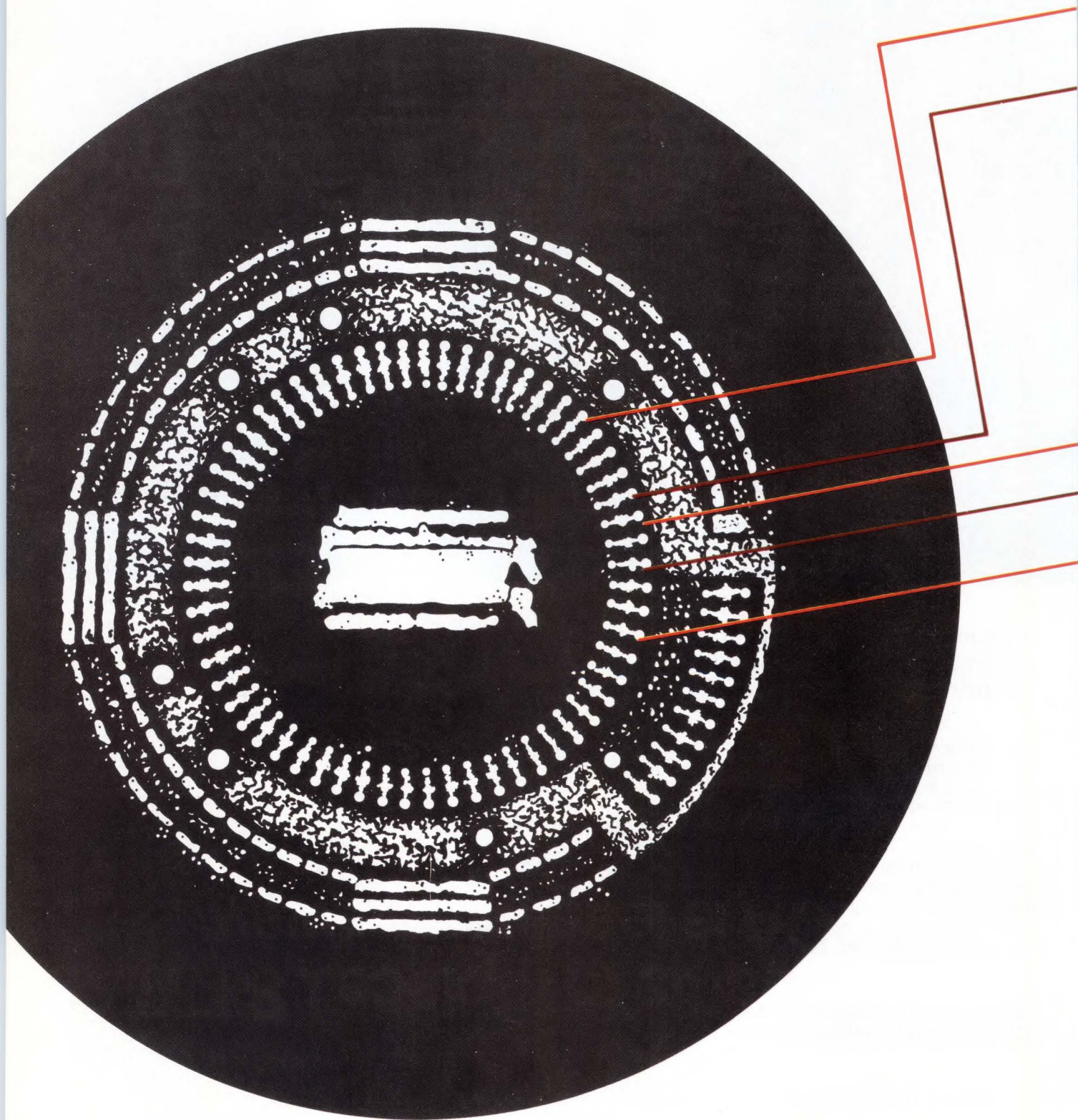
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HARRIS

Harris CMOS Analog Switches Product Summary

Function	Part Number	Typical "On" Resistance (Ω)	Typical "Off" Output Leakage (nA)	Typical Turn On Time (ns)
SPST	HI-5040	50	0.5	370
2 $\times$ SPST	HI-200	55	1	240
	HI-300	35	0.04	210
	HI-304	35	0.04	210
	HI-381	35	0.04	210
	HI-5048	25	0.5	370
	HI-5041	50	0.5	370
4 $\times$ SPST	HI-201	55	1	180
	HI-201HS	30	0.3	30
SPDT	HI-301	35	0.04	210
	HI-305	35	0.04	210
	HI-387	35	0.04	210
	HI-5050	25	0.5	370
	HI-5042	50	0.5	370
2 $\times$ SPDT	HI-303	35	0.04	210
	HI-307	35	0.04	210
	HI-390	35	0.04	210
	HI-5051	25	0.5	370
	HI-5043	50	0.5	370
DPST	HI-5044	50	0.5	370
2 $\times$ DPST	HI-302	35	0.04	210
	HI-306	35	0.04	210
	HI-384	35	0.04	210
	HI-5049	25	0.5	370
	HI-5045	50	0.5	370
DPDT	HI-5046A	25	0.5	370
	HI-5046	50	0.5	370
4PST	HI-5047A	25	0.5	370
	HI-5047	50	0.5	370



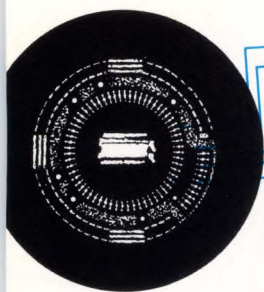
TESTING VLSI CIRCUITS

The job
starts in
design

Today's application-specific ICs and tight schedules are making designers acutely aware of the testability of their handiwork, something once the sole concern of test engineers. Customarily, a test engineer having enough probes, DIP clips, jumpers, and other test fixtures could always find some way of testing a stubborn circuit on a pc board. But VLSI techniques offer no such luxury: Untestable chips are unusable. Planning a chip's test strategy during the design phase pays off in time, the time it takes to write and to verify effective production test programs.

The design workstation is a natural breeding place for creating VLSI test programs. Already tools like fault simulators and automatic test program generators are winding up in the IC specialist's workstation, and the system's

Gil Bassak



net list (interconnections and circuit parts) and functional models constitute much of the information needed to devise a test program.

The cross-fertilization between design and testing techniques has begun. With new tools at hand, savvy designers are doing more with their simulators and test generators than merely creating testable circuits; instead they are using them to build better ICs. For their part, test engineers are drawing on high-level programming and hardware description languages—typically design aids—to devise more efficient ways of modeling faulty circuits. For now, great hope lies in designers and test engineers sharing their tools.

With such creative synergy between the two disciplines, as the technical program at last month's International Test Conference in Philadelphia testified, difficult test problems can be solved.

Unfortunately, the link between a workstation and its test equipment is usually an afterthought, compromising somewhat the ability to create good or even adequate test patterns. Moreover, verifying the fault-finding and diagnostic skills of those patterns is considered by some to be virtually impossible.

For the most part, the burden of grading test patterns falls to the fault simulator, which must model circuit faults to check a test pattern's worth. Though the latest soft-

ware and hardware simulators are keeping pace, some experts are wondering if a technique called "testability analysis" might not be the ultimate key to making big, testable chips (see "Fault Finding: Two Competing Approaches," below).

The design workstation is the obvious place to develop and grade test vectors, since the test development software can easily draw, as the design software does, on a data base that constantly updates itself with every change in a circuit. Nevertheless, test vectors in the workstation must find their way to the target system, a fact that has makers of fault simulators and testers inching toward factory-wide integration of

Fault finding: Two competing approaches

In one sense, the seemingly uphill search for faster, more efficient ways of modeling faults is a constant reminder of how big a problem testability really is. Some industry experts now suggest that fine-tuning the technique called fault simulation may not be the entire answer. Instead, the solution might lie in a completely different approach to confirming testability—namely, testability analysis. That technique judges a circuit's ability to be tested in terms of two factors: how easily it can be controlled and how closely it can be observed. Others involved in testing suggest that testability analysis should work alongside fault simulation, not necessarily replace it.

The supporters of each approach have strong arguments in their favor. For instance, testability analysis requires no test vectors, only a topological analysis of the circuit. Furthermore, it guides the designer to the optimal test vectors, instead of leading him or her through the slow process of trial and error demanded of fault simulation.

Testability programs like Scoap (Scandia controllability/observability analysis program) originally measured a circuit's testability early in

the design cycle, leaving time to modify and improve the design before running fault simulation and test generation programs. A design tackled in that manner can run faster and require less computer resources. Testability advocates now suggest that Scoap and similar programs could also gather information normally supplied by fault simulation.

Backers of fault simulation counter that their method's advantages are overwhelming, despite the fact that fault simulation becomes exponentially harder to perform as a circuit's complexity rises. The technology is improving continually; software is faster and cheaper than ever. Very large circuits can be partitioned to speed the process even further. Moreover, all possible faults need not be simulated; in fact, sampling no more than 2000 faults is usually sufficient to cover virtually all circuits.

Continuing their argument, defenders of fault simulation point out that designing a VLSI circuit to meet the strict criteria of testability analysis exacts a heavy toll in silicon. Moreover, analysis cannot deliver the valuable diagnostic information that fault simulation does, even though it might ultimately produce thoroughly testable circuits.

designing and testing chips.

Consider the Chipchecker software, which assists designers in debugging prototype ICs by letting them control a tester through the Cadat logic fault simulator. With the software, devised by HHB-Softtron (Mahwah, N.J.), a designer can extract test vectors and download them to the tester, which in turn reports the chip's performance to the workstation.

In a similar vein, Factron/Schlumberger (Billerica, Mass.), formerly Fairchild Manufacturing Test Systems, has just developed an interface that directly downloads VLSI-based pc board layout and test vector information from a Daisy workstation to Factron's functional and in-circuit testers.

Compatibility is key

The direct transfer of data from workstation to tester serves a purpose greater than mere convenience. A designer's familiarity with a circuit promises to improve the caliber of test programs. For instance, Tektronix Inc. (Beaverton, Ore.) has developed a technique for automatically transferring simulation test patterns from a host to the DAS 9100 digital analyzer. As a result, the system compares acquired data with expected results, thereby revealing a chip's faulty operation. With that setup, the analyzer can easily verify prototype chips.

Designers are also finding that traditional tools can double as aids for developing test

programs. For example, while a designer is examining the results of a simulation, he or she can also be developing test patterns that locate large numbers of faults.

For some time, high-level procedural languages and hardware description languages have been defining a circuit's function. But lately they have appeared at the forefront of automated VLSI testing, and for good reason: As VLSI circuits grow more complex, gate-level fault simulations put a heavier burden on computer resources. Hardware description languages, however, relieve computers of that burden by abandoning the minute details of each gate. Therefore they execute more

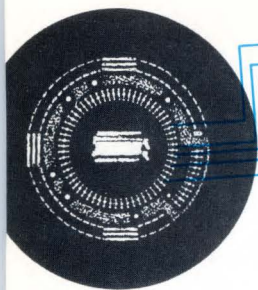
quickly and require less powerful computers.

Even where computer power is not an issue, gate-level descriptions of a microprocessor or other VLSI device are not readily available and are extremely difficult or impossible to derive. Moreover, in the early stages of design, a device's high-level description, like its architecture or function, invariably precedes the gate-level one.

A designer can understand a circuit better when it is represented by a hardware description language rather than by the gate-level model. The question facing test engineers is: Can HDLs model faulty circuits as accurately as gate-level simulations and therefore be used to grade test

INCREMENTER: =	!Model name
begin	
primary input	
INP<0>.	!Declaration
internal . variable	
INT<2:0>.	
primary . output	
OUT<2:0>.	
begin	
if INP<0>	!Statement 1a
then INT<2:0> = 000;	!Statement 1b
OUT<2:0> = INT<2:0> + 1;	!Statement 2
INT<2:0> = OUT<2:0>	!Statement 3
end	
end	

1. Research at DEC uses a high-level procedural language as the foundation for modeling a circuit, in this case, an incrementer. The language simplifies the automatic generation of test patterns. In the statements, the variables are arrays of bits. The first variable, INP, is declared as a primary input only one bit wide (indicated by the single subscript). The internal variable, INT, and the primary output, OUT, are both three bits wide (as indicated by the three subscripts).



patterns?

One project has already extended the benefits of high-level hardware description languages, which are generally used for design alone, to generating test patterns. Digital Equipment Corp. (Hudson, Mass.) tried out its experimental test program generator on a microsequencer chip. Researchers typed in the chip's published specifications using a hardware description language, omitting only the chip's 6-by-12-bit register stack (Fig. 1). From that model, the generator produced 189 test patterns.

An A+ in performance

How well did that modest number of test patterns perform? Of the 1414 possible stuck-at faults reported by conventional fault simulators, the 189 test patterns de-

tected 99.7% of them. What's more, the four faults that were not detected represented problems in the program's implementation, not in its underlying methodology. Based on these results, further research will aim at automatically generating test patterns for more complex chips.

In another crossover of testing and design software, Teradyne Inc. (Boston) is searching for ways that its Lasar-6 simulator can assist design engineers well before the testing stage of production chips. The goal is to derive the test vectors directly and easily from the patterns developed to verify the design.

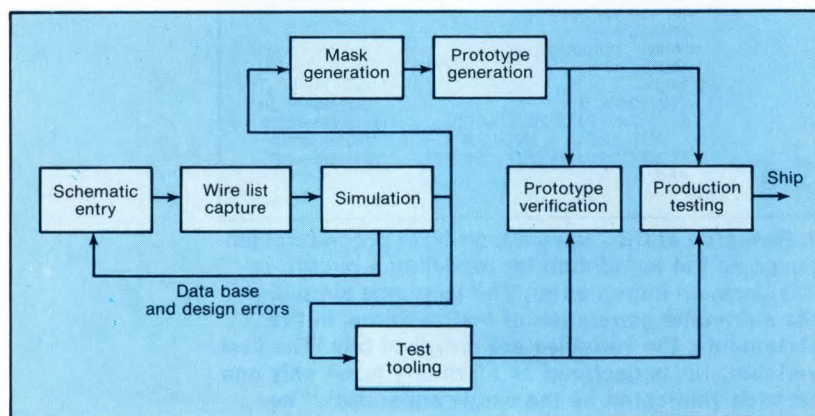
Teradyne designers, who were developing gate arrays for automatic test equipment, used Lasar-6 to create a set of

stimulus patterns (Fig. 2). The simulator, originally intended for writing and grading test patterns, models logic and timing. It gives maximum and minimum timing information and provides "phased" input patterns (in other words, patterns with implicit timing information). In addition, the simulator analyzes potential hazards, pinpointing bus conflicts, timing races, and other design faults. As a test simulator Lasar-6 naturally inserts faults to determine how effectively a test program can reveal them.

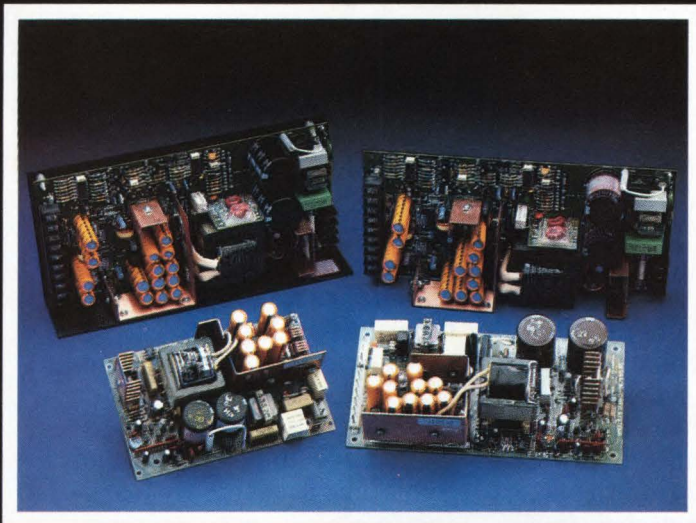
Grading gate arrays

Teradyne's results show that the simulator's patterns helped designers to analyze a gate array's logic functions and timing. In fact, errors of all kinds—schematic entry, circuit modeling, logic, timing—were caught and corrected early in the design process. Several designers changed their approach to developing gate arrays: They worked more rapidly in the early design stages, confident that the simulator would locate most errors later.

The stimulus and response patterns used to verify the logic proved to be a valuable asset for testing the first silicon and production versions of the gate arrays. Because the simulator generated a response for each test input, the designer has a complete set of test vectors as soon as the array is designed. With that arrangement, he or she need no longer deal with the time-



2. Generally used for grading test patterns, Teradyne's Lasar-6 fault simulator proves to be a powerful aid for designing, say, a gate array. The designer writes a set of functional stimuli that activate the model and then analyzes the model's logic and timing to verify the circuit. When the design is complete, the net list and stimuli are post-processed for incoming and outgoing inspection tests.



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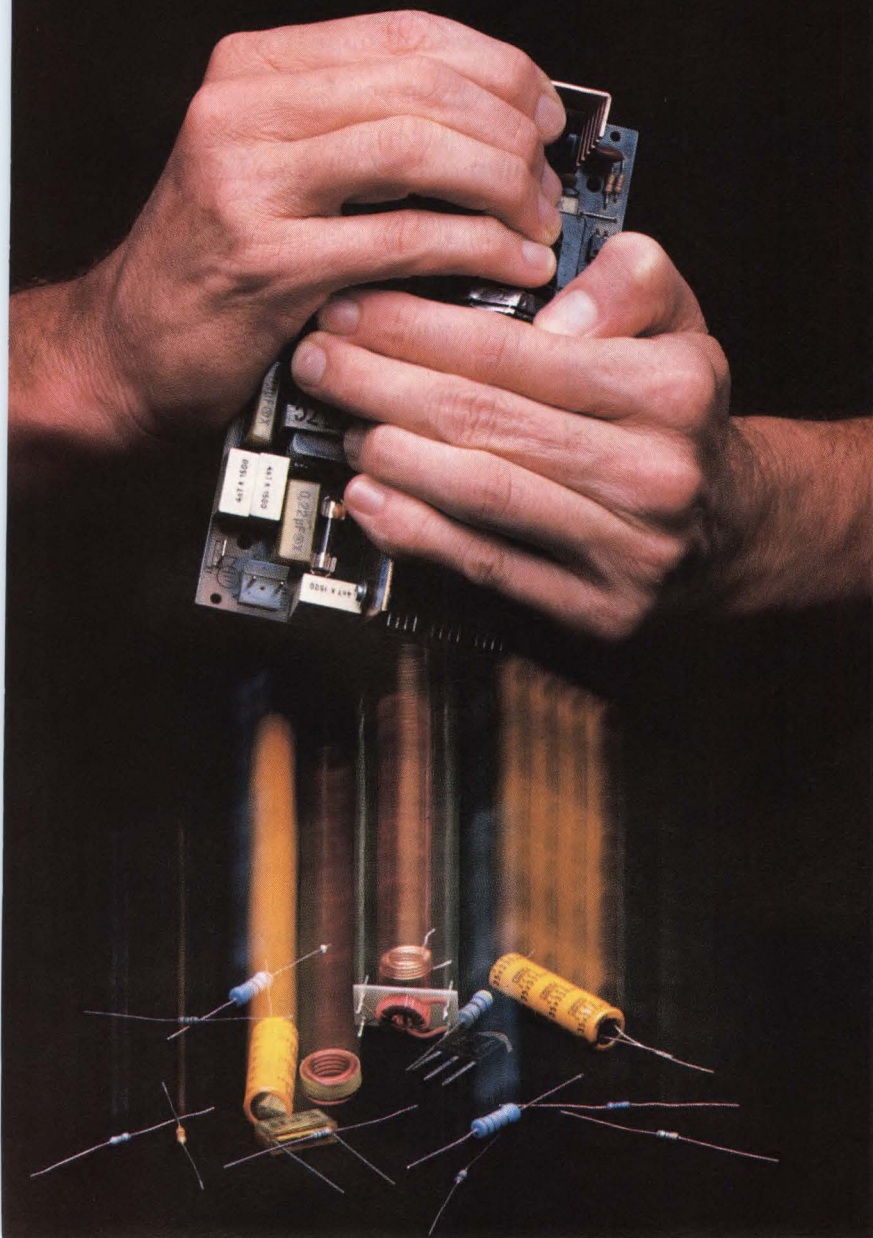
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consuming task of writing the test program after the design cycle.

When the test vectors proved insufficient to check a gate array fully for faults, Teradyne designers chose to modify the gate array for testability before sending it to production. Furthermore, they became more aware of the problems they had unknowingly caused test engineers by not making testability a high priority in the past.

Automatic test pattern generators, too, are moving

into the design cycle, at least at NEC Corp. (Tokyo). Planning originally to counter the high cost of manually producing logic verification patterns, researchers developed the mixed-level simulator-verifier which consists of five evolutions (or models) of software that use automatic test-pattern generation to verify logic design. Each evolution is more efficient and useful for logic verification than its predecessor. All versions accept high-level functional and structural descriptions of a circuit, as well as auto-

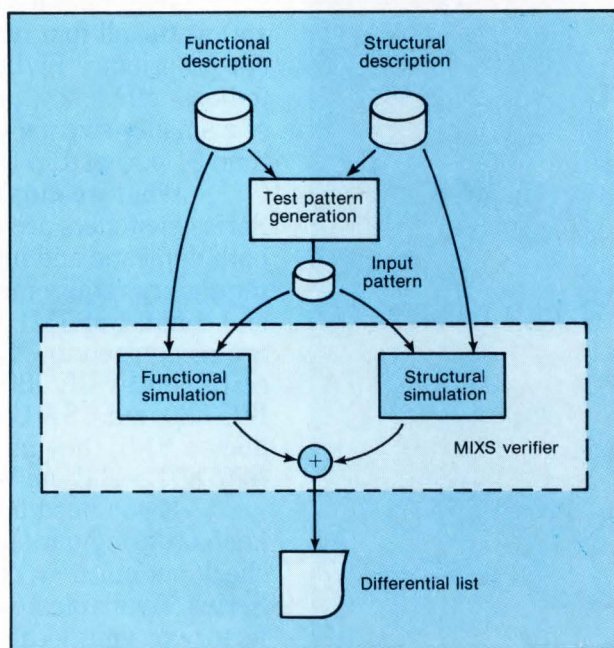
matically generated test patterns. The simulator-verifier then checks the circuit's response for a one-to-one correspondence between the two descriptions (Fig. 3).

Applying that design automation approach to more than 500 LSI designs, NEC could save money, time, and machine resources by working in a high-level language rather than with gate-level descriptions. Moreover, the results of the circuit verification are more certain than when done manually.

O say can you C . . .

Considerations of that sort spurred AT&T Co. (Princeton, N.J.) to develop an architectural-level fault model of a moderately complex MSI device, a 74LS164 shift register (Fig. 4). They started with the shift register for two reasons. First, it is easy to model architecturally in the C language. Second, the researchers had a gate-level model of the chip in their fault simulator; thus they could evaluate fault coverage in terms of the model and the high-level architectural descriptions.

The results were encouraging. First, 80 stuck-at faults were inserted in the high-level model, and a 46-pattern test detected all of them. The results were comparable to those achieved with the gate-level model. Another kind of failure, the "latched-at" fault, which prevents the shift register's memory elements from changing state, showed



3. A mixed-level simulator verifier developed by NEC plays a key role verifying logic with the help of automatic program generation software. The MIXS verifier compares the responses of a logic design's functional description (written in a functional description language) with its structural representation. The generator creates patterns by incrementing exhaustively from all 0s to all 1s.

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equally encouraging results (Fig. 5).

Inspired by success, the AT&T researchers developed an architectural-level fault simulator and an associated simulation model of their 8-bit WE 8000 microprocessor. The model, called the architectural fault simulator (AFS), is written in C, like its predecessor. Applying an existing test to the model and inserting 2512 faults, the researchers found the fault coverage to be 95%.

The architectural fault simulator actually comprises a user interface and a model. The former lets the user interactively control the simulation, examine and set the resources of the target (the virtual machine that is simulated), and debug the model and the test program (see the table, p. 150). The model itself is written for the particular target to be simulated.

Although the simulator was written in C, its inventors claim that a hardware de-

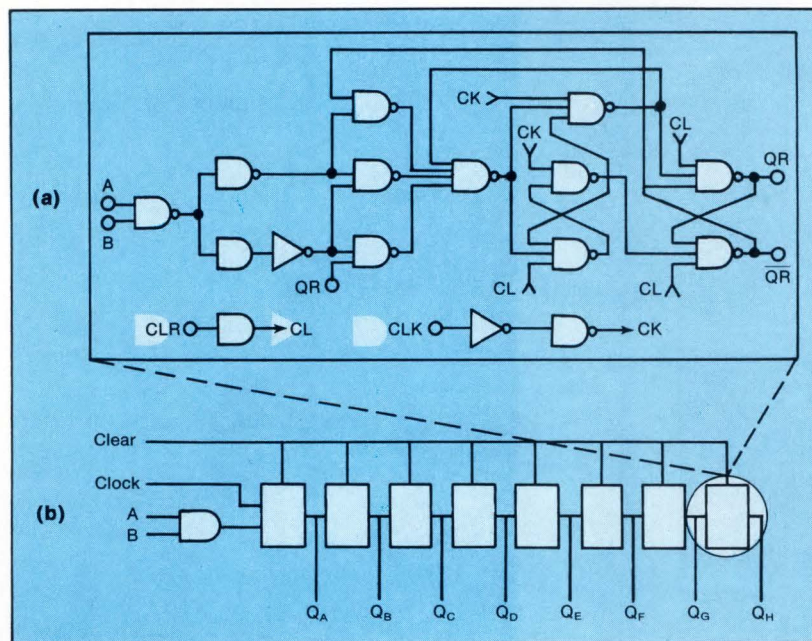
scription language could have been used. Nevertheless, C is considered to be a standard in the computer industry, and as such it is becoming a force in VLSI testing.

A language for all

Part of its appeal is that it borrows features from both high- and low-level languages. For example, C's efficiency approaches that of assembly language: It executes quickly and uses little memory. Its large number of operators make it resemble machine language, giving it the ability to manipulate individual bits and bytes. At the same time, C has several high-level flow-control instructions, like "for," "if... then... else," "do... while," and others. It also has pointers to data structures and goes further than other high-level languages by permitting efficient access to data structures by means of pointer arithmetic.

Moreover, the language's high-level features lend themselves to top-down (structured) programming, enabling someone to write, debug, and maintain code more efficiently than with assembly language. Finally, C runs under the popular Unix operating system.

Members of Zilog Inc.'s Test Development Group (Campbell, Calif.) have been using C to devise device-oriented test vectors instead of tester-oriented ones. That approach replaces confusing tables of logic 1s and 0s with



4. Unlike the gate-level model of a 74LS164 shift register (a), a high-level architectural-level representation is much simpler (b). Proposed by AT&T, the high-level structure eases the burden of fault simulation by sparing the computer the chip's details. Yet the simulator sacrifices nothing in its ability to measure fault coverage.

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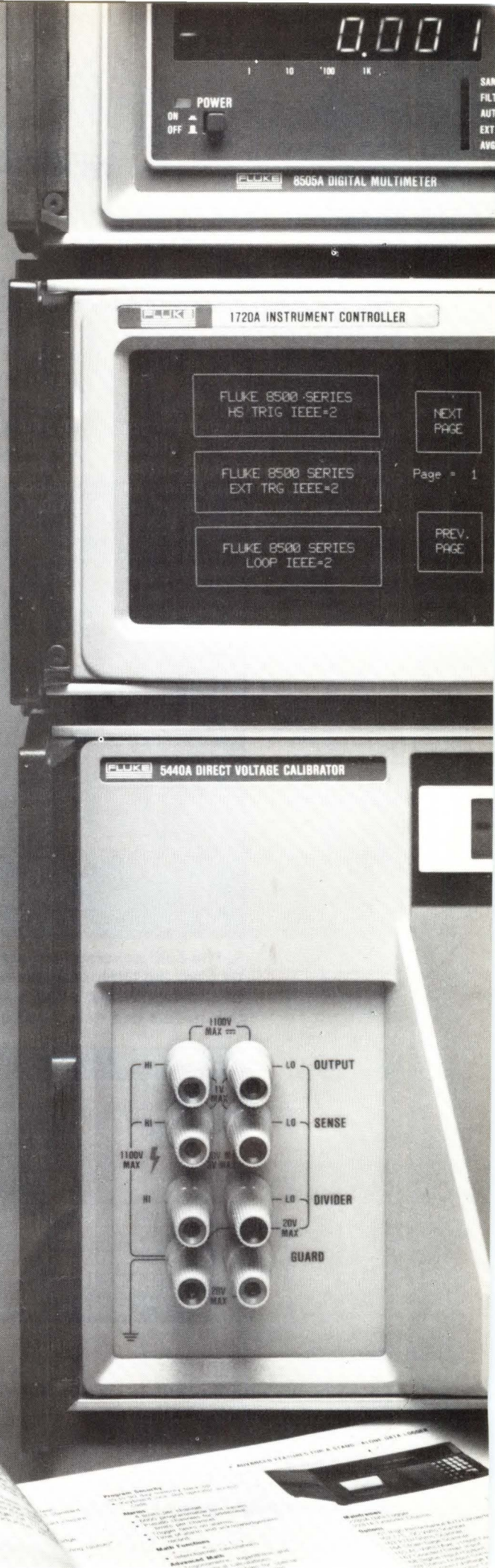
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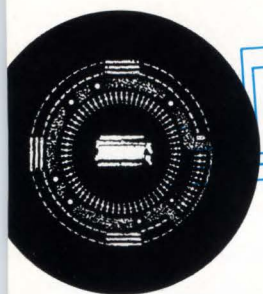
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TECHNOLOGY REPORT: TESTING VLSI CIRCUITS

more readable descriptions of circuit operations. Furthermore, it requires very little effort to move a test program among various testers.

Zilog's test software has already been put to work generating test vectors from the

output of a computer simulation. A disassembler, written in C, recognizes bus transactions and asynchronous input events and produces test patterns in the form of C language function calls. For instance, if the computer-

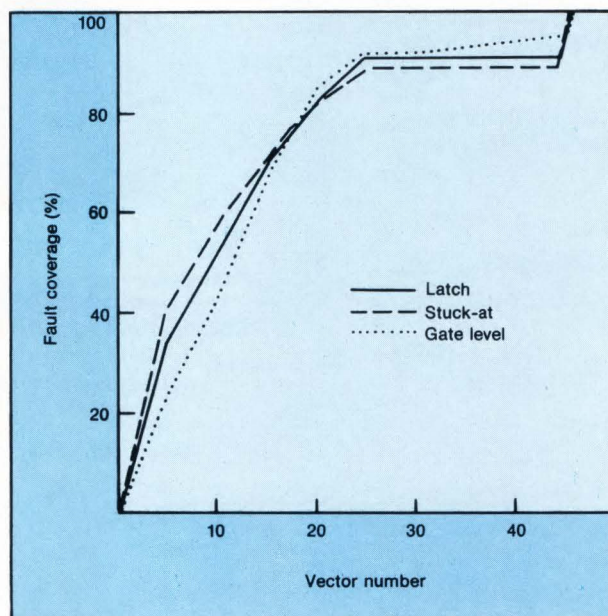
simulated transaction involves a memory read from address $A5A5_{16}$, the disassembler detects the simulation pattern and creates the statement memory (read, $0xA5A5$) in an output file (Fig. 6).

The test pattern and the definitions of the C function calls are compiled, producing a truth table for a nonspecific tester. Ultimately that truth table can be translated into data for a specific tester or used with a benchtop tester.

In a second application, the test software runs on a Z8001-based tester, which interfaces with the device under test. The tester draws on the actual device hardware and on assembly language software (Fig. 7). It interactively debugs and verifies the first silicon of a new device. Adding a text editor turns the subsystem into a fast generator of test vectors.

Although not new to testing, simulators that mix hardware and software hold great promise. Nowhere is this truer than in speeding up fault simulation of VLSI devices, the complexity of which taxes simulation software, the computer it runs on, and the test engineer who must wait for the results.

Of the various approaches to fault simulation—namely, serial, parallel, deductive, and concurrent—the serial algorithm is by far the slowest. In fact, it is hundreds of times slower than the fastest method, concurrent simulation. But the advent of hard-



5. The fault coverage of gate-level models differs little from the latch and stuck-at faults of architectural-level models. AT&T's 46-vector test stimulates the models and detects all architectural-level faults.

AFS user Commands		
Simulator control commands	Setting simulator state	Simulator resource display
Help	Break	Assign
Quit	Clear	Display
Run	Trace Full	Set
Continue	Trace Fault	Examine
Restart	Trace Inst	
I, Obey	Sample	
Init	Notify	
Output		

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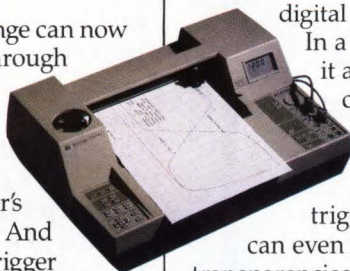
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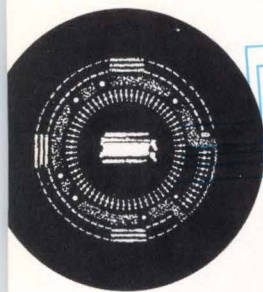
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TECHNOLOGY REPORT: TESTING VLSI CIRCUITS

```

ENABLE MA, DA;
SET F 0000000000000000 1000 1010101010 1010101010;
ENABLE MB, DB;
SET F 0000111100001111 1000 1010101010 1010101010;
SET F 0000111100001111 1000 1010101010 1010101010;
ENABLE MA, DA;
SET F 0000000010101010 0000 1010101010 1010101010;
SET F 1111111111111111 0000 1010101010 1010101010;
SET F 1111111111111111 1000 1010101010 1010101010;

```

(a)

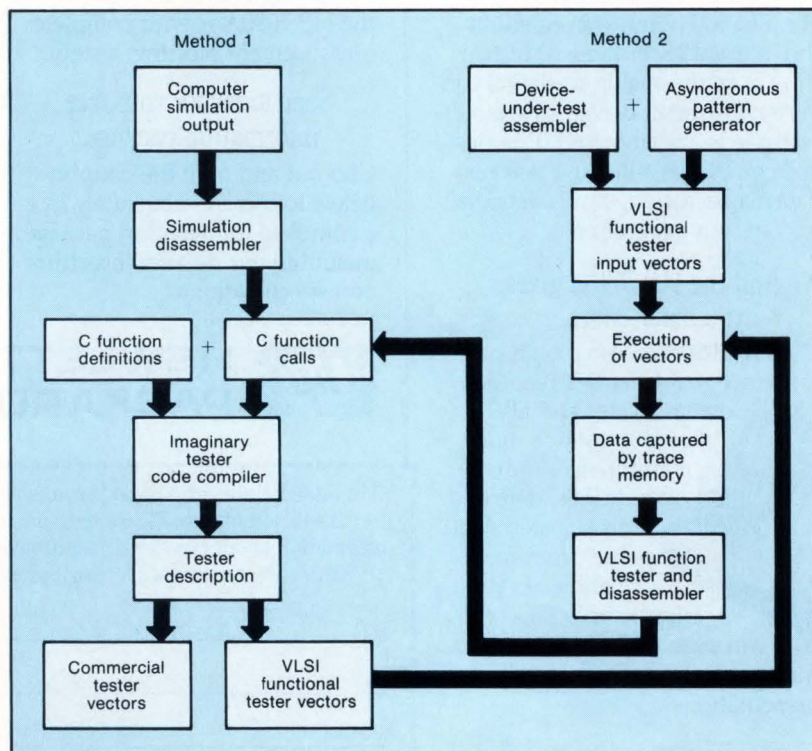
```

opcode_fetch (0,0x0F0F); /* bus transaction */
reset (interrupt1,t1); /* asynchronous input */
io (write,0xAA,0xFFFF); /* bus transaction */

```

(b)

6. The device-oriented approach for generating test vectors has two advantages: confusing strings of logic 1s and 0s (a) are replaced by readable descriptions (b), and the test vectors can easily be moved to another tester.



7. In producing device-dependent test vectors, test patterns and definitions of the C function calls are compiled, producing a truth table that describes an imaginary tester (method 1). From that truth table Zilog derives vectors for a commercial tester and a single-board VLSI tester. The latter can also generate vectors (method 2).

ware engines could make serial fault simulation as much as 400 times faster than before.

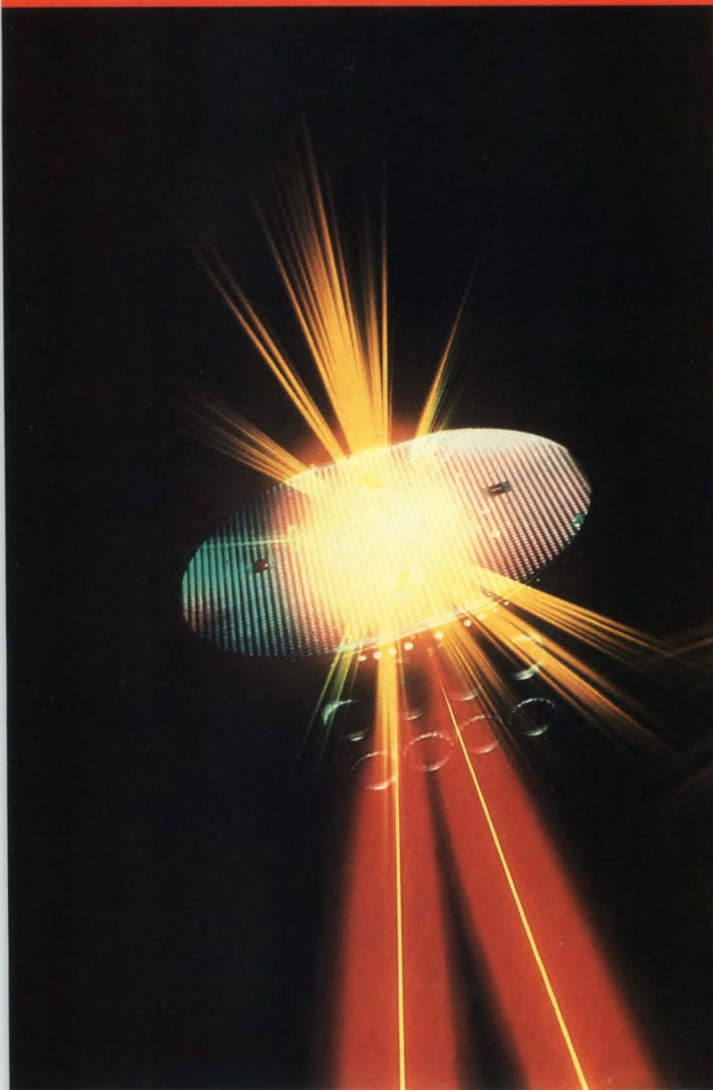
Digital Equipment, recognizing the vast possibilities for quickly grading test patterns and diagnostic programs, distributes fault simulation between a software-based concurrent simulator and a hardware-based serial simulation engine (based on the Zycad LE 1002). The company connects the hardware engine to a VAX processor via the computer's Unibus, setting up a high-bandwidth interface for hardware control, design verification patterns, and simulation results. In addition, a network link makes the simulator engine accessible to designers throughout the company.

Next it developed a way to use the software and hardware simulators alone or together, the latter affording the fastest throughput. Overall, letting the hardware engine simulate selective faults and having the software tool insert statistical faults (to avoid having to fault every node in a circuit) improved the diagnostic programs that designers developed. In fact, for runs of 200 faults the hardware-based serial approach was often faster than the software-based concurrent simulation. With these results in mind, DEC is now turning its attention to hardware simulators that process data in a parallel rather than in a serial fashion. □

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HC/HCT367*	Hex Buffer/Line Driver; 3-State	
HC/HCT368*	Hex Buffer/Line Driver; 3-State; Inverting	
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HC4050	Hex HIGH-to-LOW Level Shifter	

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HC/HCT175	Quad D-Type Flip-Flop with Reset	
HC/HCT273	Octal D-Type Flip-Flop with Reset	
HC/HCT374*	Octal D-Type Flip-Flop; 3-State	
HC/HCT534*	Octal D-Type Flip-Flop; 3-State; Inverting	
HCT564*	Octal D-Type Flip-Flop; 3-State; Inverting	

LATCHES

HC/HCT373*	Octal Transparent Latch; 3-State	
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HC563*	Octal Transparent Latch; 3-State; Inverting	
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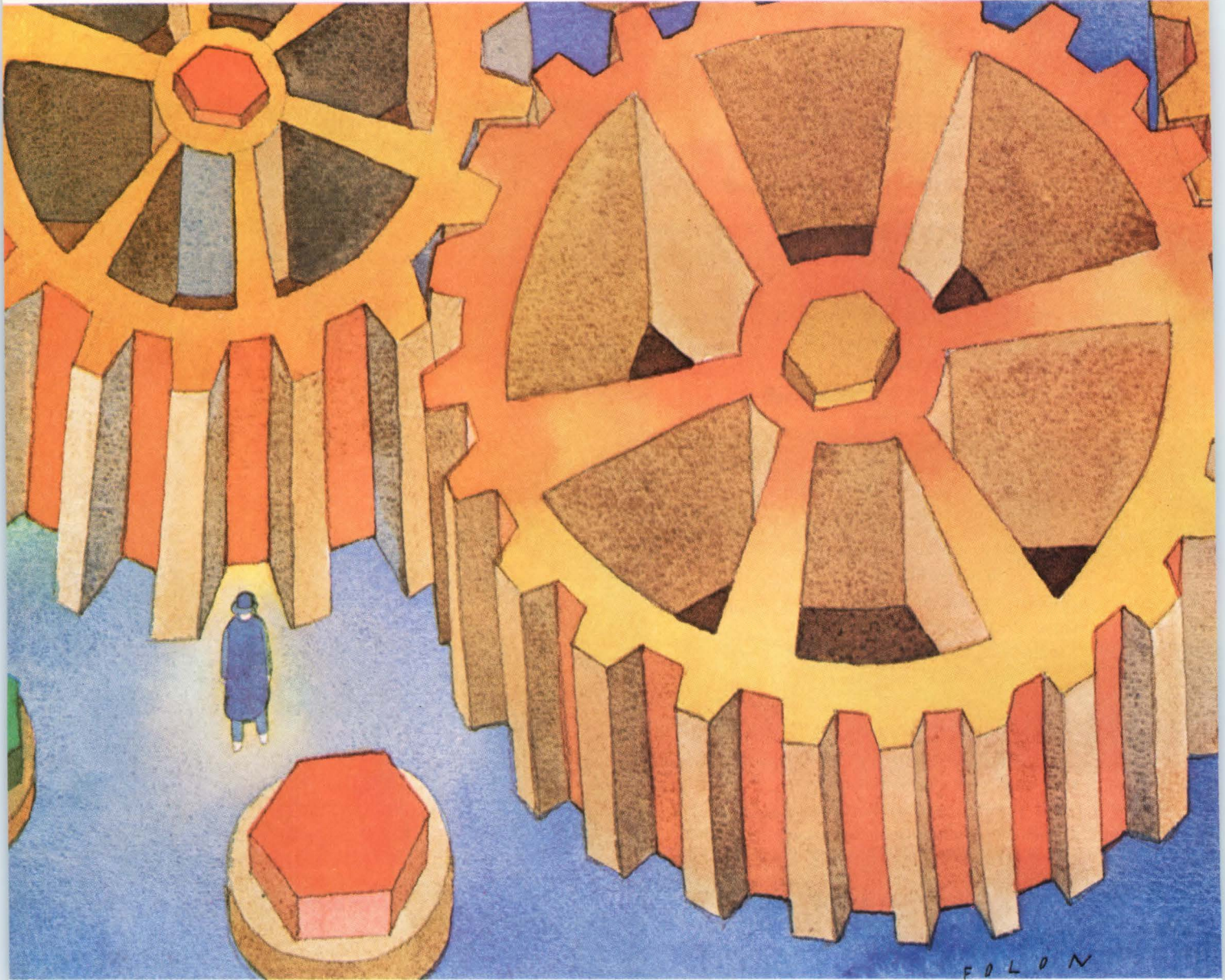
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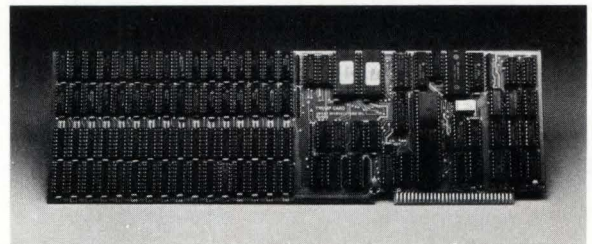


IBM® and other compatible PC computers are fast enough for general home and office use. But, for hardware and software development applications, the gears turn slowly.

What you need is a faster "gear" to co-process with the Intel 8088 inside IBM's PC. Like Zilog's Z8001® CPU. Now, there's a way to increase throughput for the IBM PC—as well as test the performance of the Z8001 CPU for your high-performance applications with a Z8001 CPU-based board called the "Trump Card" from Sweet Microsystems. And it proves dramatically how powerful Zilog's 16-bit CPU really is.

The new device is a peripheral board that plugs into any expansion slot on an IBM PC or compatible PC computer. Trump Card is addressed as an I/O device that communicates through the expansion bus. It is powered by Zilog's Z8001 CPU.

The Trump Card increases the computational power of the IBM PC, and provides maximum performance with a minimum of board space.



The Trump Card, shown from the front. The left side of the board contains 512 K-bytes of type-4164 dynamic RAM; the right side contains the Zilog Z8001 and an interface to the IBM PC I/O-expansion bus.

Z8001 COMPILER BASIC IS 80 TIMES FASTER THAN IBM INTERPRETIVE BASIC.

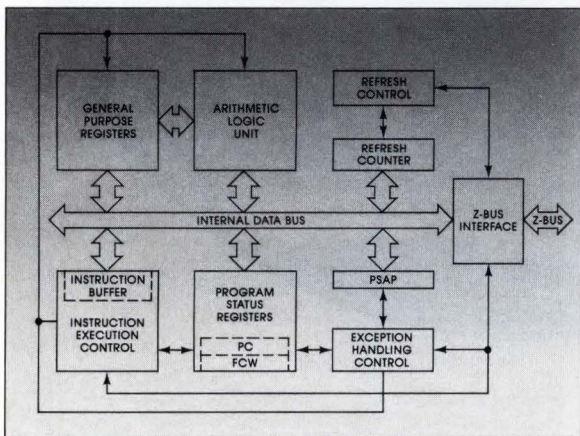
Essentially a monolithic minicomputer central processing unit, the Z8001 CPU is characterized by an instruction set more powerful than many minicomputers. As the programmer sees it, the Z8001 contains sixteen 16-bit general-purpose registers (for addresses or data) that may also be used in groups to form as many as eight 32-bit registers or four 64-bit registers. The low-order halves of the registers may be used for byte operations, thus the Z8001 CPU is able to manipulate data in 8-, 16-, 32-, and 64-bit pieces.

The Z8001 CPU, running at 10 MHz, can execute the same programs 4 to 10 times faster than the Intel 8088. What's more, the Z8001 CPU, with its large 8-megabyte memory range, makes the Trump Card's 512K bytes of memory easy to design with. (To use this memory in the card, you simply load a BASIC, CP/M-80, or C program from PC-DOS and type "RUN:")

Apple II	Apple III	TRS-80 Model II	IBM PC	IBM PC (with Trump Card)
224	222	189	190	2.4

A comparison of execution times (in seconds). Running on IBM's interpretive BASIC, a Sieve program takes 190 seconds to execute. Running the same program under TBASIC on the Trump Card Compiler takes only 2.4 seconds.

The eight addressing modes are register, indirect-register, direct-address, indexed, immediate, base-address, base-indexed, and relative-address. The instruction set utilizes data types ranging from single bits to a 32-bit long word. What's more, the processor executes 110 distinct instruction types that, when permuted by all the addressing modes and data types, create a set of more than 400 instructions.



A Z8000 CPU functional block diagram of the internal structure of the Zilog Z8000 family of high-performance microprocessors.

ALL THE PROPER SUPPORT FOR 512K BYTES OF MEMORY.

The wide range of software written for the Z8001 CPU is proven by all the programs you can run on the Trump Card. With the Z8001-based Trump Card, you can run the following software on your IBM or other compatible PC:

BASIC Compiler—TBASIC is PC BASICA-compatible. Most instructions are implemented without modification.

CP/M-80 Emulator—Allows you to run CP/M-80 Z80 assembly language programs directly. Just download your Z80 programs and run them.

C-Compiler—The industry standard version of C is available.

Debugger—Intended to aid in program development, you can examine and change memory and register contents and more.

Screen-editor—Has many word processing features, including ASCII text file development.

Multilevel Language Compiler—Allows Pascal-like control and data types, arithmetic expressions with automatic or specified allocations of registers, and more.

RAM Disk—Can allocate 128K to 387K bytes of on board memory to function as an intelligent RAM disk.

COPROCESSING IS JUST PART OF THE STORY.

The Z8001-based Trump Card is just one example of a successful application design for the Z8001 CPU. But there's far more to the Z8000 family than this.

Today, Z8000 CPU's are used in a wide range of applications, from industrial and medical products to computers and graphics imaging machines. And Zilog stands behind every application with service and software support that makes your Z8000-based products get to market on time.

Find out for yourself how much power Zilog packs into every Z8000 CPU by turning your IBM PC into a faster tool for modern times.

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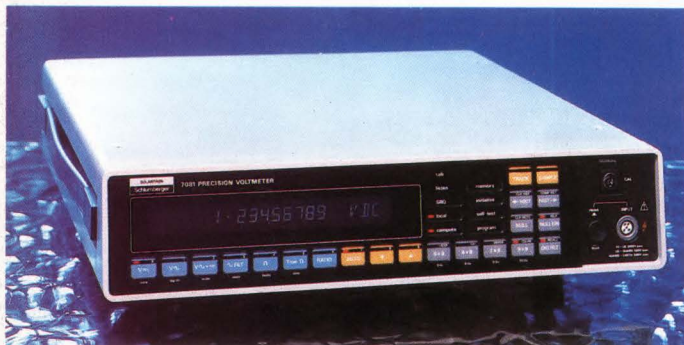
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READER SURVEY

ON PERSONAL COMPUTERS

AN EDITORIAL SERIES

PERSONAL COMPUTERS

FROM DESIGN
TO MANUFACTURING





**Engineers and
their managers depend
heavily on the many
resources of their
personal workstations.
A survey reveals
when and why they
come in handy,
and how they can
keep up with tomorrow.**

Jesse Shereff

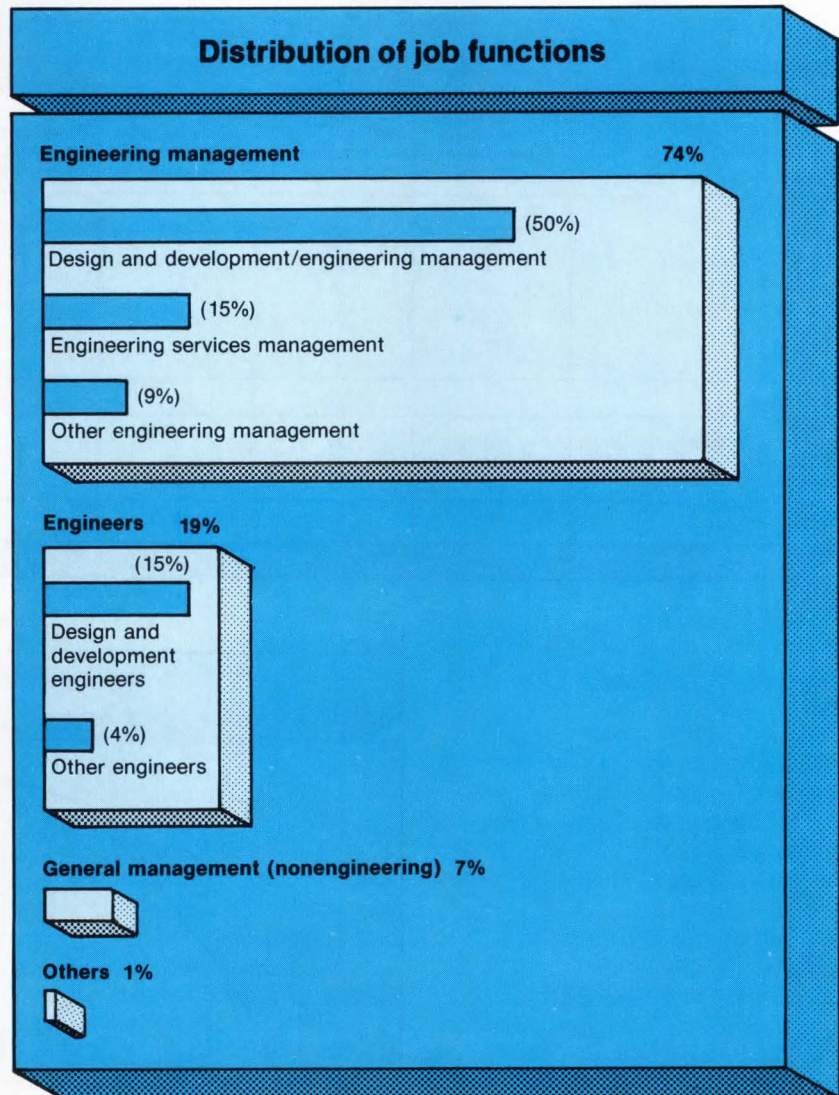
READER SURVEY

Perhaps nothing in the past five years has affected the engineering workplace as strongly as personal computers. Not only do they play steadily more important roles in job activities, they also help engineers catch up on loose ends at home as well. In fact, an astounding 90% of the readers that responded to ELECTRONIC DESIGN's recent survey use personal computer-based workstations on the job, and another 7% hope to get one of their own soon.

Asked a broad assortment of questions, ELECTRONIC DESIGN readers have given us a clear picture not only of the types of systems they use, but also of the software they run, their job responsibilities, how the applications differ for engineers and engineering managers, and how hardware and software stack up for now and for the future. The results of the survey are being presented in two issues: This report examines what kinds of personal computers are now being used and for what purposes, the second will explore the users' assessments of their systems and what the latter will need to meet demands over the next decade.

Our survey was delivered to 2000 engineers and managers. We received 396 responses, yielding a 20% answer rate that is about average for this

Figure 1



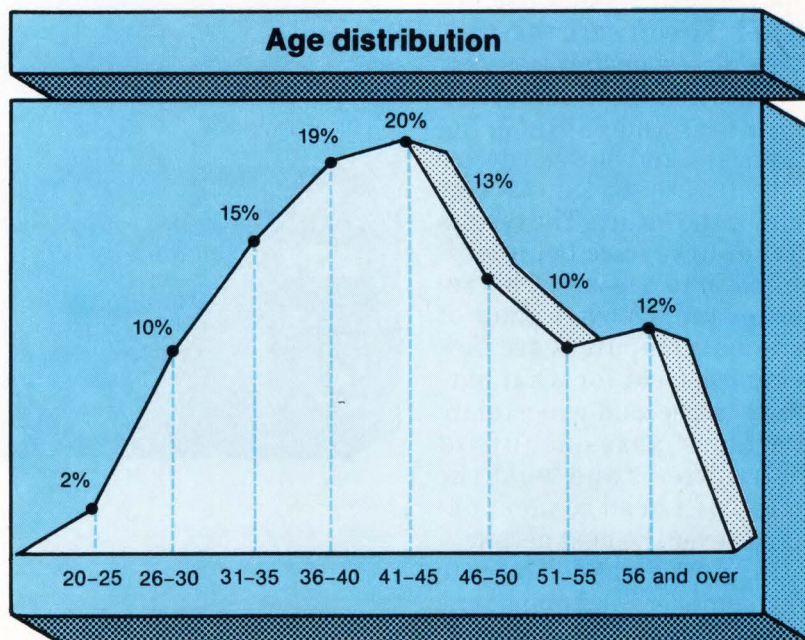
PERSONAL COMPUTER SERIES



Table 1. Type of computer usage

Age	Pc workstation plus other computer services	PC workstation without other computer services	Other computer services, and hope to get PC soon	Other computer services, but no need for PC	No computer services, but hope to get PC soon	No computer services, no need for PC
20-30	64	36	3	0	3	0
31-35	64	23	7	2	2	0
36-40	64	25	3	3	4	1
41-45	65	25	3	0	6	0
46-50	59	29	6	2	4	0
51-55	83	11	0	3	0	3
56 and over	68	22	5	2	0	2
Position						
Engineering manager	66	24	3	2	4	1
Engineer	64	26	8	1	1	0
General manager	69	27	0	0	0	0
Total sample	67	23	4	2	3	1

Figure 2



READER SURVEY

type of survey. Statistics are rounded off to the nearest percentage point; thus the total may not always add up to 100%.

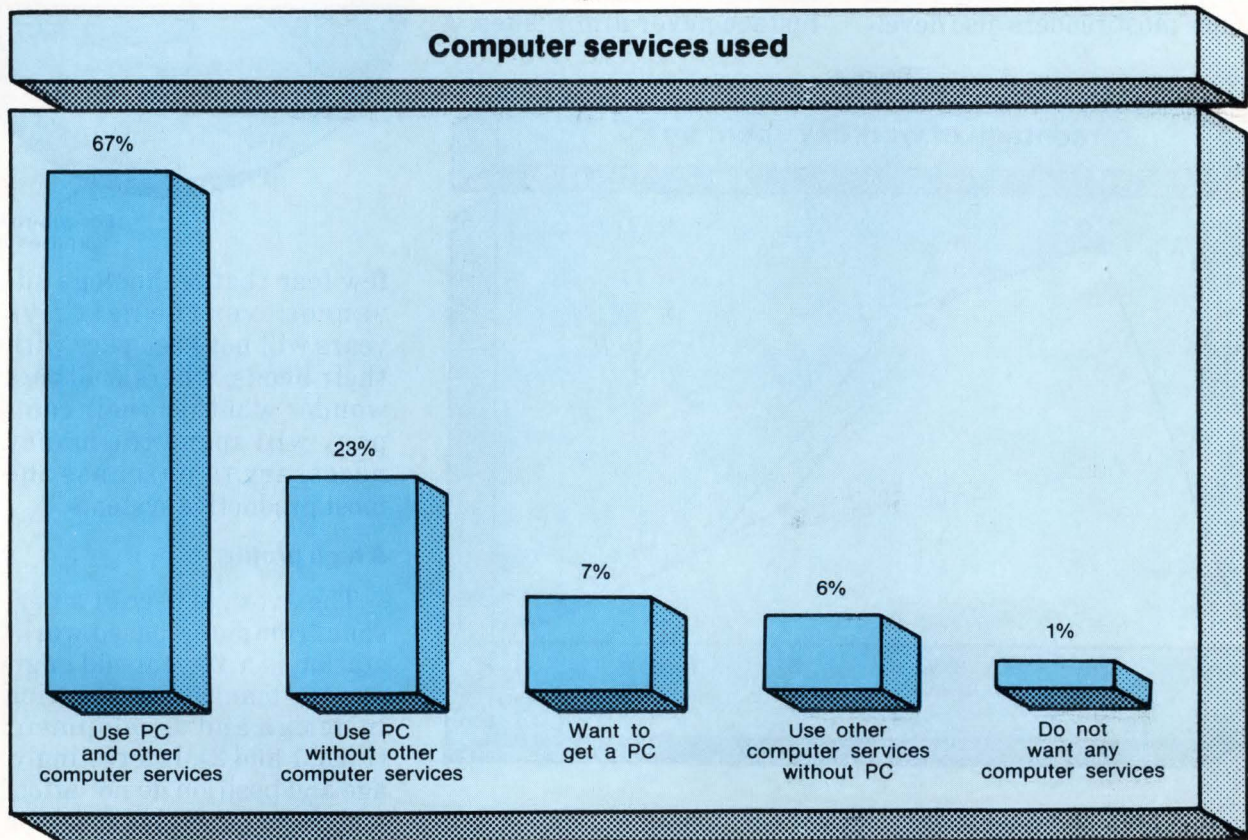
Though most of the respondents use personal computers, the engineering industry has yet to see an influx of the

larger 32-bit workstations geared for computer-aided engineering and design. Most readers work with various 8-bit CP/M-based machines, Apple IIs, TRS-80s, Commodores, and Kaypros and with 16-bit systems like the IBM personal computers and

other MS-DOS setups. Even with that lineup, a significant number consider terminals linked into time-sharing computers to be their personal workstations.

Not surprisingly, smaller systems do not usually tackle pure engineering jobs like

Figure 3



PERSONAL COMPUTER SERIES



chip and board design, on-line control, or testing and measurement. Instead, they are more likely assigned duties like word processing, project management and scheduling, data-base applications, and financial analysis. Nevertheless, programming crosses into the realms of both small and large microcomputers, since most readers also devel-

op software and write application programs on their machines.

They're OK, but

By and large, engineers and engineering managers are content with their current workstations, though the desire for more speed, more memory, and a better user interface never diminishes. A

Figure 4

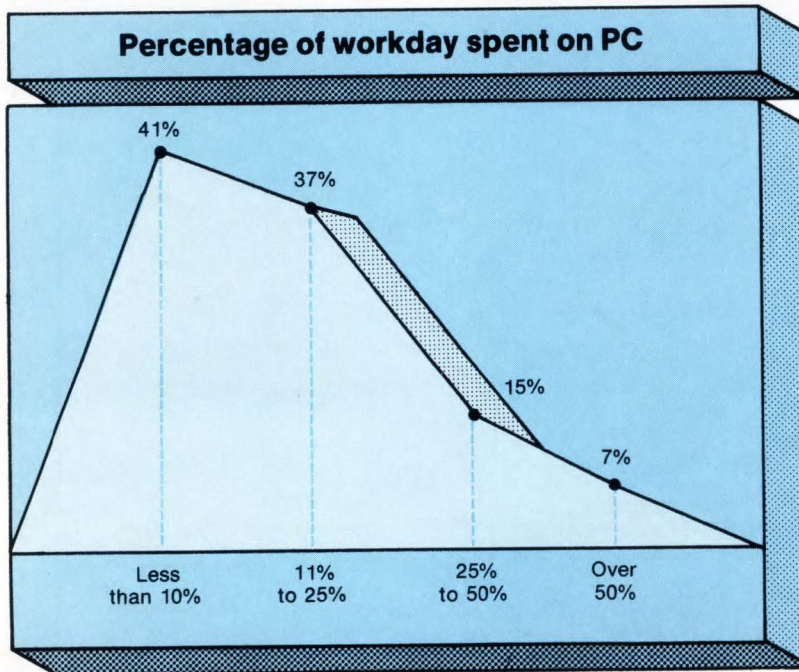
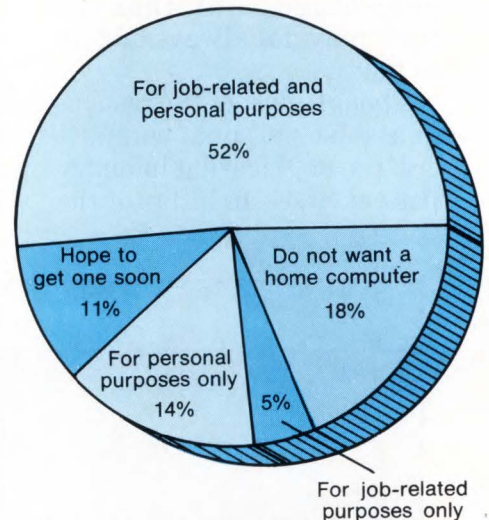


Figure 5
Use of home computers



few fear that technology advances over the next five years will not keep pace with their needs, whereas others wonder whether their company will spend the money necessary to purchase the most productive systems.

A high profile

The average user of a personal computer-based workstation is a 42-year-old engineering manager specializing in design and development (Figs. 1 and 2). Interestingly, age and position do not affect whether the engineer uses a computer or even for what purposes (Table 1). Obviously, a manager is far more likely to manage and schedule projects on his personal computer than is an engineer without

management responsibilities.

ELECTRONIC DESIGN readers are a remarkably computer-literate bunch. Two-thirds of them use both a personal workstation and other computer services, and nearly a quarter do all their computing on their workstation (Fig. 3). Only 3% see no reason for a PC in their job, 4% use no computer services, and only 1% have no need for computer services of any kind. Six percent of the respondents rely strictly on other computer services, with no recourse to a personal computer.

Though personal computers have penetrated their workplace, engineers and engineering managers do not necessarily devote much time to them. Only 23% spend more than a quarter of their work week seated at the computer, and 41% are busy at the PC for only a tenth of the time (Fig. 4). In all likelihood, those statistics will change when the sophisticated 32-bit workstations become more common.

Seventy percent of the readers have personal computers at home, with many of those machines similar to and often compatible with the PC at work. Indeed, more than half apply their home system to both work and personal purposes, and another 5% assign it strictly to job-related

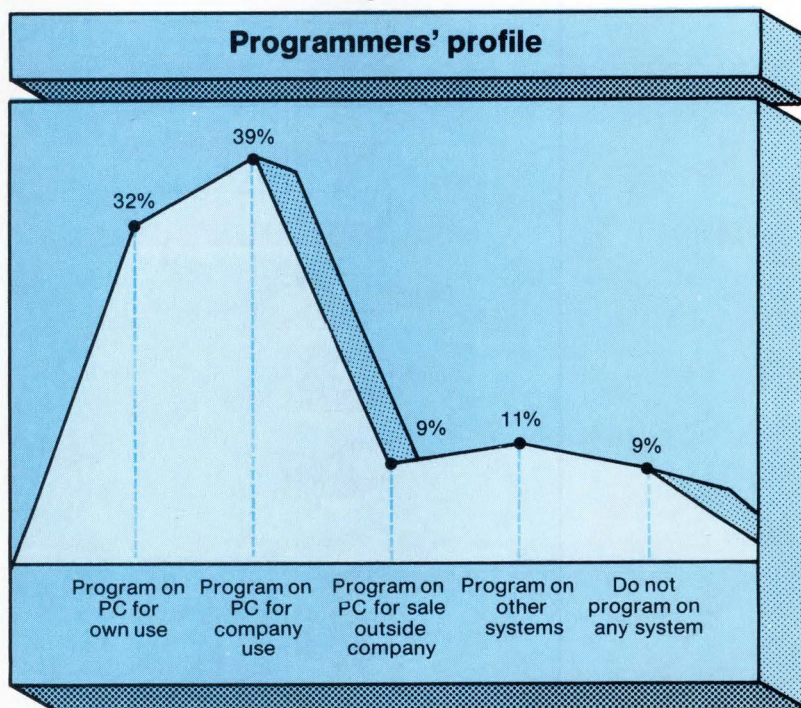
activities (Fig. 5). Only 18% have neither plans nor the desire to obtain a personal computer for their home.

Hands-on software

Whereas business users rarely program their own personal computers, preferring instead to run standard application software, the re-

verse is true for readers of ELECTRONIC DESIGN (Fig. 6). A full 80% not only write but also debug programs on their workstations; only 9% do no programming at all. Slightly more than one-third develop software for their company's use, and another third write programs for themselves. An enterprising nature appears

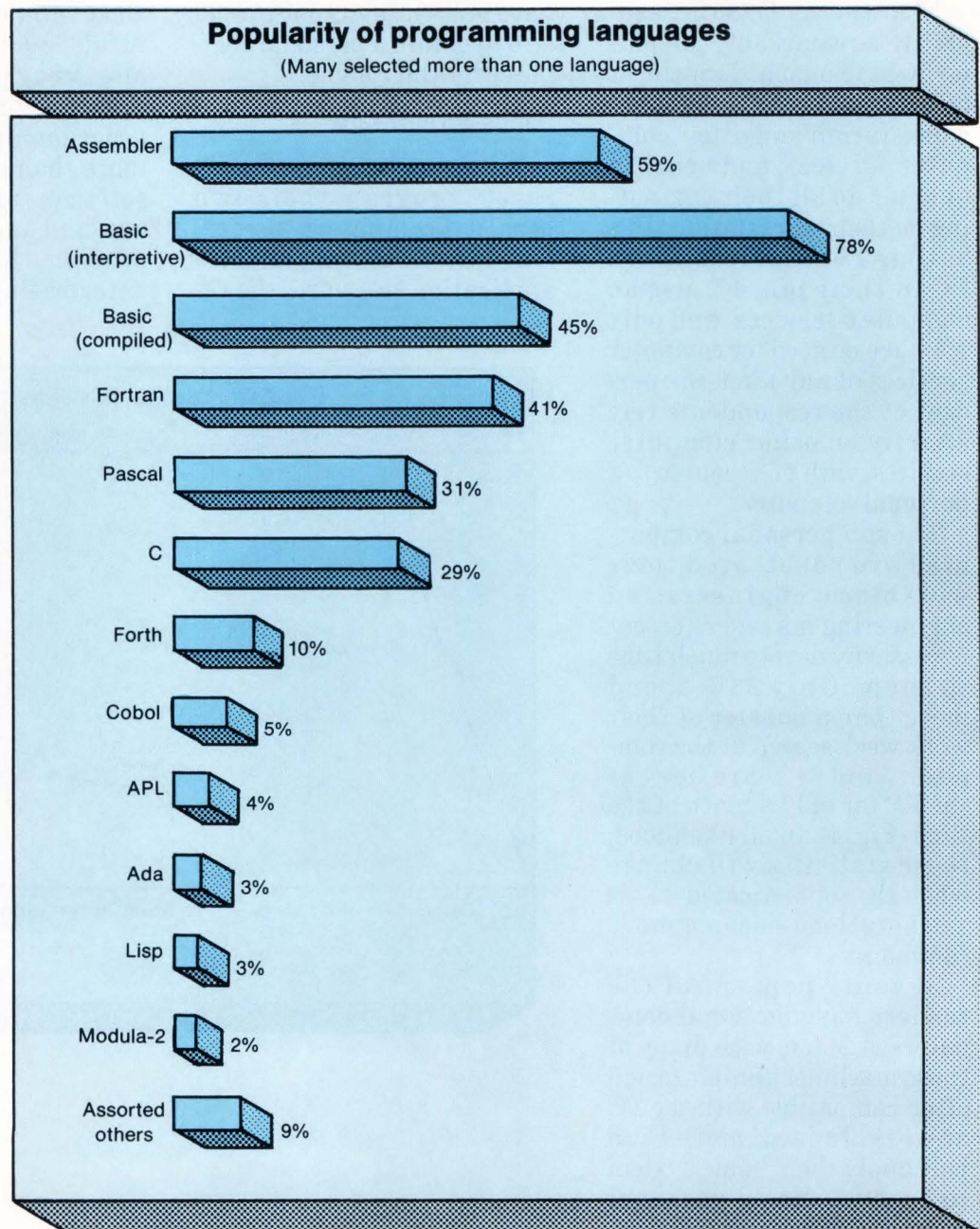
Figure 6



PERSONAL COMPUTER SERIES



Figure 7



READER SURVEY

in another 10% of the respondents, who actually sell the software they develop on their personal computer.

Interpretive Basic and assembly language—respectively the easiest and hardest to learn—are the most frequently used programming languages (Fig. 7). Both come bundled with many 8- and 16-bit systems. With the exception of C, which is usually supplied with Unix-type systems, other programming languages are purchased as an option.

Not popular

Compiled languages are not in high favor among the engineering group, perhaps because the ones found on 8-bit and 16-bit PCs are generally a limited subset of languages used in mainframes. The problem is somewhat less severe for 16-bit systems. The Basic compiler is the most popular of this group, followed sequentially by Fortran, Pascal, and C. Forth has a more modest backing, and compilers for Cobol, APL, Lisp, Ada, and Modula-2 are used by fewer than 5% of the respondents. Full-feature Fortran and Pascal compilers that are compatible with their mainframe equivalents are now being offered for 32-bit workstations.

Like programming lan-

guages, the jobs performed on workstations are rather limited by system type. For more than three-quarters of the readers, word processing is the primary (sometimes secondary) activity, probably because every engineer and manager must at one time or another write reports. Pro-

ject management and scheduling were listed by almost two-thirds of the readers as the second most common tasks—a percentage that makes sense for a survey in which more than 80% shoulder some management responsibilities. Programming, software development, and

Table 2. Workstation applications by job function (%)

Application	Engineering managers	Engineers	General managers	Total
Chip design	4	5	4	4
Board design	14	13	4	13
Manufacturing and on-line control	10	7	24	10
Testing and measurement	32	25	16	30
Other engineering functions	25	25	8	25
Software development	58	66	48	59
Programming for own needs	59	64	52	60
Project management and scheduling	71	48	52	65
Financial analysis	47	31	52	44
Data-base applications	55	44	56	52
Word processing	78	76	76	77

PERSONAL COMPUTER SERIES



data-base applications occupy more than half the PCs, and somewhat fewer use it for analyzing finances.

Despite the industry's overwhelming concentration on CAE, CAD, and CAM, only 30% of the respondents actively assign their PCs to

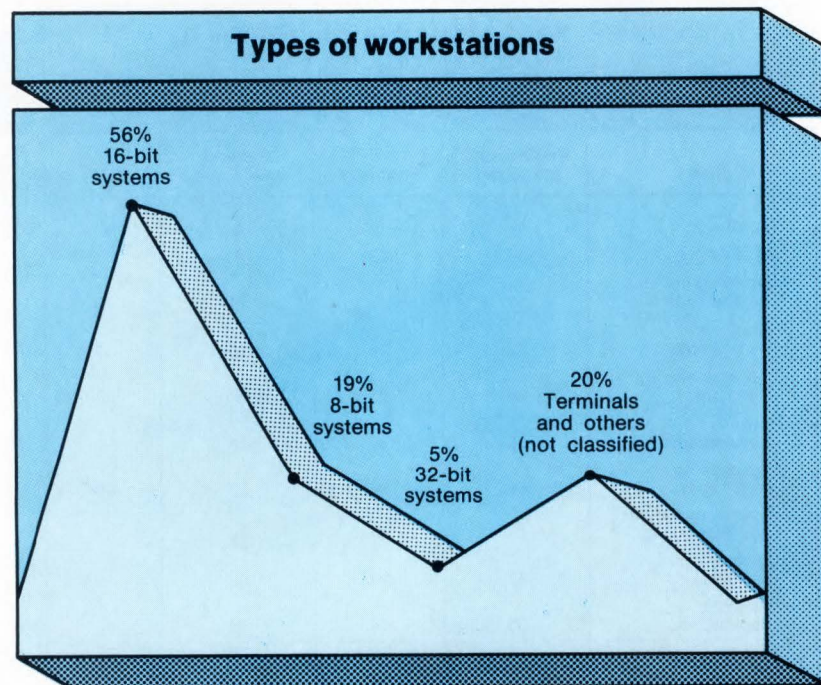
those tasks (Table 2), with testing and measurement garnering the most attention. Ironically, although 65% of those surveyed deal largely with design and development (50% engineering managers, 15% engineers), only 4% actually design chips on their

personal workstations. Half of those use the IBM PC or PC XT personal computer, and one makes do with an Apple IIe. Here again, engineers will be more likely to dive into chip and board design as 32-bit workstations emerge.

Pegging down exactly which type of personal computer they use at work, many engineers and engineering managers answered either ambiguously or not at all. Several name Hewlett-Packard or Digital Equipment, despite the fact that both companies produce a variety of terminals and computers. Five readers even work on home-made models.

Not unexpectedly, the IBM personal computers dominate, with 32%; the HP 150 is the system of choice for 4%, and Texas Instruments' personal computer is used by 2%. Other 16-bit systems constitute another 4%. All told, 42% of the respondents own 16-bit workstations, and 14% employ 8 bitters. The latter break down into Apples (5%), TRS-80s (3%), and others (6%). Individual systems with 32-bit CPUs account for only 4% of the total, with Apple's Lisa and Macintosh computers composing two-thirds of that figure and Apollo, Cadmus, and Sun computers composing the other third. The remainder of all re-

Figure 8



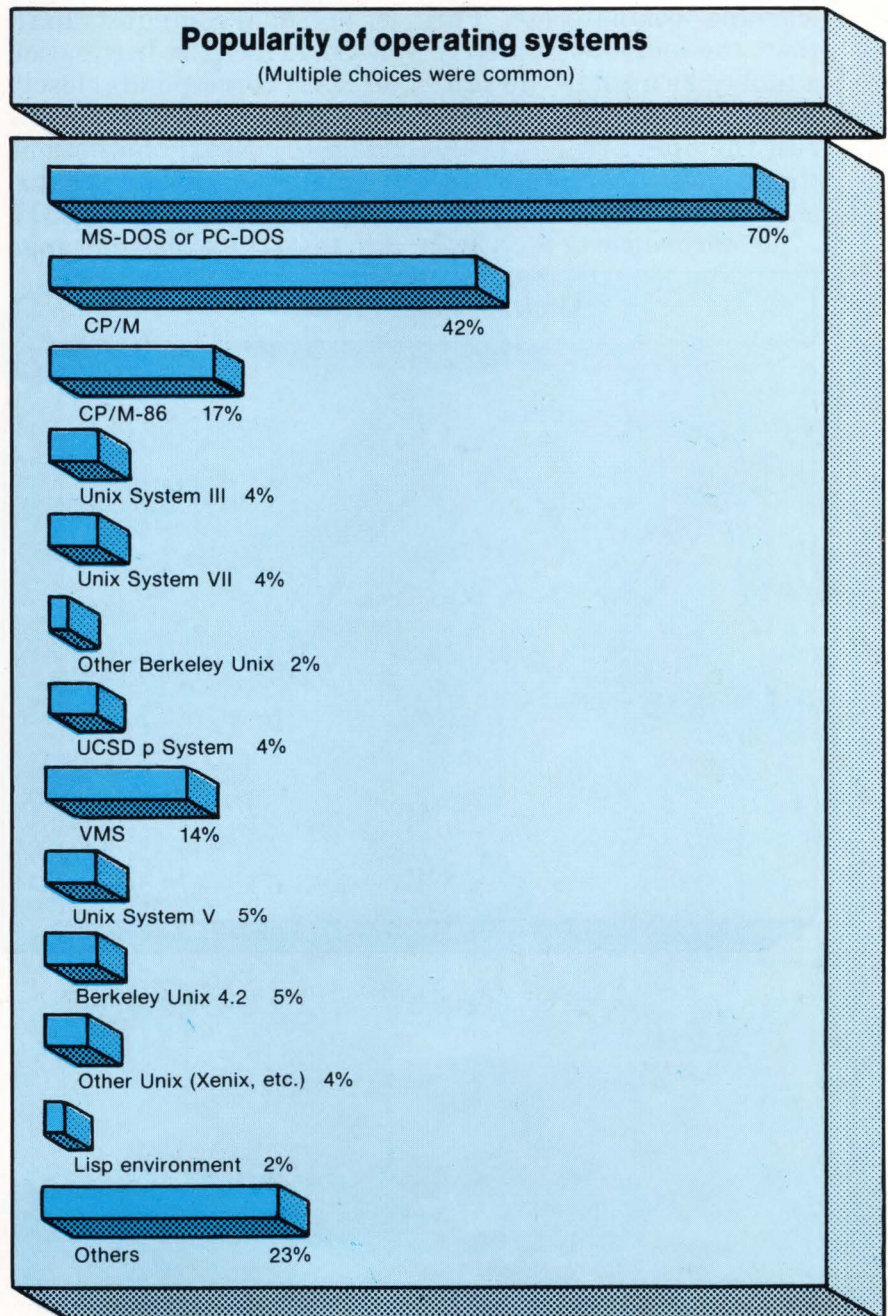
sponses lists their personal workstations as terminals or remote-entry stations on time-shared computers.

Rules of the computer

Operating systems are becoming machine-independent in that the popular ones are now available for a broad range of computers, and many computers can be run with a wide variety of operating systems (Fig. 9). Given the popularity of the IBM computers and their look-alikes, PC-DOS and MS-DOS are understandably used by 70% of the respondents. (In fact, the IBM PC can run under at least six operating systems.) Trailing those Microsoft systems are Digital Research's CP/M (42%) and CP/M-86 (17%) and Digital Equipment's VMS (14%). AT&T's Unix systems and the versions enhanced by the University of California at Berkeley run 4% to 5% of the computers. (Unix users tend to run several if not all versions.) The p System, developed by the University of California at San Diego, runs 4% of the computers. The Lisp environment is favored by 2%, and 23% employ other operating systems.

Although many engineers and engineering managers avail themselves of several operating systems, others do

Figure 9



PERSONAL COMPUTER SERIES



not want to be bothered by learning "computerese." For them the computer is merely a tool to be used in the simplest manner; those people run the operating system that comes with the system, as long as it is easy to run.

Memory capacity is critical

to engineering, but the smaller personal computers limit RAM. In fact, the distribution of RAM corresponds closely to the type of workstations (Fig. 10). Nearly half of our readers peg their workstation's RAM at 128 to 512 kbytes—the expected range

for 16-bit systems. Another 20% tag their RAM at 64 kbytes, an appropriate level for 8-bit machines. The leaders of the PC movement are those 4% with more than 2.5 Mbytes of RAM associated with their workstation.

The high-capacity, attractively priced disk drives introduced over the past few years have greatly enhanced the value of microcomputers (Fig. 11). For instance, 7% of the readers boast truly massive storage of more than 100 Mbytes, and about 40% indicate that their workstation has access to 2 to 50 Mbytes—the range associated with Winchester disk drives. Another 45% specify 1 Mbyte or less, which is considered about average for two floppy disks.

Despite the inherent usefulness of most personal workstations, engineers and engineering managers cannot help but add or purchase new features for their systems. In general, those with management responsibilities have slightly better equipped systems than pure engineers. Rank has its privileges.

The most popular enhancement, a communication hook-up, extends the user's reach: 56% talk to other systems by telephone, and 29% tie into local networks. Even with the broad scope of current sys-

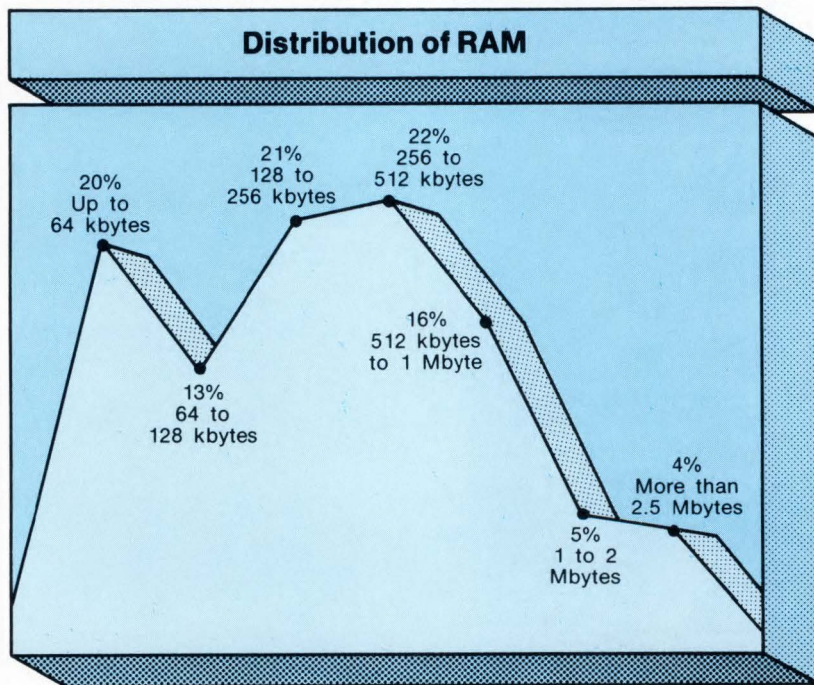
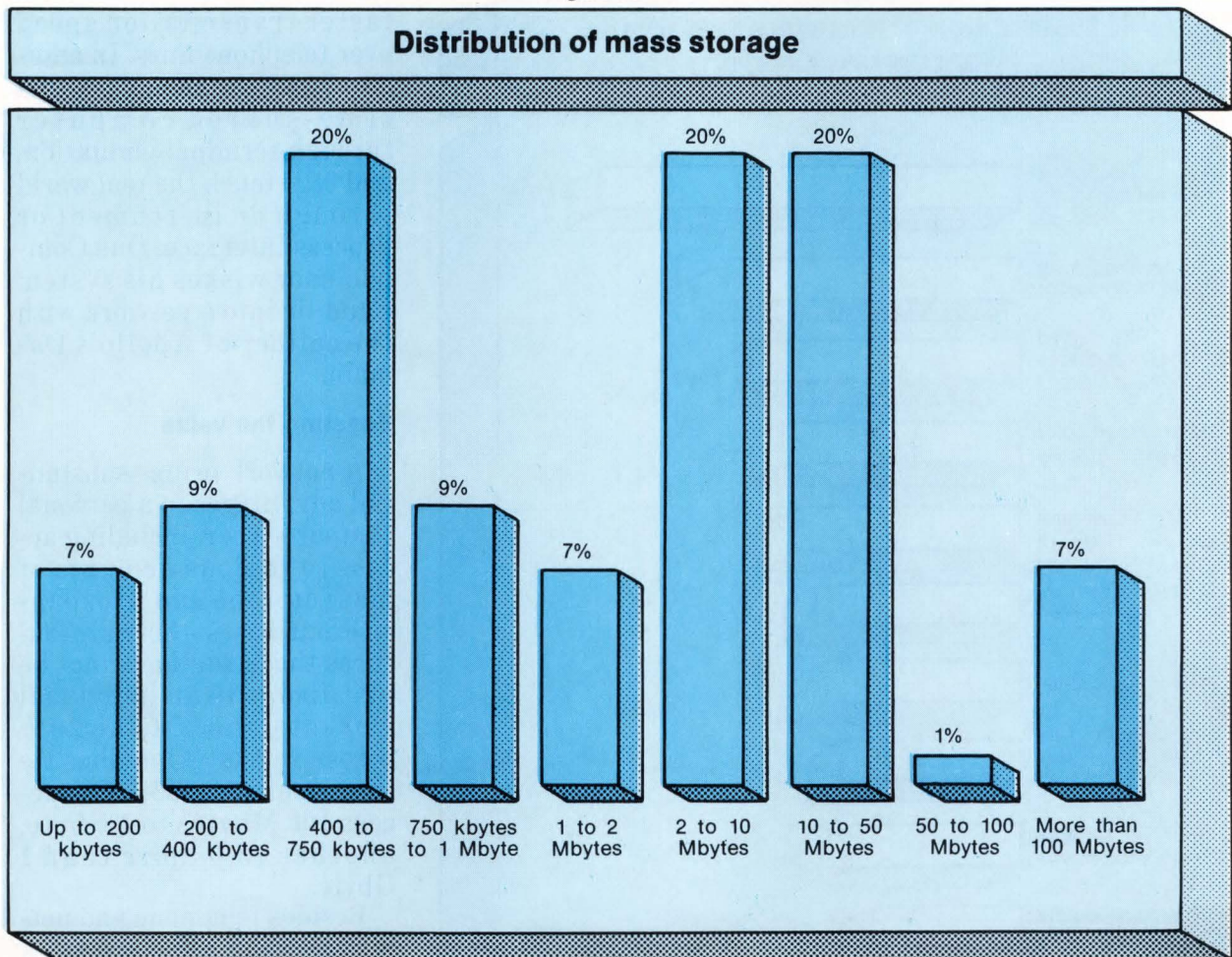


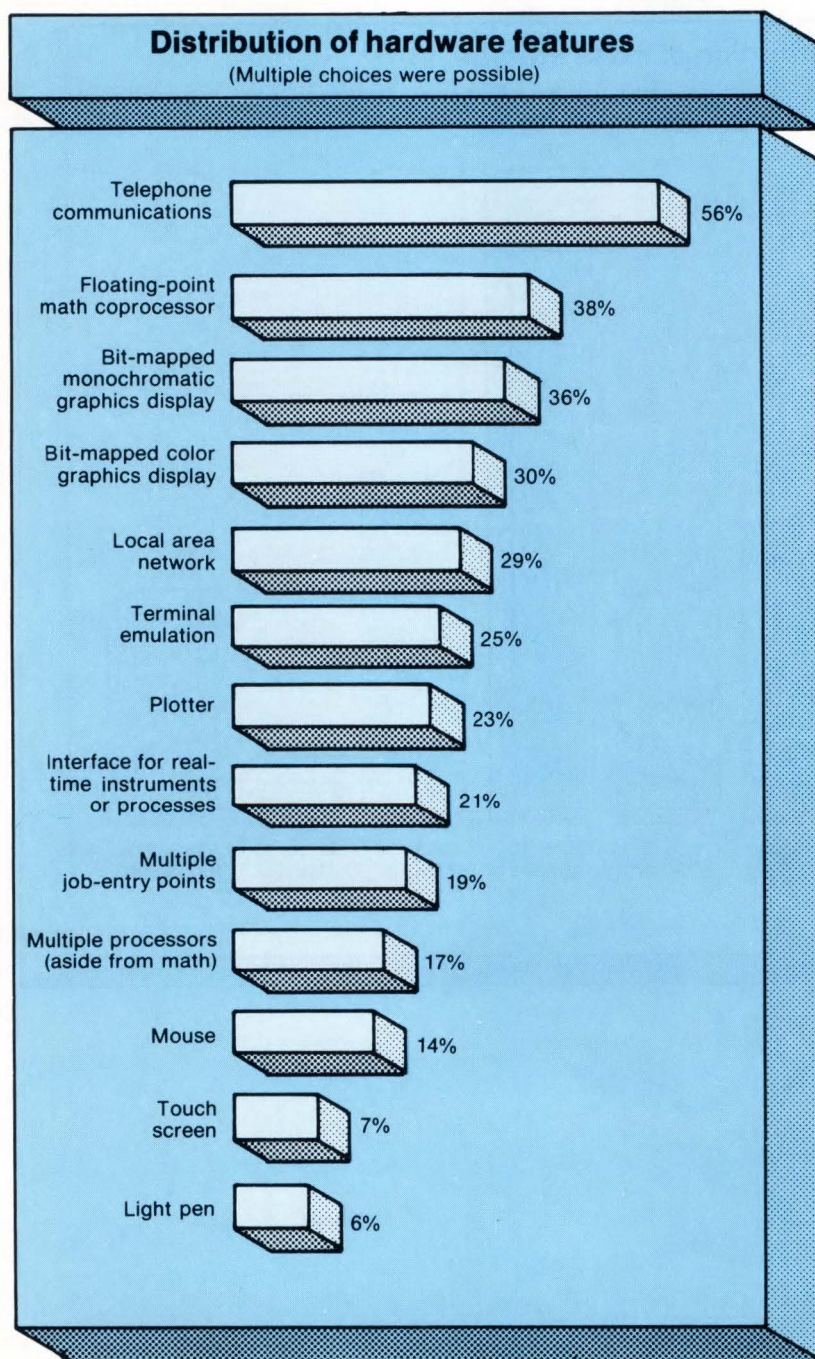
Figure 11



PERSONAL COMPUTER SERIES



Figure 12



tems, respondents demand faster transmission speed over telephone lines. In addition, 25% have access to a time-shared computer through terminal emulation, and 21% touch the real world through an instrument or process interface. One Compaq user wishes his system could tie into a network with the caliber of Apollo's Domain.

Boosting the value

A network brings substantial advantages to a personal computer user, including access to copious amounts of mass storage and to expansive data bases—both are features that usually cannot be justified with an individual workstation. Of the 29% whose workstation does tie into a network, 23% can access 100 Mbytes to 1 Gbyte, another 13% more than 1 Gbyte.

Besides telephone and network enhancements, a healthy number of workstations (38%) are equipped with a floating-point math coprocessor. Surprisingly, engineering managers are more likely than engineers to have the math chip by three to two.

About two-thirds of the readers use a high-resolution, bit-mapped graphics display—36% monochromatic, 30% color. Many users feel

READER SURVEY

that the displays need improvements though, especially over the graphics capabilities featured in IBM PC-like computers. More sophisticated graphics will prompt greater numbers of engineers to attempt CAE/CAD jobs on their workstations.

As for producing hard copies of what they see on the screen, most engineers attach printers primarily and then plotters; the latter are included on almost 23% of the systems (Fig. 12). Light pens and graphics tablets, which have been around awhile, have not yet caught on, but the mouse and the touch-sensitive screen may still find a following, despite the fact that a touch screen is neither a standard peripheral nor easy to add.

Many multiples

Rounding out the hardware configuration, 19% of the engineers and engineering managers work on a computer having more than one terminal, and 21% on a computer that accommodates multiple users. Here again, job responsibilities enter the picture (Table 3). Engineers with no management duties are most likely to use such systems, whereas general managers are least likely. Engineering managers work with the systems at a rate

slightly beneath the population as a whole.

Our readers are also enjoying the most sophisticated software (Fig. 13). Nearly a quarter of them benefit from multitasking software, 21% from windowing, and 15% from programs that allow them to cut and paste or

transfer data between windows. The multitasking "environment" is handled partially by Apple's Macintosh and completely by many enhanced Unix systems; developers are now trying to bestow the capabilities on MS-DOS. Again, these statistics may not go up until

Table 3. Distribution of workstation hardware features by job function (%)

Feature	Engineering managers	Engineers	General managers	Total
Floating-point math coprocessor	41	26	38	38
Multiple processors	16	20	17	17
Monochromatic graphics	35	34	39	36
Color graphics	30	36	22	30
Local-area network	31	26	13	29
Telephone communications	54	62	61	56
Mouse	13	22	13	14
Light pen	5	8	9	6
Graphics tablet	5	10	9	6
Plotter	23	28	13	23
Touch screen	6	10	13	7
More than one job entry point	18	22	13	19
Interface with real-time instrument or control	22	20	13	21
Terminal emulation	24	24	35	25

PERSONAL COMPUTER SERIES



engineers trade their 8- and 16-bit machines for 32-bit workstations. Virtual memory is currently beyond the scope of most small workstations: Only 14% of the readers name it among their

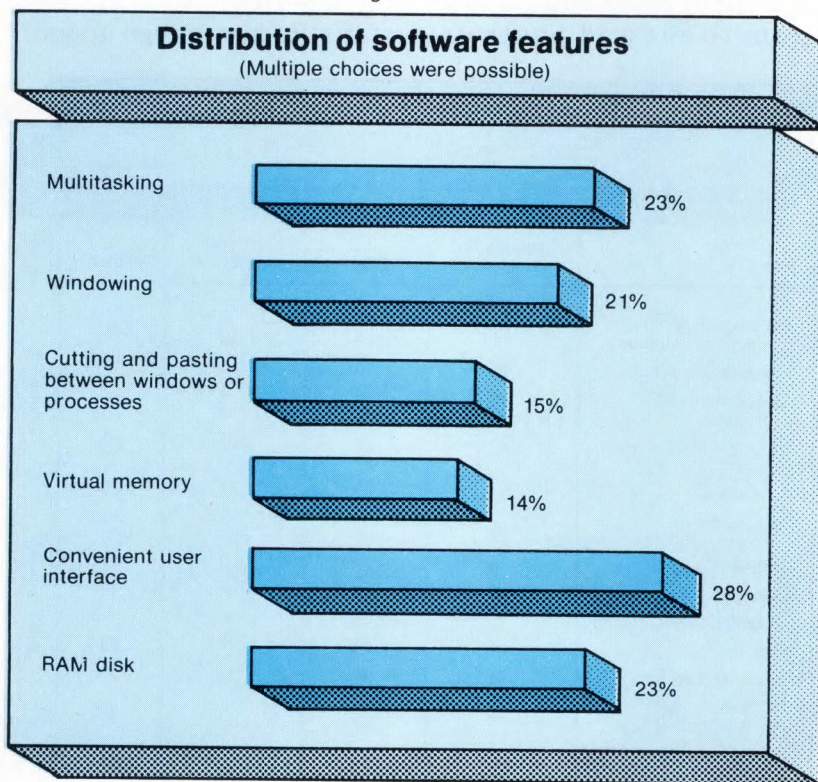
workstation's features. However, 23% can emulate disks in RAM—a trick well within the capacity of 16-bit systems, as well as many 8-bit systems.

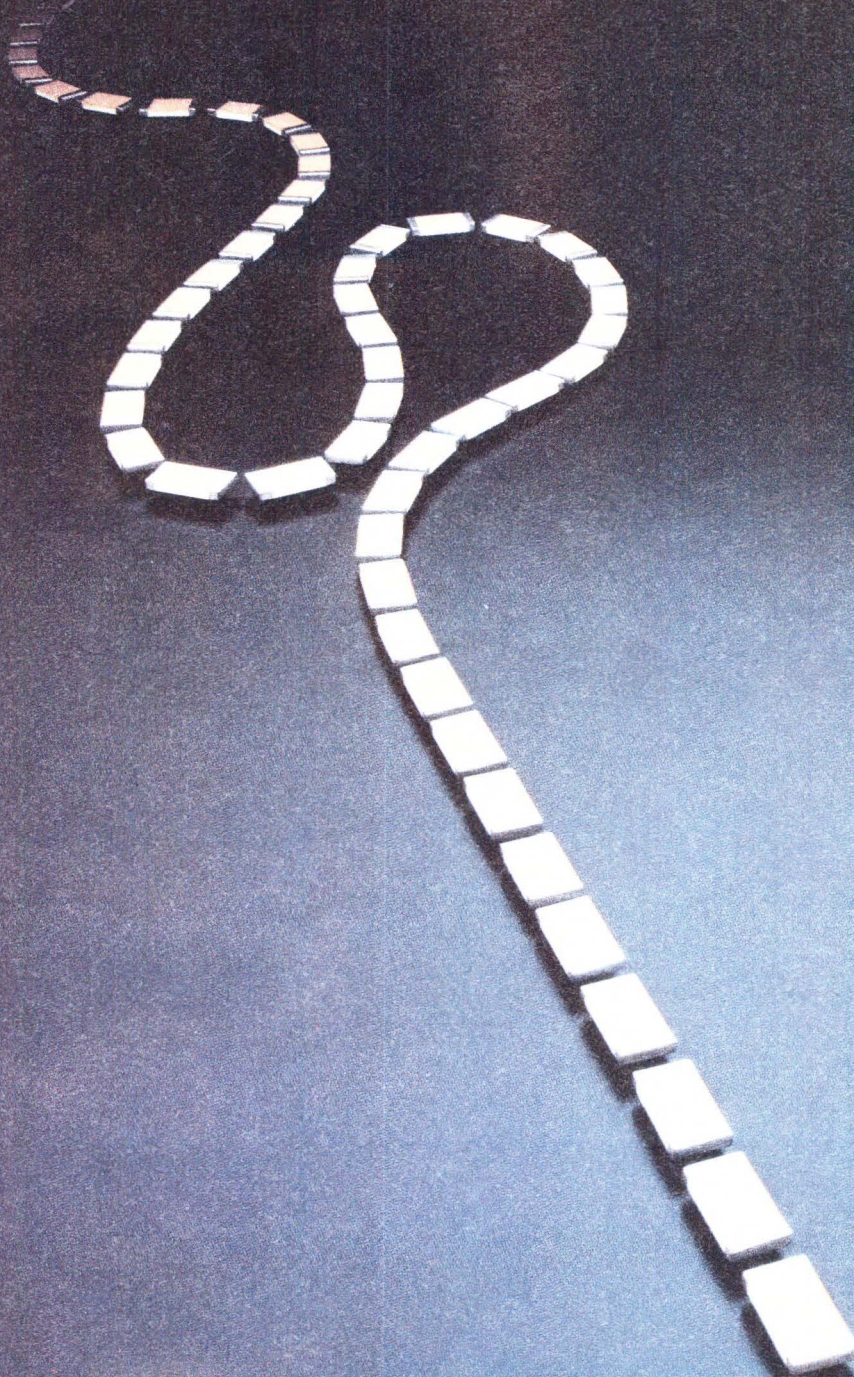
The user interface, as always, is a major source of con-

tention in the microcomputer world and among ELECTRONIC DESIGN readers. A full 63% feel that improvements are mandatory over the next five years. Currently 28% work on a system with a helpful user interface; the remainder had to learn the command structure of an operating system. The Macintosh's menu-driven, icon-oriented interface has made a tremendous impact on personal workstations, and software developers are busily developing imitation Macintosh shells for most popular OSs. Unix's menu-driven shells have been around for a while, and some PCs are just now incorporating MS-DOS shells. Nevertheless, many users feel that once they have learned the command structure of an operating system or an application program, the menu-driven shell gets in the way.

Not surprisingly, OEMs are gaining a solid foothold in engineering workstations, enhancing nearly 20% of the respondent's systems (Fig. 14). The actual manufacturer of the hardware or its distributor sells about 75%, and the rest were obtained from other sources, including home-built models. The majority of software comes from the system supplier, including the operating systems, 65% of the programming languages, and

Figure 13





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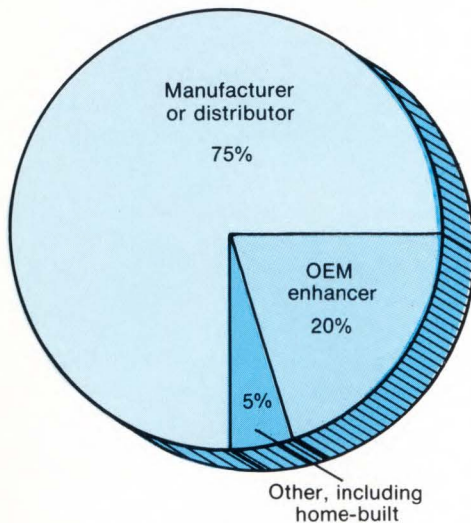
CIRCLE 75

PERSONAL COMPUTER SERIES



Figure 14

Source of systems



about half the graphics and word-processing programs. Interestingly, many readers state that they purchased their chip and board design software from the system supplier.

Roughly half the time, standard "business" software—word processing, data base, financial analysis, communications, and project scheduling and management—comes from third parties. As might be expected, job-related and engineering programs more often than not are developed in house, particularly packages for testing and measurement (69%), manufacturing and on-line control (64%), sundry engineering purposes (58%), and general job-related tasks

(55%). Except for the case of company-specific engineering applications, the hardware supplier is in an excellent position to develop software (Table 4).

Just imagine . . .

Sometimes we forget that products and developments introduced in these pages do not actually appear in the field for some time. Computer equipment especially tends to be announced long before production versions are ready to be shipped. More than three years ago IBM started delivering its personal computers, and now more than half our readers use them or

similar systems. With that in mind, it will probably be at least two years and most likely three before the latest generation of multiprocessor 32-bit workstations become fully entrenched in the graphics-intensive CAE environments for which they are designed.

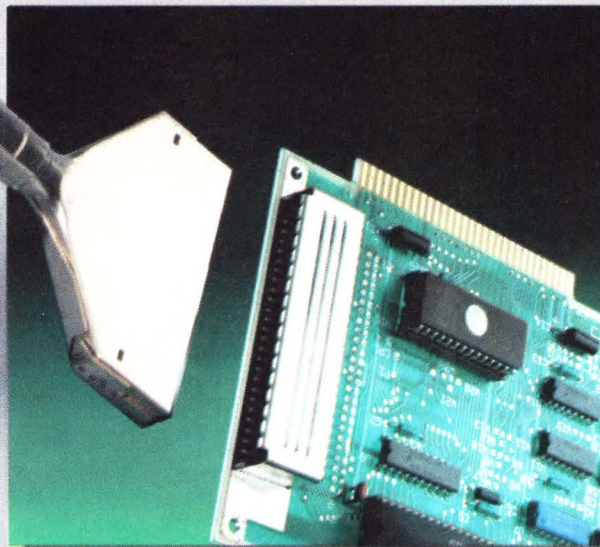
The prevalence of personal computers is undeniable. If those who say they plan to own a computer actually go out and buy one, only 3% of ELECTRONIC DESIGN'S readers—including the engineering managers, who constitute 80% of the respondents—will be left out of the personal computer movement. □

Table 4. Source of software (%)

Software	Hardware supplier	Third party	Developed in-house
Operating system	90	7	3
Programming languages	65	30	4
Communications	39	45	16
Graphics	52	32	16
Chip or board design	42	28	30
Manufacturing or on-line process control	22	14	64
Testing and measurement	15	16	69
Other engineering	16	26	58
Project management and scheduling	25	49	25
Financial analysis	32	49	19
Data base	36	51	13
Word processing	46	49	5
Other job-related software	22	23	55

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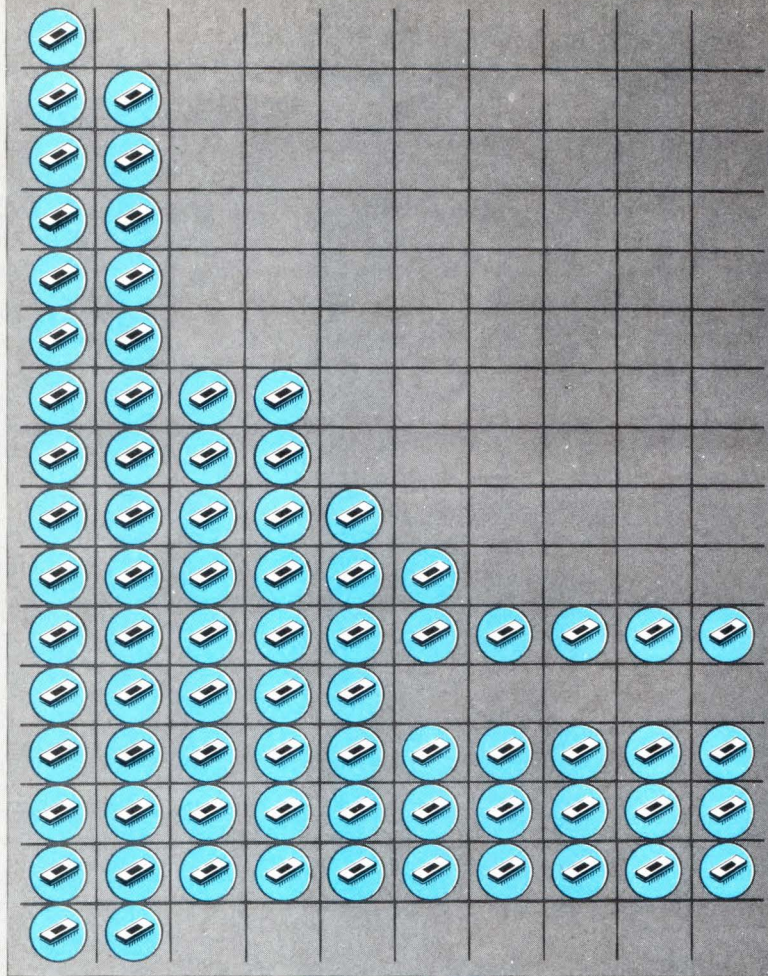
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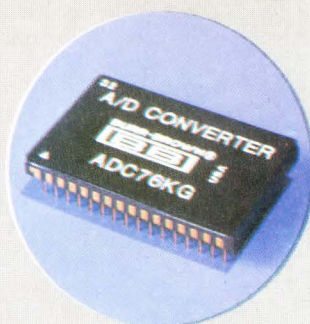
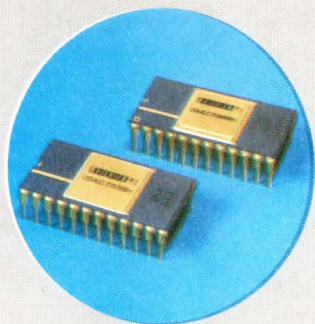
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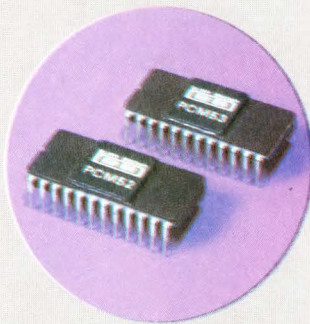
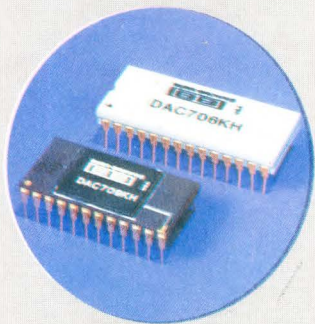
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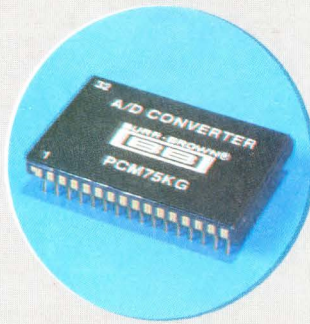
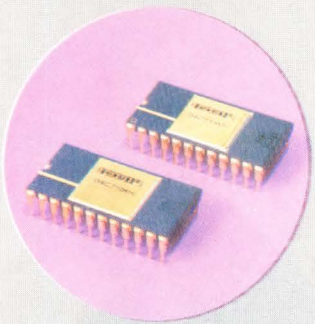
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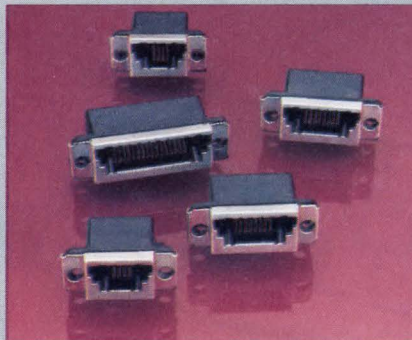
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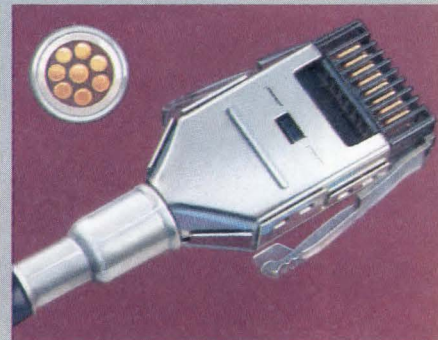
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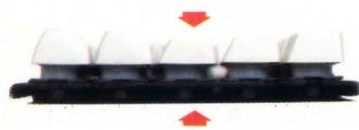
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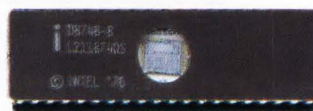
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DESIGN ENTRY

Monolithic color palette fills in the picture for high-speed graphics

The first color palette chip puts a staggering array of hues at a designer's fingertips almost instantly. To boot, it boasts its own video output.

The graphics color palette is one of several modular blocks for building flexible, high-resolution graphics systems (see the Design Entry, p. 203). Standing alone, it eases programming, overlays text on graphics, and coordinates video-sync and blanking pulses.

A picture today is worth more than the customary 1000 words. On a color graphics system, it could—in theory—easily need over 1 million 24-bit words. That is certainly the case when such a system resolves an image into 1024-by-1280 picture elements and assigns every one 256 gradations each of red, blue, and green, making for a total of 16.8 million possible hues.

The color palette approach cuts this overwhelming memory requirement down to a manageable size by making only a small subset of the full spectrum available at any one time. Now, a complete subsystem implementing this

technique for one color gun has been integrated onto a single chip.

Optimized for high-resolution color graphics systems, the Am8151 is essentially a 256-by-8-bit RAM plus an 8-bit digital-to-analog converter that is compatible with an RS-343-A video output. At any moment, three such chips yield no more than 256 out of 256³ possible colors. But

Steven B. Sidman and John C. Kuklewicz
Advanced Micro Devices Inc.

Steven B. Sidman is a manager in AMD's analog and interface product-planning department in Sunnyvale, Calif. Earlier, he designed high-speed test systems at GenRad/STI, and before that he worked as a staff scientist at Lawrence Berkeley Laboratory. He holds a BSEE from Tufts University.

John C. Kuklewicz, who works at Kaiser Electronics in San Jose, Calif., is a former member of AMD's technical staff in analog and interface product planning. He earned a BSEE from Worcester Polytechnic Institute.



Cover: Color palette chip

the host processor may rearrange the contents of each RAM at any time to create a different set of 256 colors (see "Portrait of a Color Palette," opposite). Each palette chip can be completely reloaded within 52 μ s (it needs 200 ns to load a byte), leaving ample processor time for handling an array of 1024 by 1280 picture elements.

For the host processor, the palette approach slashes software overhead; for the system designer, it makes writing software easier. From the point of view of the application programmer, it makes colors much easier to manipulate. Moreover, the chip can be used independently or as part of a four-member family of bit-mapped graphics system ICs.

In good company

Although similar color encoders exist as hybrid circuits, the palette chip is the first IC to combine a 256-byte color map, a low-glitch d-a converter, three pixel-data and two monitor-control pipeline registers, a voltage reference, and all monitor control signals on a single chip (Fig. 1). In fact, it stands in for two 256-by-4-bit ECL RAMs, four 6-bit ECL registers, an 8-bit d-a converter and voltage reference, and various logic elements. That is just part of the picture; it also replaces 32 termination resistors (in single in-line packages) and a monitor-control IC.

More than simply cutting parts count, the chip also holds down the number of connections that must be made. These can become troublesome at high frequencies. Further, the IC's internal pipeline registers serve as buffers along its internal data paths. That arrangement relaxes the timing requirements for incoming signals and eliminates the need for external delay elements. The chip runs on a 103-MHz clock and delivers color to 60-Hz, non-interlaced displays of 1024-by-1280-pixel arrays. Separate controls allow text to overlay any graphics.

Timely interfacing

Internally, the chip's pipelined architecture simplifies the task of linking to its primary input, the color-map RAM, and its output, the d-a converter. A map-address register, for instance, holds pixel data—actually an address that is sent from the frame buffer. By storing

the address, the register leaves most of the system clock cycle for generating the next address. Similarly, a color-data register holds the map's output and eases speed constraints on both the memory access time and the d-a converter's decoding circuitry. The d-a decoding register stores the converter's decoded input and deskews it, consequently helping reduce output glitches. Lastly, all monitor-control signals—High Sync (HSYNC), Vertical Sync (VSYNC), Blank, Overlay (OVLY), and White or Black (W/B)—are also loaded into registers to keep them synchronized with the Map Address inputs. Thus no external delay elements are needed for that purpose.

The fact that video-frequency inputs can handle either ECL or TTL also helps the input interface. One signal, LC (Level Change) actually controls the input threshold: when it is at +5 V dc, the inputs accept TTL; when it is at ground, the inputs work with 10K ECL. When set for the second, the inputs lend themselves to wired-OR multiplexing, which simplifies the interface over which the host processor changes the chip's color map. The signals that can switch between TTL and ECL thresholds are Map Address, OVLY, W/B, CLK and CLK.

Framing the picture

In normal operation, the palette chip either refreshes or updates the display with data (actually, indirect addresses) from the frame buffer. The buffer's parallel data is serialized before it is fed to the chip from a bank of video shift registers. The information enters through the Map Address inputs PD₀-PD₇ and accesses the 256-byte color map. Subsequently, the map's contents are applied to the d-a converter, which in turn produces an output for driving a CRT monitor.

Before generating the colors indicated by a bit-mapped frame buffer, the chip has to be loaded with a color map. To do so, the host processor must address the map, write new data, and possibly verify the entry.

The host loads and reads the color map through the graphics chip's bidirectional Color Data pins, which are controlled by the I/O and Enable (EN) inputs. When EN is high, the data path is disabled and the pins remain in a high-impedance state. That makes it possible to con-

Portrait of a color palette

Digital color palettes, sometimes called palette mixers or encoders, simplify the problems involved in managing the massive number of color combinations and the associated memory space found in high-performance bit-mapped graphics systems. Typical examples are engineering workstations and image-processing equipment.

A raster-scanned display composes images out of picture elements of different relative intensities, or brightnesses. A digital word N bits long defines the brightness of each pixel, and a frame buffer N memory planes deep stores each word in accordance with each pixel's position in the display. (Every memory plane mirrors the organization of the pixel array.)

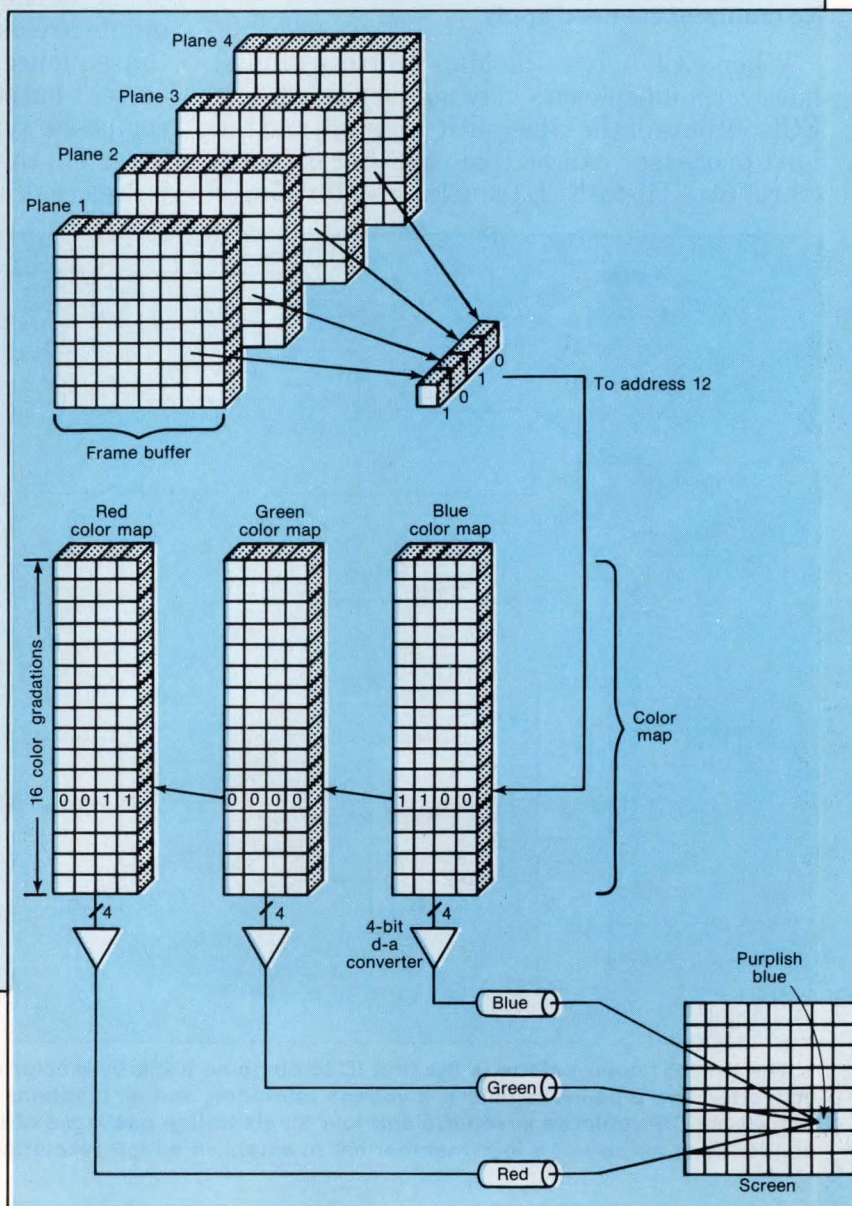
For a color system, each pixel requires at least three N -bit words, since three color guns contribute to each pixel's overall hue and intensity. Given an array of 1024 by 1024 pixels, each described by, say, three 8-bit words, the requisite 24 million bits of memory would be impossible for the host processor to manage.

A color palette—actually a look-up table stored in RAM—both eases the host's task and cuts the amount of memory needed in the frame buffer. At any one time, the RAM is capable of mapping all the gradations possible for each of the three primary colors. Consequently, instead of storing these color intensities directly, the frame buffer is free to store merely their locations within the color map. Each address points to the set of three red, blue, and

green intensities that describe the color of a given pixel (see the figure). Thus color palettes are a form of indirect addressing.

A major advantage of this approach is that it alleviates the chore of changing colors because the system's host processor must write each color change to only one address in the palette. Its chief limitation is that it restricts

the number of colors available to the display at any one time to a single set of red, blue, and green combinations—in other words, to the cube root of the entire spectrum of possible combinations. But the system's host processor can change the assortment of color intensities in the map, making the entire spectrum available at different times.



Cover: Color palette chip

nect the Color Data pins directly to the host's data bus.

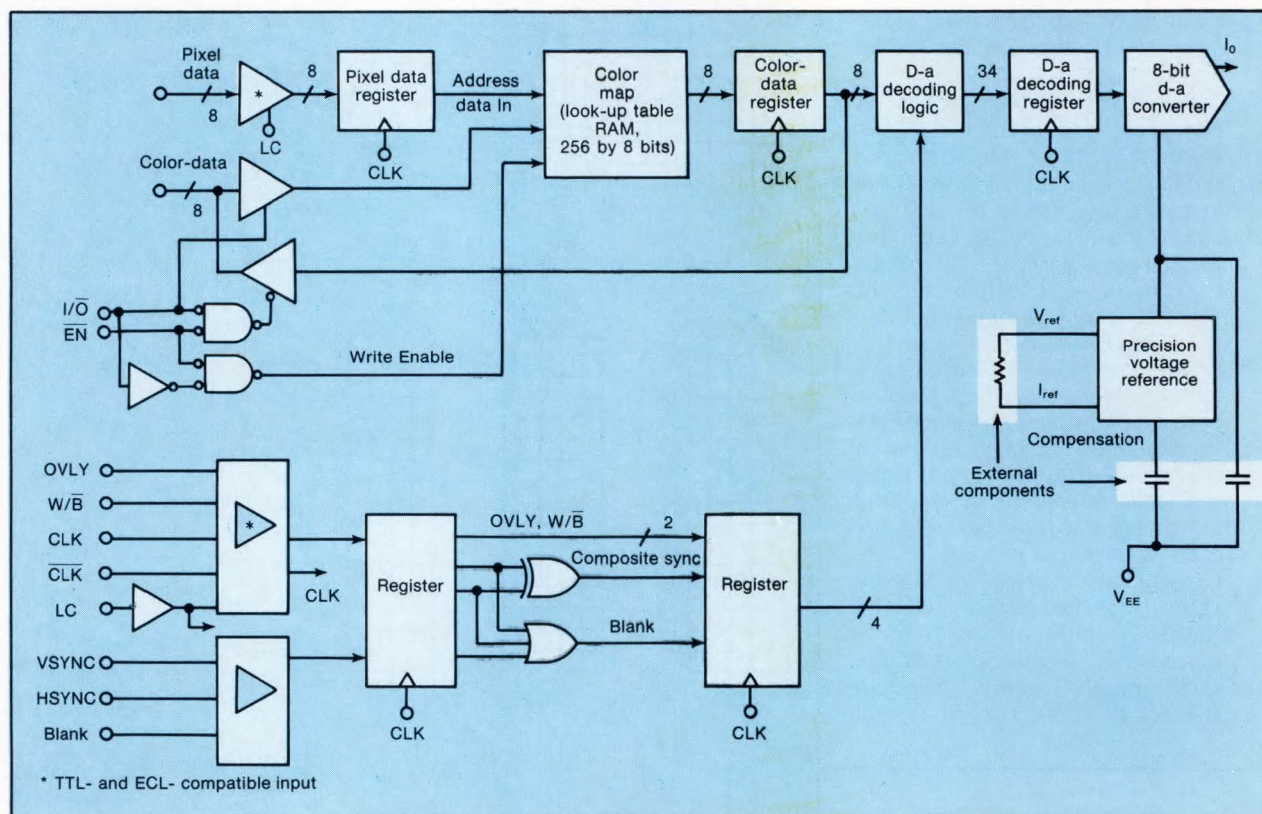
The processor selects bytes contained within the color map, singly or sequentially, by placing addresses on the chip's Map Address inputs (also referred to as Pixel Data inputs) and asserting the I/O and EN signals. Because the address inputs are also driven by the frame buffer (through the video shift registers), they must be multiplexed between the buffer and the processor to refresh and update the display. A bank of eight 2-to-1 TTL-level multiplexers is sufficient for that chore.

No multiplexers need apply

When ECL drives the Map Address inputs, however, multiplexers may not be needed. The ECL outputs of the video shift registers and the host processor can be tied together directly (through TTL-to-ECL translators), forming a

wired-OR connection. Then, when the processor accesses the color map, it is only necessary that the outputs of the video shift registers be at a logic low. Conversely, when the frame buffer is addressing the map, the processor's translators must stay low. No matter how the processor enters the color map or for what purpose, the selected locations will be displayed unless the chip's Sync or Blank inputs are asserted.

The chip's HYSNC AND VSYNC inputs cause the converter's output to assume the proper voltage levels for synchronizing or blanking the display's sweep (Fig. 2). The two inputs are exclusive-ORed within the chip. In consequence, when either goes high, the converter's output is unconditionally driven to the composite sync level. But when both inputs are asserted, the horizontal sync pulses generate pulses that alternate between sync and blank



1. The Am8151 color palette is the first IC to combine a 256-byte color map, a low-glitch digital-to-analog converter, five pipeline registers, a voltage reference, and all functions for controlling a color CRT monitor. The 40-pin DIP replaces seven ICs and four single in-line packages of pull-up resistors. It can be used independently or as part of a four-member set to establish a high-resolution bit-mapped graphics system.

levels during the vertical retrace period, keeping the horizontal oscillator locked into its proper frequency. Asserting the chip's Blank input forces the converter's output down to the blank signal line level. That occurs regardless of all other inputs, except when HYSNC and VSYNC are driving the output to the still lower sync level.

Whiter than white

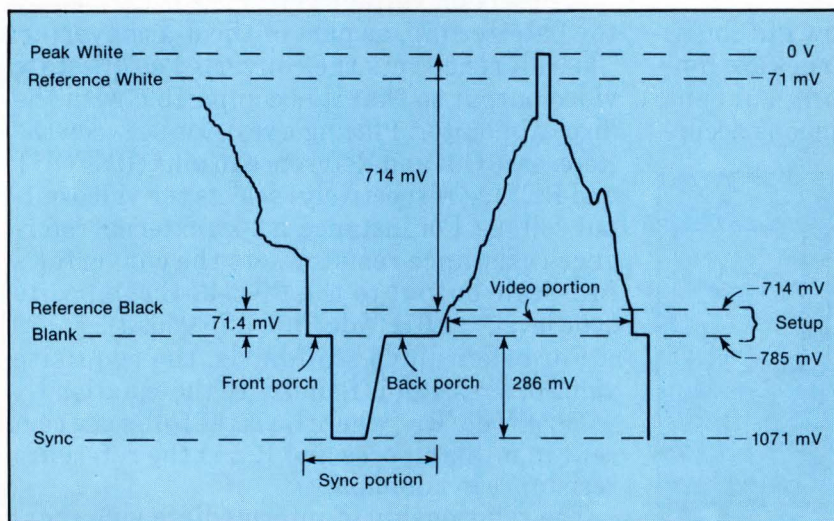
The OVLY and $W/\bar{B}$ inputs overlay text onto graphics. When both are high, the graphics chip's output is driven to peak white, a condition that is 10% whiter than the reference value and allows white text to be written over white graphics. When three palette chips are configured in a RGB system, it is possible to write text over graphics in eight colors by supply independent $W/\bar{B}$ lines for each chip (Fig. 3).

Invoking an overlay allows other video

sources to be multiplexed onto the display because the chip's output in the peak white condition is 0 V dc, which corresponds to a high-impedance state. As a result, when the palette is operating in this condition, another source can drive the monitor with no interference.

When changing colors, it is possible to load a single word into the color map in about 200 ns. It can be read back in 110. Thus all three chips in a color system can be loaded in less than 160 μ s and read back in 90. If the host processor can carry out the necessary 768 writes and an equal number of reads rapidly enough, the entire color map can be altered and verified during the vertical retrace time—approximately 1.5 ms.

Transfers that involve the color map must take into account the chip's pipeline registers. Reading from or writing to the map does not instantly change the displayed image because the pipelines delay the processing of individual



2. The palette chip conforms to video standard RS-343-C and even has a peak white level for superimposing white text on white graphics. It contains a nearly glitch-free d-a converter that produces the video output waveform by sourcing current into a reference resistance. The resistance also sets the voltage for black and white reference levels, blanking, and setup. (The last is the difference between the blank and black reference levels).

Cover: Color palette chip

colors by three clock cycles. For the same reason, it takes two clock cycles to load an initial byte into the color map. Once the pipeline is filled, through, successive changes occur like DMA transfers: one byte to a clock cycle.

An 8-bit d-a converter links the palette to a video monitor. The latter is designed to minimize output glitches and eliminates the need for deglitching circuitry. Glitch energy is kept to 50 pV-s or less by segmenting the converter into two separate, but matched, d-a converters. One accepts the four most significant input bits; the other receives the four least significant bits. The full-scale output of the second d-a converter is $1/16$ of the full-scale output of the first d-a converter. Importantly, each converter is decoded, which means that instead of the four binary-weighted current sources that are found in most d-a designs, each of the palette's two converters contains 15 equal sources—one for each analog output increment.

The converters feature such low glitch energy because internal current changes are limited to either opening or closing current sources, and exclude the simultaneous occur-

rence of both. In contrast, binary-weighted converters attempt to switch on some currents as others are turned off. When skewed, these opposite current switches can cause a converter's worst glitches. What's more, the weighted currents create glitches in proportion to their weight, up to $1/2$ MSB. The two decoded converters, however, never switch a current larger than $1/16$ of the full-scale output.

The converter's output also settles quickly, within 12 ns, contributing to the graphics chip's high speed. Its dual-decoded architecture, bipolar process, and careful layout not only help it settle quickly but also further limit glitch energy. Also, for short paths the converter's current output can directly drive low-impedance loads (50- or 75- Ω), eliminating the need for a buffer.

On-board reference

A precision voltage reference is carried by the palette chip, as part of the d-a converter. The reference sets the converter's full-scale video output so that it is compatible with the display monitor. Placing a resistor between the Reference Out and Reference In pins (REFOUT and REFIN, respectively) selects the video output voltage. For instance, a 2-k Ω external reference resistance resistor sets the converter's full-scale output to the RS-343-C composite sync level, -1.071 V dc (into a 75 Ω load).

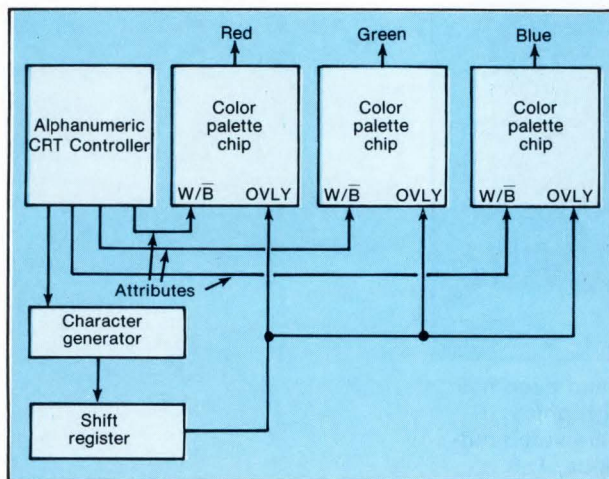
For other video standards, the requisite value of a resistor is found with the equation $I_{FS} = 28.56 \text{ V dc} / R_{ref}$, where I_{FS} is the full-scale current in milliamperes and R_{ref} is the reference resistance in kilohms.

The relationship of intermediate video currents to I_{FS} and R_{ref} hinges on two facts: I_{FS} corresponds to the composite sync level, and the chip resolves the video signal between reference white and reference black into 256 equal steps. For that reason, other important currents are:

- reference white, $I_{REFWHT} = 1.7556 \text{ V dc} / R_{ref}$
- reference black, $I_{REFBLK} = 17.676 \text{ V dc} / R_{ref}$
- blanking, $I_{blank} = 19.421 \text{ V dc} / R_{ref}$
- setup, $I_{setup} = 1.7556 \text{ V dc} / R_{ref}$

The last current, I_{setup} , is the difference between the blank and the reference black levels.

The precision voltage source's Reference In



3. The OVLY and W/B inputs are the keys to the palette's ability to superimpose text on graphics. When OVLY is asserted, a high on the W/B input generates a 10% "overwhite" that writes white text against a white background. In a three-gun color system, keeping the three W/B lines independent furnishes a total of eight possible colors for the superimposed text.

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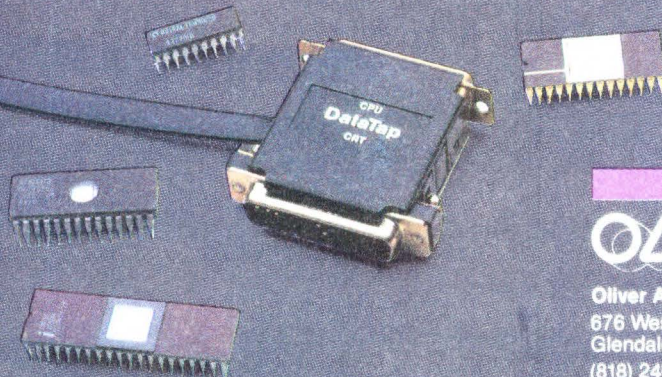
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Cover: Color palette chip

and Reference Out pins also enable several palette chips to be linked to the same reference. In doing so, a designer can better match the color intensities among all of the chips. Specifically, the REFOUT of one palette chip may be used to drive the REFIN of two other chips. Because the absolute gain of each palette's d-a converter is within 1% of its setting, the full-scale outputs of any three converters driven from the same reference will match each other to within 2% (excluding mismatches caused by other current-setting or load resistors).

Bit mapped and blocked out

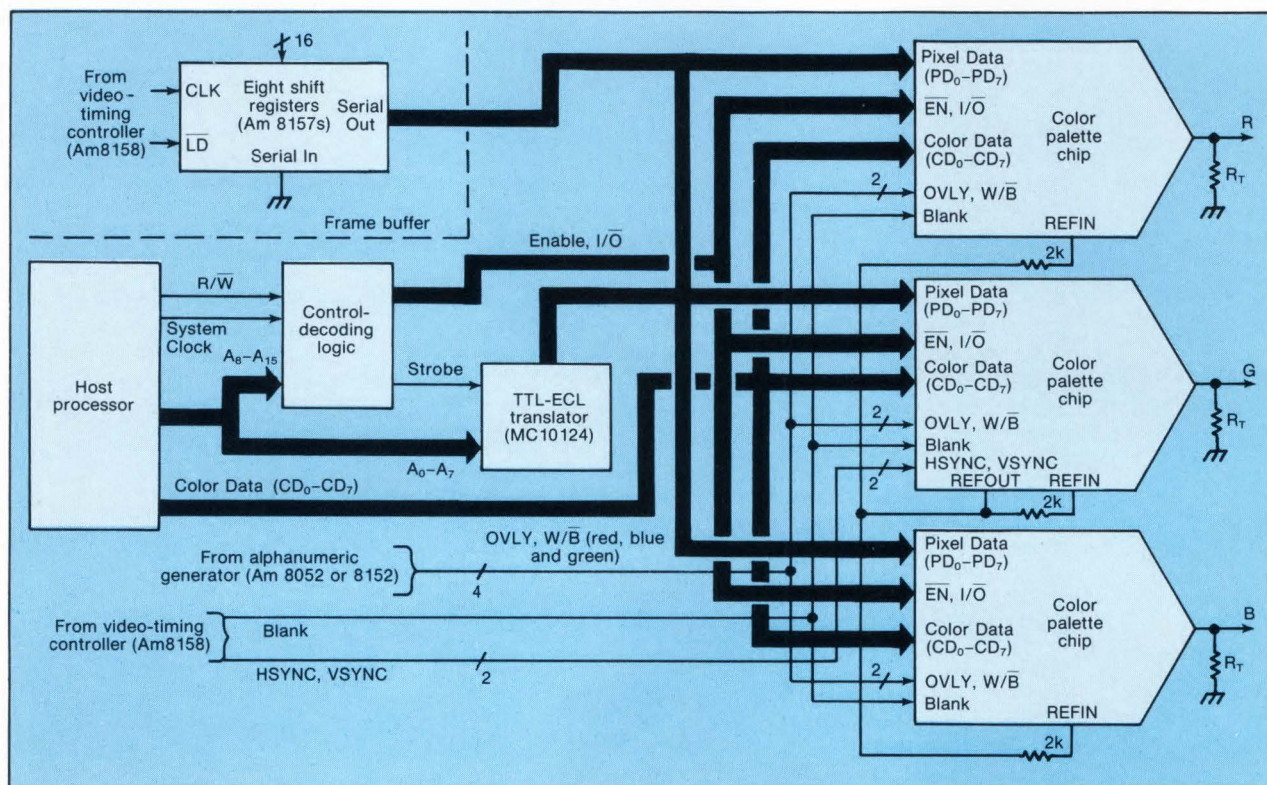
A simplified block diagram of a bit-mapped graphics system is an easy way to show the signal paths leading to the palette chip (Fig. 4). In the circuit, a wired-OR handles the multiplexing that lets the host processor (through the aforementioned TTL-ECL translators) and the frame buffer (through eight video shift registers) share access to each palette's Memory

Address inputs.

Since the video shift registers work in conjunction with the other members of the graphics chip family, the register's outputs can be made low whenever a video timing controller asserts the Blank signal. That sequence of operations prevents the shift registers from being updated during the retrace intervals. Consequently, the host processor can address the color map during these intervals, allowing the user to change or check the available colors without the monitor showing any disturbance.

Part of the overall system, a control-decoding block, generates a common strobe for all TTL-ECL translators from the processor's Read and Write lines, system clock, and high-order address bits. Here, the translators are set up so that a low on the strobe line forces the ECL outputs low.

The decoding block also drives the $\overline{EN}$ and I/O palette-state control signals. The bidirectional Color Data Lines from all three palettes



4. In a simplified block diagram of a color bit-mapped graphics system, a host processor (through TTL-ECL translators) and a frame buffer (through video shift registers) are wire-ORed to three palette chips. To avoid disrupting the display, the chip's color maps can be loaded or changed while the color gun is vertically re-tracing its beam. One palette drives each gun.

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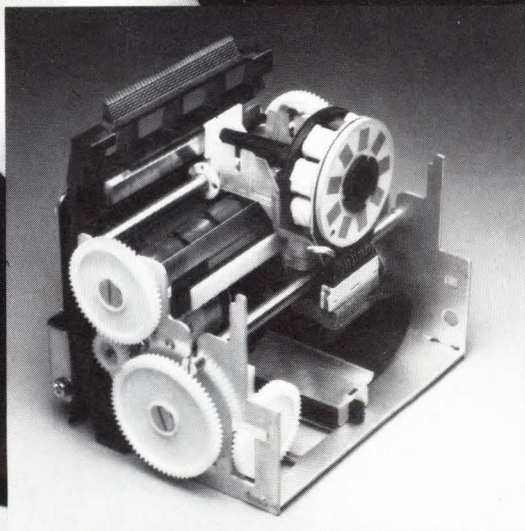
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Cover: Color palette chip

are connected directly to the host processor's data bus.

A video-timing controller generates the Blank, VSYNC, and HSYNC monitor-control signals and transmits them to the monitor through the palette. In most monitors, composite sync information is decoded from only the green channel because just one set of sync pulses is needed. Blanking information, on the other hand, goes to all three color channels. An alphanumeric CRT controller subsystem supplies the OVLY and W/B inputs to the palette.

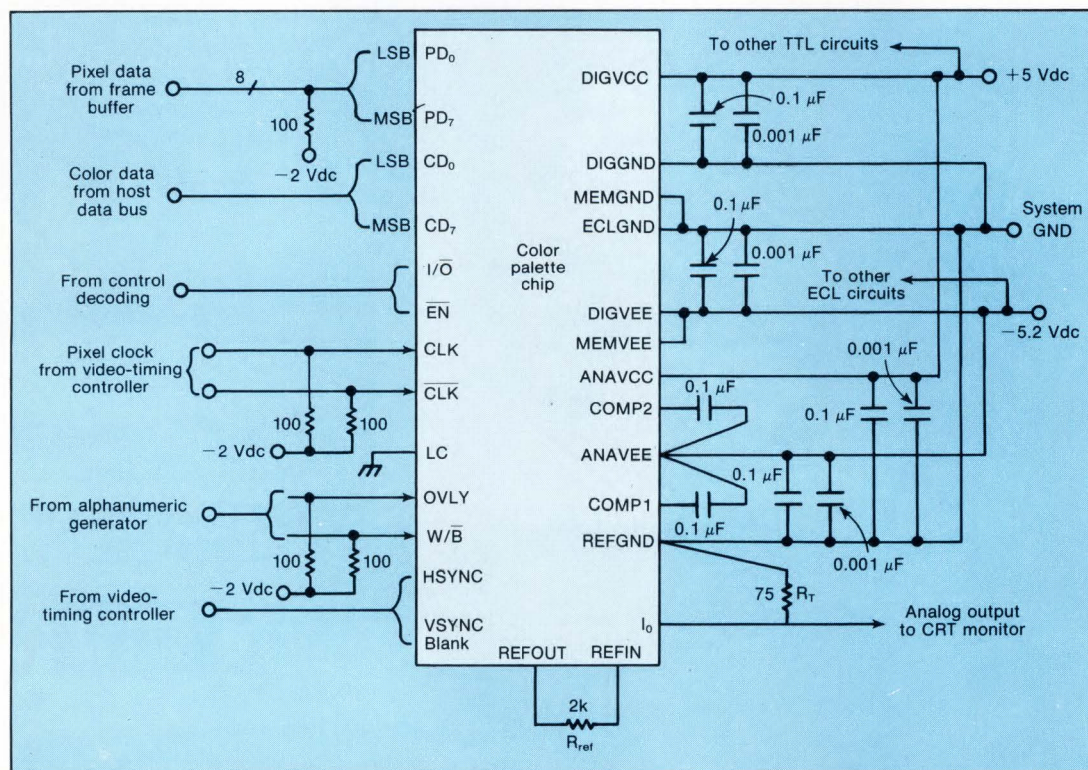
Because of the palette's high speed, care must be exercised when linking it to surrounding circuitry. To this end, the chip has several different ground and power connections to help limit the effects of noise. There are four ground pins: one each for TTL digital (DIGGND), ECL (ECLGND), memory (MEMGND), and reference (REFGND) circuits. The first should be tied to the ground point used by all TTL circuits on the board. ECLGND and MEMGND should be con-

nected at the chip and then to the board's ECL ground point. And REFGND should be joined to the ground system as close as possible to the analog V_{EE} supply point, ANAVEE, to minimize noise from digital ground currents. A good point of connection is where the ground systems are brought onto the board.

Power points

A typical pin-by-pin hookup for ECL-compatible inputs (Fig. 5) is quite similar to that used for TTL-compatible inputs. With the latter, the LC input would be tied to +5 V dc at the digital V_{CC} pin, DIGVCC, instead of to ground. Further, the 100- Ω resistors terminating at -2 V dc would be eliminated, and the CLK input would be tied to the digital ground point.

To minimize noise, DIGVCC is linked to 5 V dc and can share a common connection with other TTL circuits on the same board. But the analog V_{CC} input, ANAVCC, should be con-



5. The palette's 103-MHz speed demands that a designer pay special attention to minimizing noise, especially from ground loops. The power pins for TTL (DIGVCC), memory (MEMVEE), and analog (ANAVEE and ANAVCC) supplies are at the right. Individual pins are used for TTL, ECL, memory, and voltage-reference resistance.



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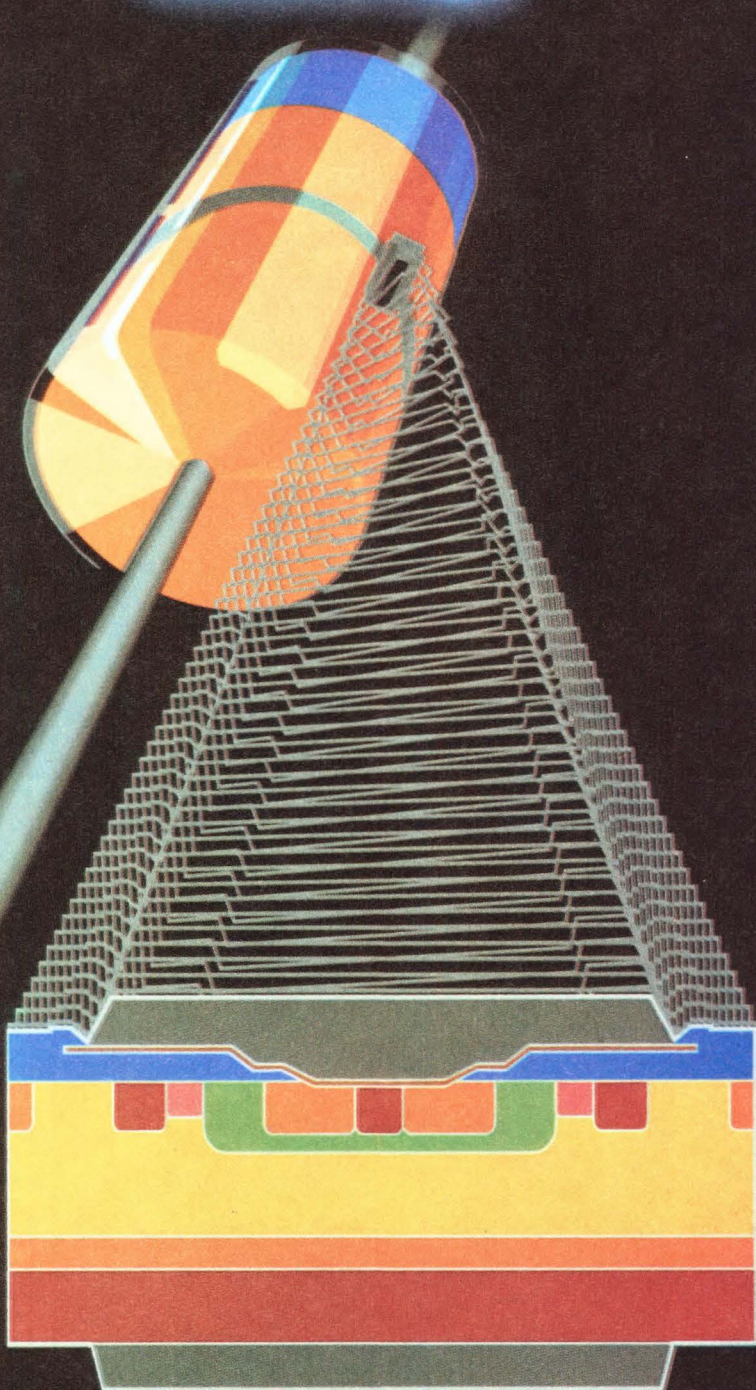
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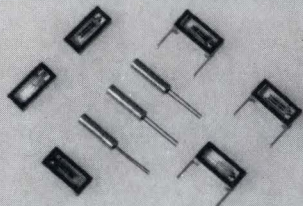


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CIRCLE 84

DESIGN ENTRY

Cover: Color palette chip

nected as closely as possible to the 5-V dc digital supply. In addition, the digital V_{EE} and memory V_{EE} inputs (DIGVEE and MEMVEE, respectively) are best tied in to -5.2 V dc and connected in common with other ECL circuits on the board. As with ANAVCC, however, the analog V_{EE} connection is best made as near as possible to its respective -5.2 -V dc source.

All power supply lines, whether analog or digital, should have not only a low dc resistance but also a low impedance, even at frequencies in the hundreds of megahertz. This requirement means placing high- and low-frequency bypass capacitors ($0.1 \mu\text{F}$ and $0.001 \mu\text{F}$, respectively) as closely as is practicable to the chip's power supply and ground pins.

Low-impedance grounds are equally important, and a ground plane for ECL is recommended. In addition, the reference ground system should have wide, thick conductors to introduce as little inductance as possible into the system. To avoid signal-induced ground currents, a $75\text{-}\Omega$ resistor to REFGND should terminate output I_0 because its complement, $\bar{I}_0$, returns to REFGND within the chip.

Similarly, all signal paths and components should be laid out paying careful attention to good high-frequency practices. Short lines built as microstrips work best for all digital inputs like Map Address, OVLY, W/B, CLK, and CLK. Moreover, termination resistors that match each line's characteristic impedance should be tied in as near as they can to the chip's pins.

Extra care is also called for at REFIN and compensation points COMP1 and COMP2, because their high impedance makes them particularly susceptible to externally induced noise. Links to these points must be as short as possible, even at the expense of lengthening connections on the other side of the chip. Capacitors at COMP1 and COMP2 should be located particularly close to their respective pins, and their dc ends should be terminated at ANAVEE in a single-point, or star, fashion to avoid ground current loops. □

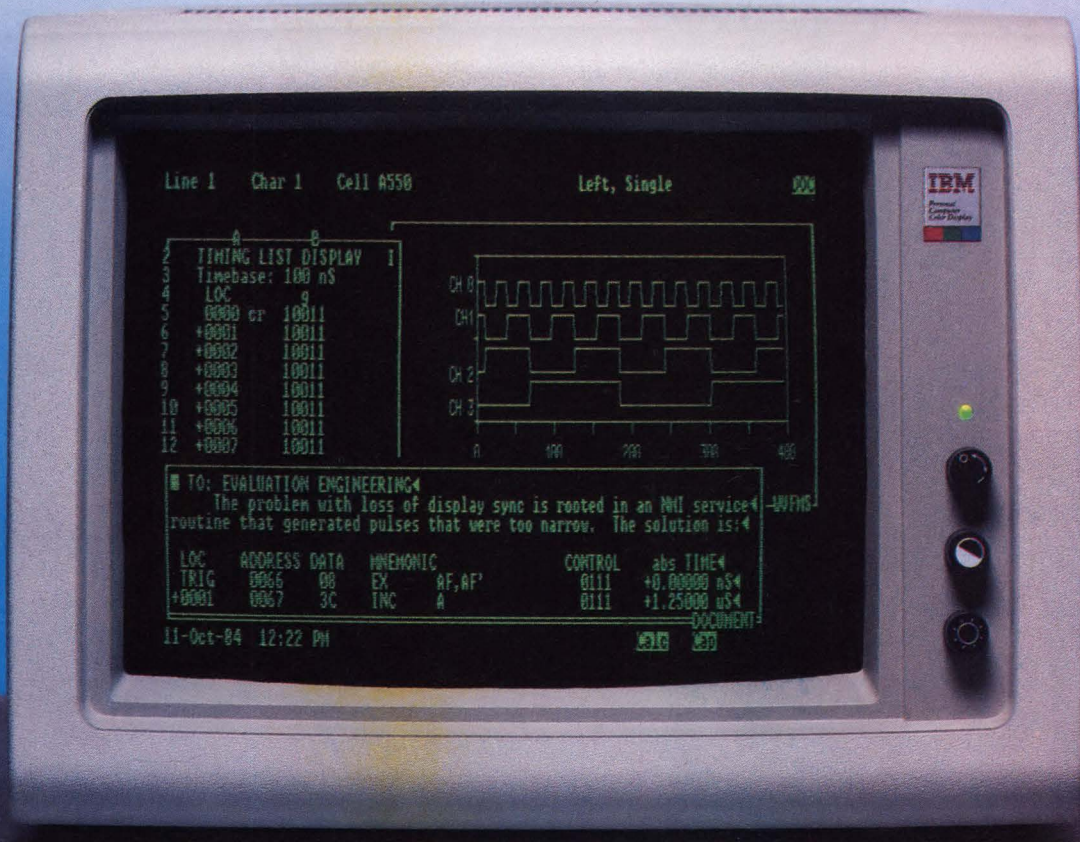
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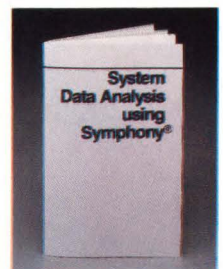
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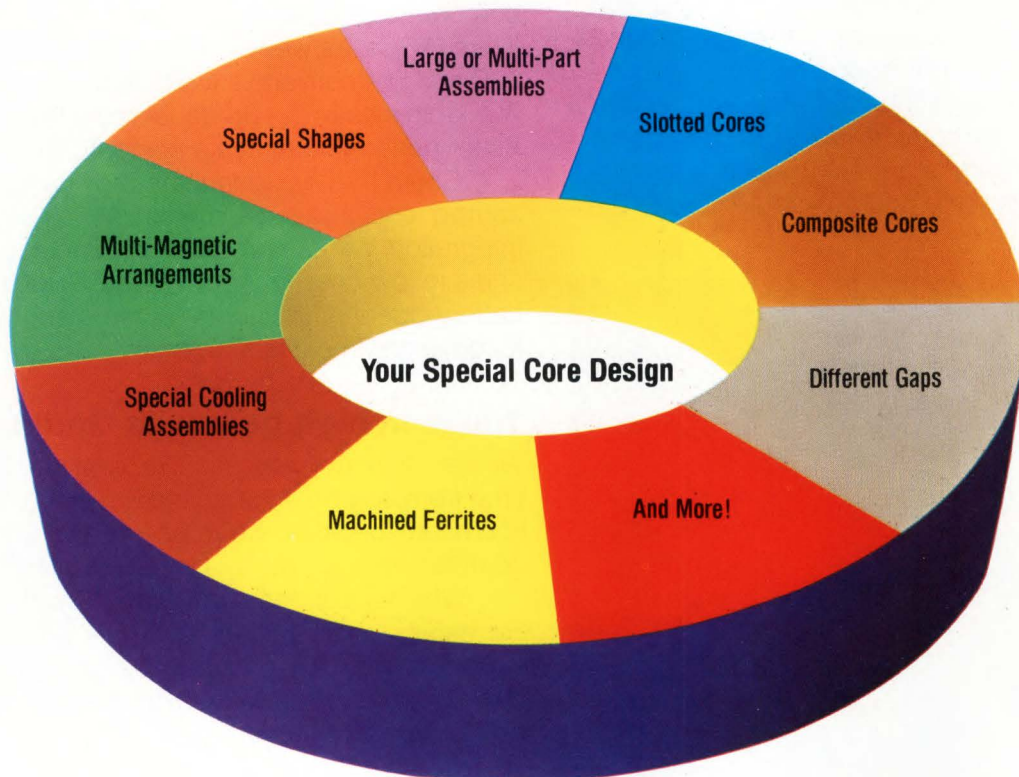
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Three chips, plus palette, aid graphics designers to paint detailed pictures

Three coordinated building-block ICs, organized around a bit map, ease the job of designing graphics systems that can resolve upward of 1024 by 1024 pixels.

This article, which is related to the cover story on a color palette chip (p. 187), deals with the three other chips in a family of high-performance graphics building blocks. They are powerful and programmable; thus they do not tie a designer to a particular graphics processor, image updating scheme, or video standard.

Like the harried air-traffic controllers who allocate airspace, graphics system designers must allocate access to the address space in a display's bit-mapped memory. In both cases, timing is everything, and often the designer's job can seem as much of a juggling act as the air-traffic controller's. To satisfy a graphics system's conflicting memory access demands, designers can now call on the

Andrew Daniel, Adrian Sfarti, and Achim Strupat
Advanced Micro Devices Inc.

Andrew Daniel is a product planner and an applications engineer with AMD's advanced graphics group in Sunnyvale, Calif. He has been with the company since 1982 and now designs and develops VLSI graphics chips. He holds a BSEE and an MSEE from Rensselaer Polytechnic Institute.

Adrian Sfarti is a section head of the advanced graphics group for product planning. He holds a BSEE and an MSEE from the Polytechnical Institute of Bucharest in Romania and a BS in mathematics from the University of Bucharest.

Achim Strupat has been a product planner and an applications engineer at AMD since 1983. He is responsible for specifying high-performance VLSI graphics components and holds an MS in computer engineering from the RWTH Aachen in West Germany.

Am8150 display refresh controller for assistance.

It is the most complex of three chips designed to support the Am8151 color palette, an IC that conserves memory space. Three color palettes together need only 8 memory planes to display 256 hues simultaneously out of 16.8 million. The two other supporting chips are the Am8157 video shift register, which serializes parallel data from the bit map and sends it to a color palette, and the Am8158 video timing controller, which synchronizes the system and sends timing signals to a display monitor. Together, the four ICs ease the job of designing high-resolution graphics systems—those with at least 1024 by 1024 pixels.

High on the refresh controller's list of strengths is its ability to execute any of three different memory arbitration schemes. Perhaps the most interesting is the one that interleaves memory refreshing and display updating cycles, a first for graphics chips. This mode ensures flicker-free screen refreshing while maintaining a high bandwidth to update the video image.

Rally round the bit map

The bit map is the focal point of a graphics system built around the Am815x family (Fig. 1). Working together, the chips can be programmed by the system CPU to adjust the display memory's size, the memory chip's organi-

Graphics chip set

zation, and the video frame's size and position. For example, the number of memory planes, bits per pixel, and bits per memory word all can be expanded in increments.

The display refresh controller addresses the bit map to refresh both the CRT screen and the dynamic RAMs that make up the bit map. In addition, the controller translates linear updating and refreshing addresses into multiplexed row and column addresses.

These processes all use the same address path to the display memory. Thus the time it takes to cycle through a single access, as well as to arbitrate among the three processes, is critical. Excessive flickering, sluggish image motion, or no image at all may result if the bit memory is not accessed when needed.

The problem of meeting each demand for access on time is complicated by the different address sources and data-path requirements of refreshing and updating. On the one hand, the addresses for refreshing the video display and

dynamic RAMs come from the refresh controller, and the complete set of display memory words are accessed in predictable cycles. On the other hand, the addresses that update the bit map originate at the system's graphics processor. They are bit-oriented and random, and they involve updating a video image by, for example, drawing vectors and circles or moving blocks of pixels.

Addressing ability

Because of the inherent differences between refreshing and updating an image, the display refresh controller lets the designer decide how best to accommodate each. It offers three programmable arbitration modes: interleaved updating, retrace updating, and update overriding.

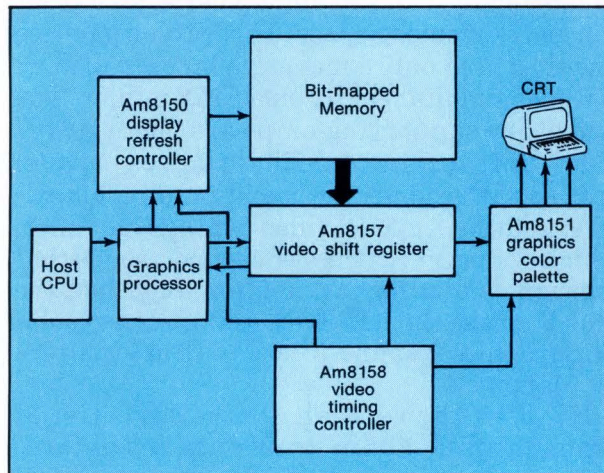
In interleaved updating, about 50% to 70% of the frame time is available for updating the video. This mode supplies a flicker-free video screen and simultaneous high bandwidth for updating. To achieve this mix, video refreshing and updating cycles alternate during the active video time (the interval when the CRT's display is scanned). The retrace time is shared between updating the display and refreshing the dynamic RAMs.

In retrace updating, about 10% to 20% of the time is spent updating the display. Here the active video time is devoted exclusively to refreshing the video. Updating shares the retrace time with the dynamic RAM refreshing cycles.

In contrast, update overriding, as its name implies, gives top priority to updating the display: about 95% of the time is available for that. On the other hand, video refreshing—and therefore any visible image—is sacrificed to the need for high bandwidth to change the bit map. When updating is complete one of the other two modes must be activated for the displayed image to return.

In all modes, the dynamic memories are refreshed during the horizontal retrace time. A user-programmable number of dynamic memory refresh cycles are used for each horizontal sync pulse.

Whereas the video-refresh and memory-refresh addresses are generated by the controller, the image-updating addresses enter the controller from the graphics processor; thus a



1. A bit-mapped memory is the focal point of a high-resolution graphics system built with the Am815x family of chips. The display refresh controller, which juggles memory accesses, and the video shift register, which serializes parallel data from the memory, connect directly to the bit map. The video timing controller synchronizes the digital and video signals, and the graphics color palette makes a wide choice of colors available with relatively little memory.

three-input multiplexer is needed in the refresh controller (Fig. 2). The multiplexer selects one address and sends it to the display memory as a row-address and column-address pair. The controller also issues correctly timed Row Address Strobe (RAS) and Column Address Strobe (CAS) signals. In all, it has four RAS signals with which to expand the memory plane up to four banks.

Expanding, panning and scrolling

The refresh controller also allows for smooth panning and scrolling, which in turn permit the screen to scan across a stored image that is larger than the screen itself. These effects are possible because the refresh controller can generate video refresh addresses for a small screen within a large display memory.

Two user-programmable registers define the display memory's screen size and position within a larger memory. A top-of-frame register stores the screen's starting location in memory.

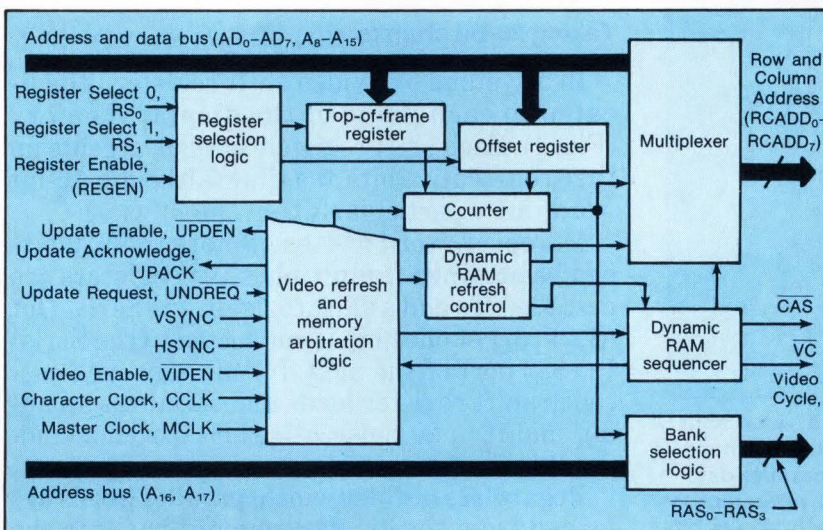
Subsequent addresses within a row are generated by incrementing the top-of-frame value. An offset register stores the number of locations between the last word of one row of the screen and the first word of the next row. The first address of the second row is the sum of the offset register value and the last address of the first row.

To achieve panning or scrolling, the contents of the top-of-frame register is incremented (that is, the register is reloaded) before every frame. For either effect, each new entry starts the screen at a different position.

Speedy and serial

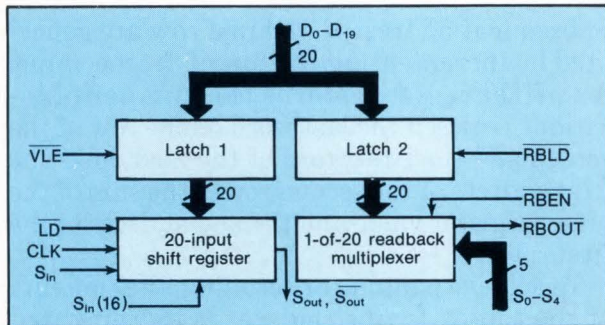
As video refreshing sequentially addresses all graphical data in the memory, the video shift register receives the accessed data and sends it to the screen. This occurs during the active video portion of the sweep.

To refresh the video image in a high-resolution system, the display memory data must be

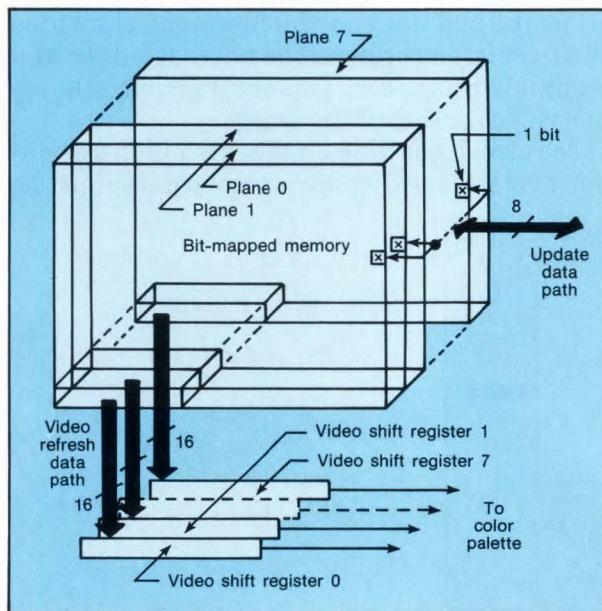


2. The display refresh controller orchestrates accesses to the bit-mapped memory's addresses. Demands for access come from the video refresh section, which sustains the displayed image; the dynamic RAM refresh circuitry; and an external graphics processor, which updates the bit map. The controller is the first graphics chip to interleave video refreshing and bit-map updating during an active video display.

Graphics chip set



3. The video shift register has two main functional blocks: a 20-bit shift register that serializes bit-mapped data and sends it to the monitor (or optionally to a palette) and a readback multiplexer that sends pixel information to the host processor. Each block has a latch to ease timing restrictions.



4. An eight-plane display memory with a video shift register at each plane satisfies conflicting memory access requirements. The eight 16-bit parallel data paths help meet the demands for video refreshing of 125 MHz per plane. A narrower, 8-bit path allows bit-by-bit access of each plane for updating individual pixels.

read very quickly. For example, about 125 million pixels a second must be read to refresh a noninterlaced display that generates 1280 by 1024 pixels (horizontal by vertical) at a 60-Hz rate. This leaves only about 8 ns to access each pixel.

Because conventional dynamic RAMs have access times of about 100 ns (in page mode), data must be read several bits at a time to meet the 8-ns/pixel limit. Then the parallel data must be serialized to drive a monitor. All of these requirements are met by the video shift register.

The register is well equipped to accept parallel data and put it in serial form. It also offers a way to read back a set of retrieved pixels to the graphics processor. Reading data back can occur simultaneously with—and independently of—the serialization and transmission of data. To keep serialization independent of reading back, the video shift register is divided into two main blocks, one for each major function (Fig. 3).

Taking 20-bit chunks

In a system, one video shift register is dedicated to each plane of the display memory (Fig. 4). Each shift register, in turn, accepts up to 20 consecutive bits at a time (although 16-bit words are a particularly convenient width).

Moreover, word widths of more than 20 bits can be attained if multiple shift registers are cascaded. To add a shift register, the Serial Out (S_{out}) port of one chip is connected to the Serial In (S_{in}) port of the next. In this way each cascaded shift register loads and serializes an additional 16 or 20 consecutive bits from a memory plane.

Regardless of their width, parallel words are loaded from the display memory bus into the shift register when LD is asserted. Words also may be preloaded into a built-in latch to relax the incoming data's setup and hold requirements. The latch is controlled by the Video Latch Enable input (VLE). Whichever way the data gets into the shift register, it is sent out serially and synchronously with the chip's Dot Clock input (CLK).

Dedicating at least one shift register to each plane has two major advantages. First, adding memory planes is relatively easy, necessitating

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Graphics chip set

little more than additional memory chips and shift registers. Second, the system's bandwidth requirement does not increase with additional planes.

One bit at a time

In a multiplane system, each shift register sends out one bit of a pixel at a time. Therefore, at any given moment the sum of the bits out of all the shift registers defines the pixel in question. From the shift register's serial output port, the bits go either to the color palette chip or to the monitor.

The second major function of the video shift register is to feed bits back to the host processor. Invoking the shift register's readback feature begins by asserting the Readback Load input (RBLD), which stores one display memory word in the readback latch.

Up to 20 pixels are available; selection lines S_0

through S_4 choose which of the 20 will be read out of each latch. Provided the value of the selection lines is less than 20 (values of 20 or more are ignored), asserting the Readback Enable signal (RBEN) places the selected bit on the chip's Readback Out line (RBOU). Therefore, when the RBOU lines of each shift register—and therefore each memory plane—are connected to a different line of a system bus and RBEN is asserted, the entire pixel is presented to the graphics processor.

All timing under one roof

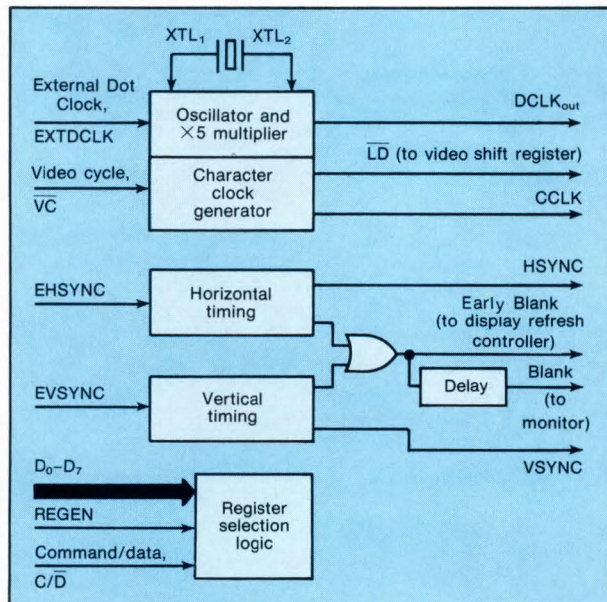
The third member of the family is the video timing controller. It issues all the timing signals needed by the other components of the bit-mapped system, including those for the video monitor (Fig. 5).

Ultimately, all timing signals are generated from the chip's on-board dot-clock oscillator. The clock, capable of reaching up to 125 MHz for high resolution, is crystal-controlled. Although an on-board oscillator simplifies the system, a designer can elect to supply a dot clock from one of two sources. The first is a TTL-compatible signal that, like the crystal, is one-fifth of the desired dot-clock frequency. The second is an ECL-compatible signal at the full dot-clock frequency.

A character clock output and an $\overline{LD}$ signal derived from the dot clock, supply the timing signals for the display refresh controller and video shift register, respectively. With these signals, the chips address and latch display memory words during the refresh cycles.

To adapt to different video standards and screen sizes, the timing controller's video signals have programmable parameters. For example, the lengths of the Horizontal and Vertical Sync pulses (HSYNC and VSYNC), as well as their front and back porch lengths, are programmable, as are the number of pixels to a scan line and scan lines to a frame. The chip also produces a video blanking signal for the monitor and a Video Enable (VIDEN) signal for the display refresh controller.

As an alternative, the video pulses from the timing controller can be synchronized to external sources. That permits the chip set to operate with other devices, as needed, to mix text and graphics, or to synchronize the display to the



5. The fully programmable video timing controller generates horizontal and vertical synchronization pulses, blanking pulses, and dot and character clocks. The dot clock and synchronization pulses can be externally triggered to coordinate the action of other graphics circuits.



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Graphics chip set

power-line frequency. For greater flexibility, the external sources, which are applied to inputs EHSYNC and EVSYNC, can be asynchronous to the character and dot clocks.

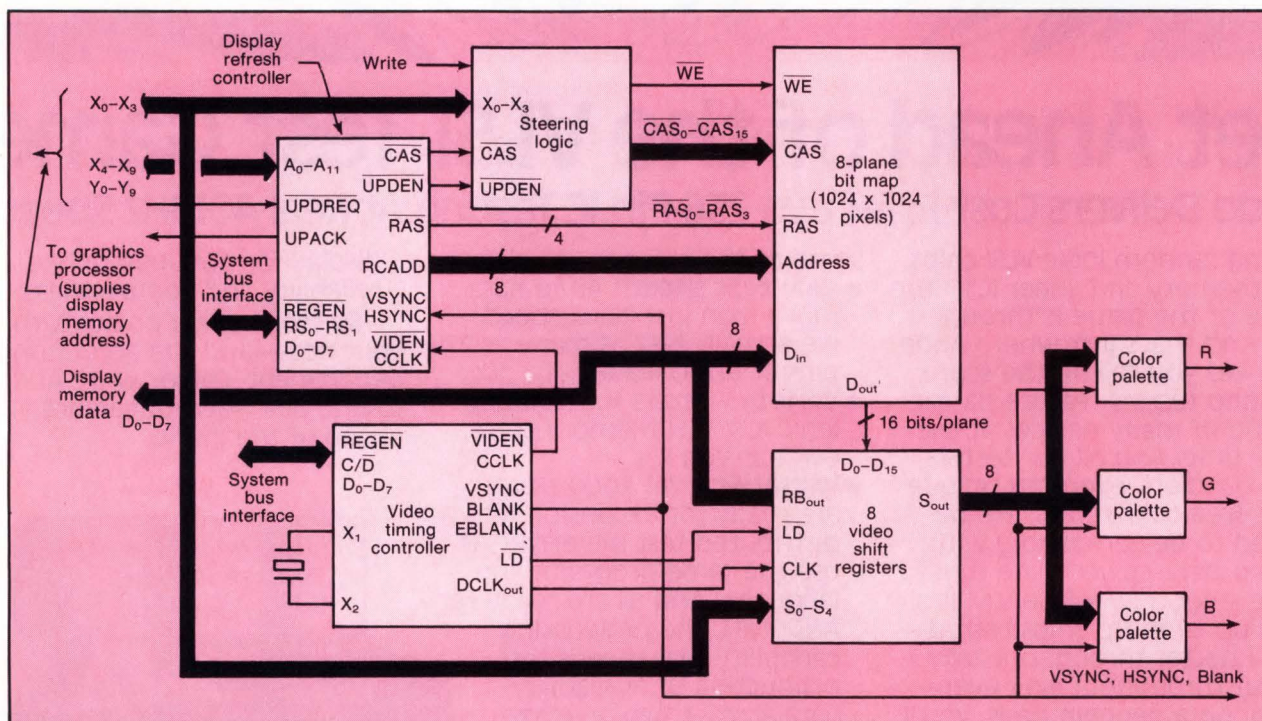
In a typical application, the four chips form the core of an efficient pixel-oriented graphics system that resolves the conflicting requirements of refreshing the video screen, refreshing the dynamic RAMs, and updating the display memory (Fig. 6). For low-overhead video refreshing, the system lays down a wide data path from the display memory to the CRT; for efficiently updating the bit map, it provides addresses to individual pixels.

The system has eight 1024-by-1024-bit memory planes, each made up of sixteen 64-kbit RAMs. The display refresh controller orchestrates the video refreshing, memory refreshing, and video updating. Eight video shift registers, one for each memory plane, serialize the data and are a means for reading back the con-

tents of the memory. The shift registers' serial outputs drive three color palette chips, and the timing controller produces all the timing signals. A separate graphics engine generates updated addresses and manipulates the stored images; a sprinkling of additional components, embodied in the steering logic, completes the system.

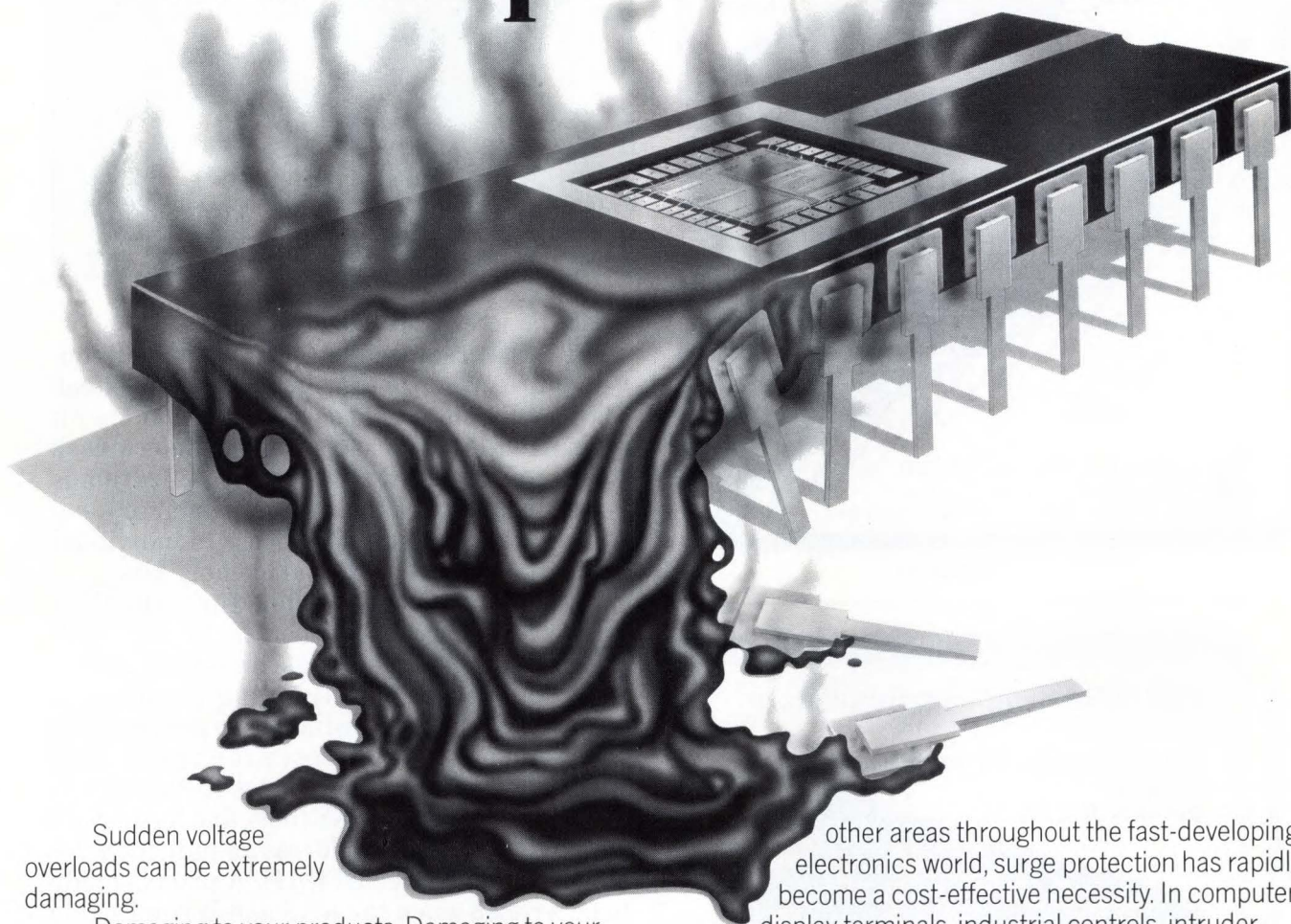
The pause that refreshes

To refresh the screen at the standard rate of 60 frames/s, a complete frame must be sent to the monitor every 16.6 ms, requiring that a new line be scanned every 16 μ s. With 1024 pixels in a line, the bit rate for refreshing the screen would seem to be 15 ns/bit, but after horizontal and vertical retrace times are subtracted, the actual bit rate is more like 10 ns/bit. Therefore, if the memory is read in the page mode and its read cycle time is 160 ns, then at least 16 bits must be read from the memory simultaneously to re-



6. Together, the four-chip set reduces the parts count of a 1024-by-1024 pixel graphics system. The added steering logic helps the display refresh controller by distributing the controller's CAS output among individual memory planes so that a graphics processor can update individual pixels. The system uses eight video shift registers, one for each memory plane, and three color palettes, one for each color gun.

What will happen when the chips are down?



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CIRCLE 91

DESIGN ENTRY

Graphics chip set

Steering logic truth table

Input					Output		
UPDEN	X ₀	X ₁	X ₂	X ₃	Active CAS lines	WE	Process
1	X	X	X	X	None	1	Dynamic RAM refreshing Video refreshing Video updating
1	X	X	X	X	All	1	
0	0	0	0	0	CAS ₀	1,0	
↑	0	0	0	1	CAS ₁	(1 for read cycle, 0 for write cycle)	
	0	0	1	0	CAS ₂		
	0	0	1	1	CAS ₃		
	0	1	0	0	CAS ₄		
	0	1	0	1	CAS ₅		
	0	1	1	0	CAS ₆		
	0	1	1	1	CAS ₇		
	1	0	0	0	CAS ₈		
	1	0	0	1	CAS ₉		
↓	1	1	1	1	CAS ₁₅		

fresh the screen adequately.

With that requirement, it is especially convenient to organize the planes around sixteen 64k-by-1 RAMs and to concurrently take one bit from each RAM to satisfy the video refresh requirements. However, this organization is not convenient for updating the memory, because updating demands access to individual pixels and thus to individual memory bits.

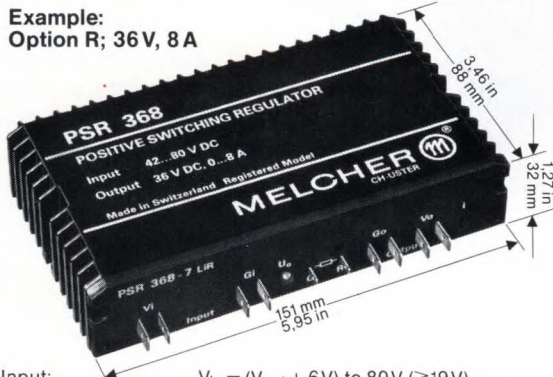
For video updating, therefore, the $\overline{\text{CAS}}$ signals are steered to each of the 16 chips individually. Addressing a single bit is then accomplished by time-multiplexing the display memory's X and Y coordinates to generate the row and column addresses for the 64-kbit RAMs. Specifically, coordinates X_0 through X_3 activate one of the 16 $\overline{\text{CAS}}$ lines, and X_4 through X_9 and Y_0 through Y_9 address an individual location within a selected RAM. A pixel is ready to be written when the $\overline{\text{RAS}}$ and Write Enable lines ($\overline{\text{WE}}$) for all 128 RAM chips are activated; then, with the help of the steering logic, only one of 16 $\overline{\text{CAS}}$ signals is asserted and a pixel is written (see the table, above).

To read back the memory contents, data can again be accessed in 16-bit words (representing 16 pixels) from each memory plane and latched into eight corresponding video shift registers. Select lines pick one bit of the 16 in each read-back latch and assertion of the shift register's Readback Enable activates the path. □

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CIRCLE 92

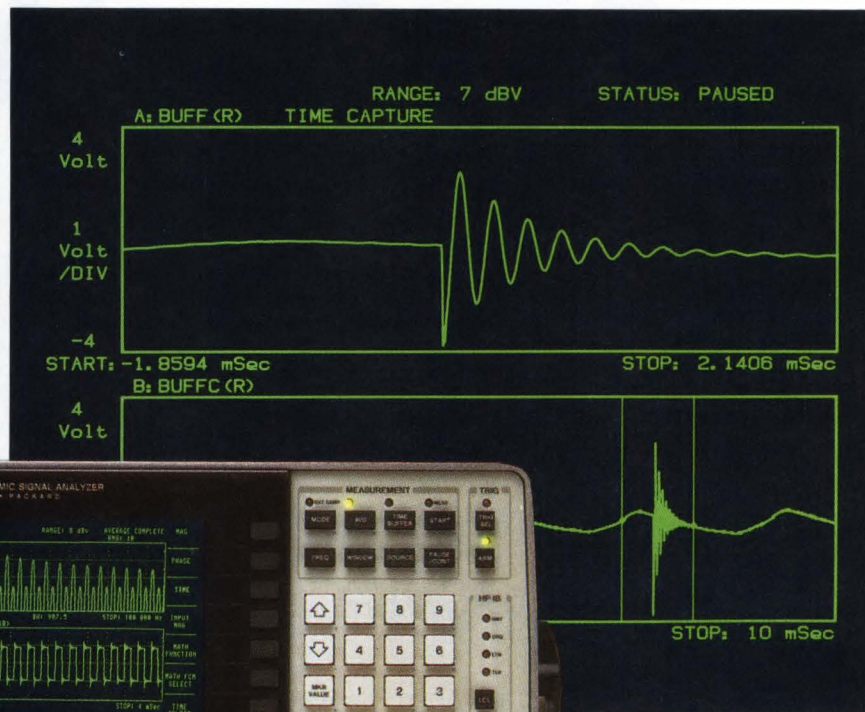
How useful?

Immediate design application
Within the next year
Not applicable

Circle

544
545
546

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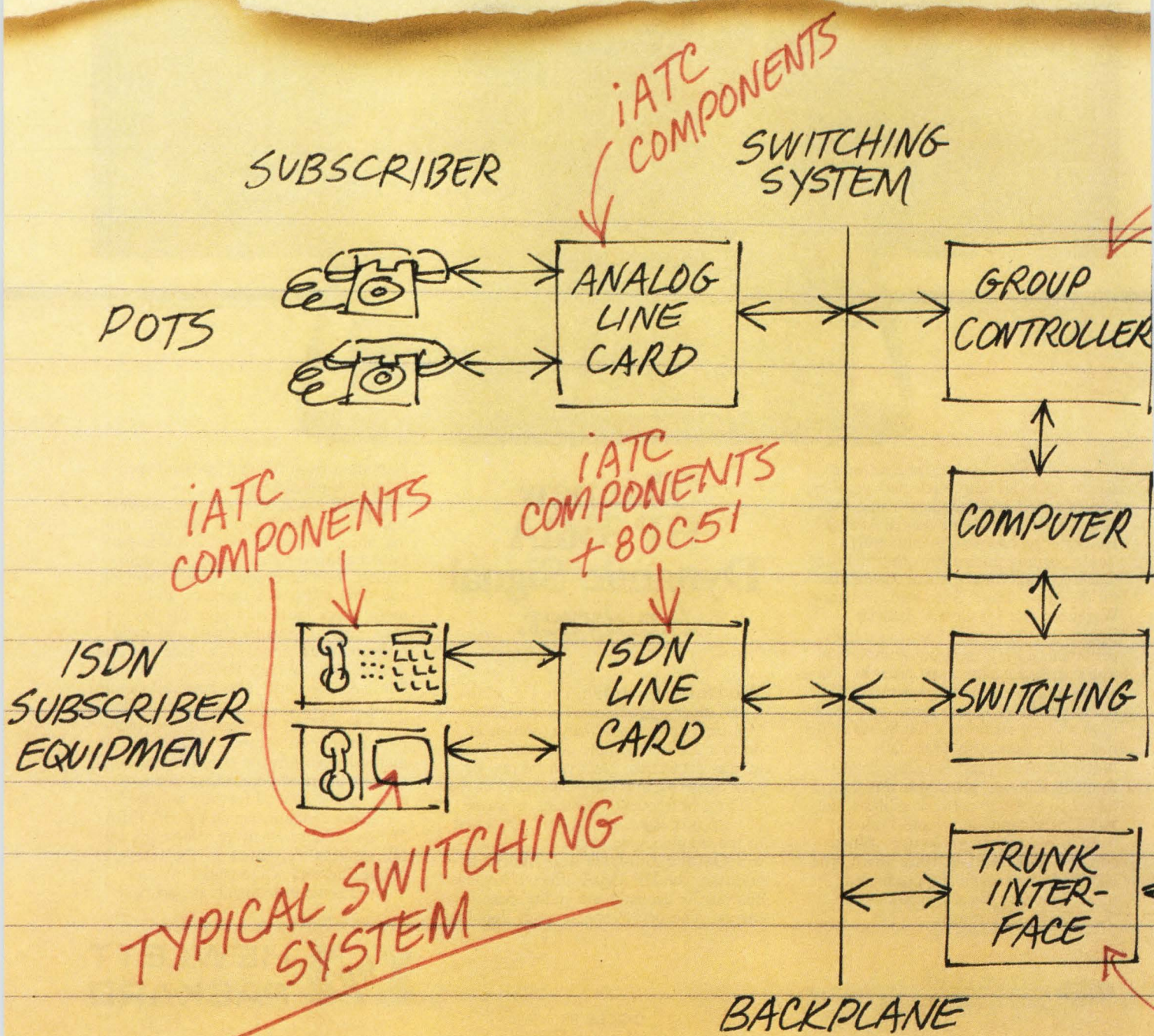
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CIRCLE 93



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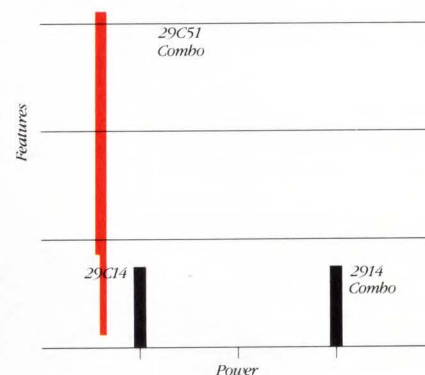
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CIRCLE 95

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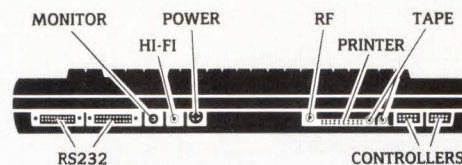
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GaAs cell array lets designers fit a fast subsystem into a chip

Borrowing a standard-cell design technique from silicon technology, a gallium arsenide array chip adds gigahertz speed to digital and analog subsystems.

Today's increasingly complex subsystems cry out for a chip technology that can hit clock rates of more than 300 MHz. In silicon, such fast circuits typically are limited to the small-scale level of integration, and even then they dissipate a fair amount of power. Gallium arsenide is positioning itself to answer those appeals, bringing speed to analog or digital circuits or both.

Witness a gallium arsenide cell array dubbed the Quick Chip. This medium-scale IC integrates more functions, performs at higher speeds, and dissipates less power per function than do comparable silicon implementations. Thanks in part to a specially designed leadless chip carrier, the packaged device attains digital

clock rates of up to 2 GHz and a 3-dB analog bandwidth of 5 GHz—the highest ratings for any packaged MSI chip. Moreover, even designs that employ all of the array's 28 core cells dissipate 2.8 W at most.

The list of possible applications for the array is outstanding. In the digital world, it can build divide-by-N counters, multiplexers and demultiplexers, and even combinatorial logic. On the analog front designers can create vhf and microwave gain blocks, oscillators, and attenuators. In particular, the medium-scale technology is well suited to mixed analog and digital such as gigabit-per-second optical fiber links, extremely fast encoder-decoders, and converters that translate data from parallel into serial and back into parallel form.

Implementing specific circuits with the cell array is straightforward: The cells are organized hierarchically, and a library of digital macrocells includes I/O devices that interface readily with ECL, TTL, and CMOS circuits. Manufacturing a design is fast, involving only three metallization layers for digital and simple analog applications.

Mounting the Quick Chip is no problem. With its leadless chip carrier and socket—both developed specifically for use in prototype systems—it can be mounted on high-speed boards without soldering and without performance degradation.

The GaAs array packs 28 core cells and 24 I/O

M. Louis Pengue, Thomas M. Reeder, and Binoy A. Rosario, Tektronix Inc.

Now a design engineer in the GaAs Integrated Technologies unit of Tektronix, M. Louis Pengue originally joined the Beaverton, Ore., company to design bipolar silicon analog ICs. He holds a BSIM, BSEE, and MSEE from Georgia Institute of Technology.

Thomas M. Reeder first worked on Tektronix's high-speed GaAs IC process in 1978 as manager of solid-state research. Now the GaAs unit's marketing manager, he has a PhD in electrical engineering from Stanford University.

In his 10 years at Tektronix, Binoy A. Rosario has designed analog and digital silicon ICs and helped develop new CAD tools. He became the GaAs unit's design manager in June. He earned a PhD from the University of California at Berkeley.

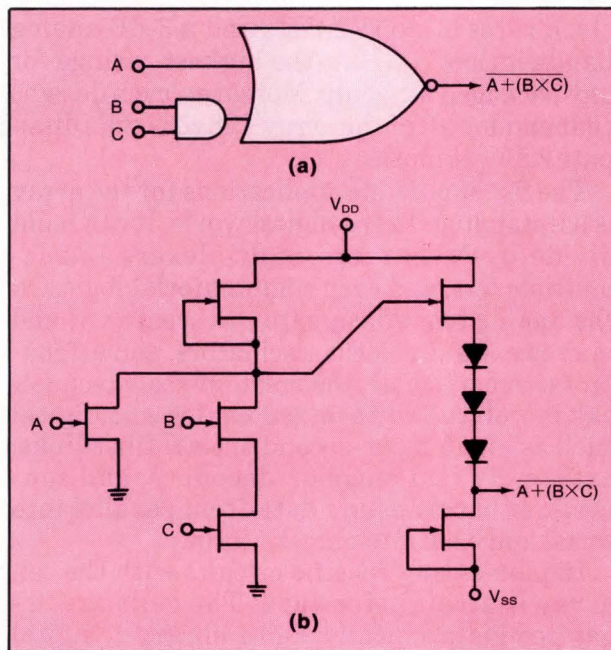
GaAs cell array

cells into a chip measuring 2 by 2 mm. Each core cell contains 20 depletion-mode transistors, 8 diodes, and 12 resistors, all used as primitives in the construction of basic logic macrocells.

Making the floorplan

A logic device with the complexity of a D latch can be formed in just one core cell, and a master-slave flip-flop in just two. Simple NAND and NOR gates and a variety of latches and flip-flops are included in the macrocell library.

To build logic gates, the array uses buffered FET logic (Fig. 1), the most mature of several GaAs logic families now emerging (see "Gallium Arsenide: Ready to Fly," opposite). It also is well known for its ability to form circuits that can block at 2 GHz and up.



1. The gallium arsenide cell array contains depletion-mode transistors and buffered FET logic. To build an inverter gate with it (a), a designer would link six of the core cell's 20 transistors, three of its eight diodes, but none of its 12 resistors (b).

Buffered FET logic requires two power supplies, since the depletion-mode transistors in the core cells must be biased negatively to turn them off. The diodes at the source-follower output of each logic gate shift voltage levels, so that logic levels are the same at both input and output.

As for the 24 I/O cells, they and their associated bond pads have been arranged on the chip, so as to reduce high-speed crosstalk. The power supply connects to the four chip corners, and multiple ground pads ensure that no more than two I/O bond pads are next to each other. The I/O cells can be tailored to match the voltage and current characteristics of ECL, TTL, and CMOS circuits.

The fabrication of digital circuits requires three custom photomask layers (the first metal layer, vias, and the second metal layer) above the preprocessed layers that form the cell array. Simple analog circuits, using only transistors and ion-implanted resistors, may also be formed in this process.

Circuits containing inductors can be built in the digital process, but the design and placement of inductors is a custom job that lengthens design time. For more sophisticated analog circuits, extra process steps can be added to create metal-insulator-metal (MIM) capacitors and precision nickel-chrome resistors. Thus analog and digital circuits can be integrated without the use of elaborate interchip interface technology and with minimum parasitic elements.

The right wrappings

An unsuitable package can degrade the performance of any high-speed IC. In response to fast rise times—on the order of 0.5 ns or less—it may distort waveforms and induce crosstalk on the signal lines, which should ideally be as much like uniform transmission lines as possible, with little or no impedance variations. Also, a package with more than a few I/O lines is difficult to mount on standard printed circuit boards.

The package designed for the GaAs gate array builds on one used earlier in high-speed oscilloscopes. A 0.42-by-0.42-in. ceramic chip carrier, it is connected to a custom-designed high-speed circuit board through an elasto-

meric interconnection system. Thin-film metallization overlays the carrier with two dozen 50- Ω transmission-line I/O connections leading to contacts 0.025 in. apart—a spacing that matches today's high-performance boards. Chip bypass capacitors mounted on the ceramic substrate afford excellent power bus decoupling.

Once mounted on the chip carrier, the GaAs array is protected by a ceramic lid. A plastic frame, or socket, ensures accurate positioning on the board of both the carrier and its strips of elastomeric contacts. The carrier is placed lid down on the board. With that upside-down arrangement, a heat sink can be used with screws going through both the frame and the board to secure the assembled package.

The resultant package has excellent elec-

trical thermal characteristics. Impedance varies about $\pm 5 \Omega$ or less throughout the signal path for an input with a 100-ps rise time. Crosstalk between adjacent signal lines is more than 20 dB down for frequencies up to 5 GHz, and the 3-dB bandwidth of the connection from board to chip to board also comes in at 5 GHz. The assembled package can safely dissipate more than 2 W in calm air and still keep the GaAs junction temperatures below 125°C.

A familiar approach

Digital circuit design with the Quick Chip resembles gate-array techniques. The standard macrocell library consists of symbols, models, and cell layouts. The user constructs a schematic diagram from the symbols and then simulates the design with models, which include

Gallium arsenide: Ready to fly

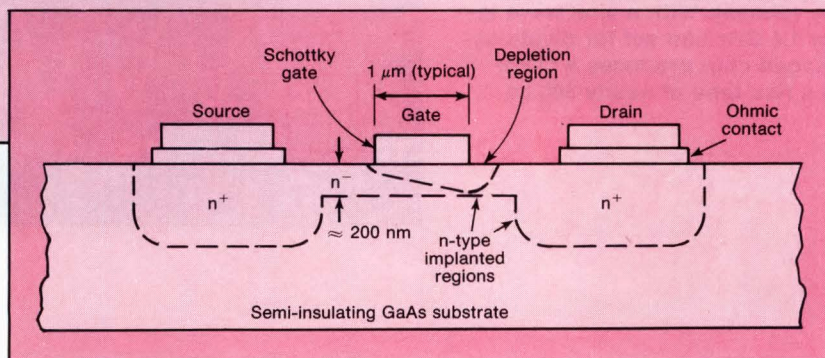
Long a laboratory curiosity, gallium arsenide is now crossing the boundary into commercial production. Better starting material is being grown, processing steps are being whittled away compared with those for high-performance ECL and CMOS, and manufacturers are successfully exploiting process and design techniques originally developed for silicon.

Just five years ago, gallium arsenide substrates were plagued with inordinate amounts of defects and residual impurities. Fortunately most of those flaws have disappeared. Large uniform wafers, 3 in. in diameter, are being created with ingots grown by the liquid-encapsulated Czochralski manufacturing process.

As for the processing steps, consider the most mature gallium arsenide process. It employs depletion-mode ion-implanted MESFETs and produces a relatively simple, planar structure (see the figure). In the setup, multiple layers of a titanium-gold alloy are deposited atop the Schottky barrier

gate, which is usually 1 μm long. The n^+ source and drain regions make contact through layers of a gold-germanium alloy. A lift-off process defines both these layers and the gate length. An insulating thin film of, say, silicon nitride passivates and protects the unmetallized GaAs surface. The various processing steps—including photolithography, ion implantation, diffusion, layer deposition, and annealing—add up to about half the number needed for high-performance CMOS and almost one-third the steps of ECL.

Many gallium arsenide manufacturing techniques are borrowed from the silicon production line. An exception is the technique known as air-bridge metallization, which has not traditionally been used for silicon ICs. This approach lifts the metallization about 1 μm above the semiconductor substrate, thus more than halving the wiring capacitance. On the Quick chip, it is used for second-level interconnections, enhancing both circuit speed and manufacturing yield.



GaAs cell array

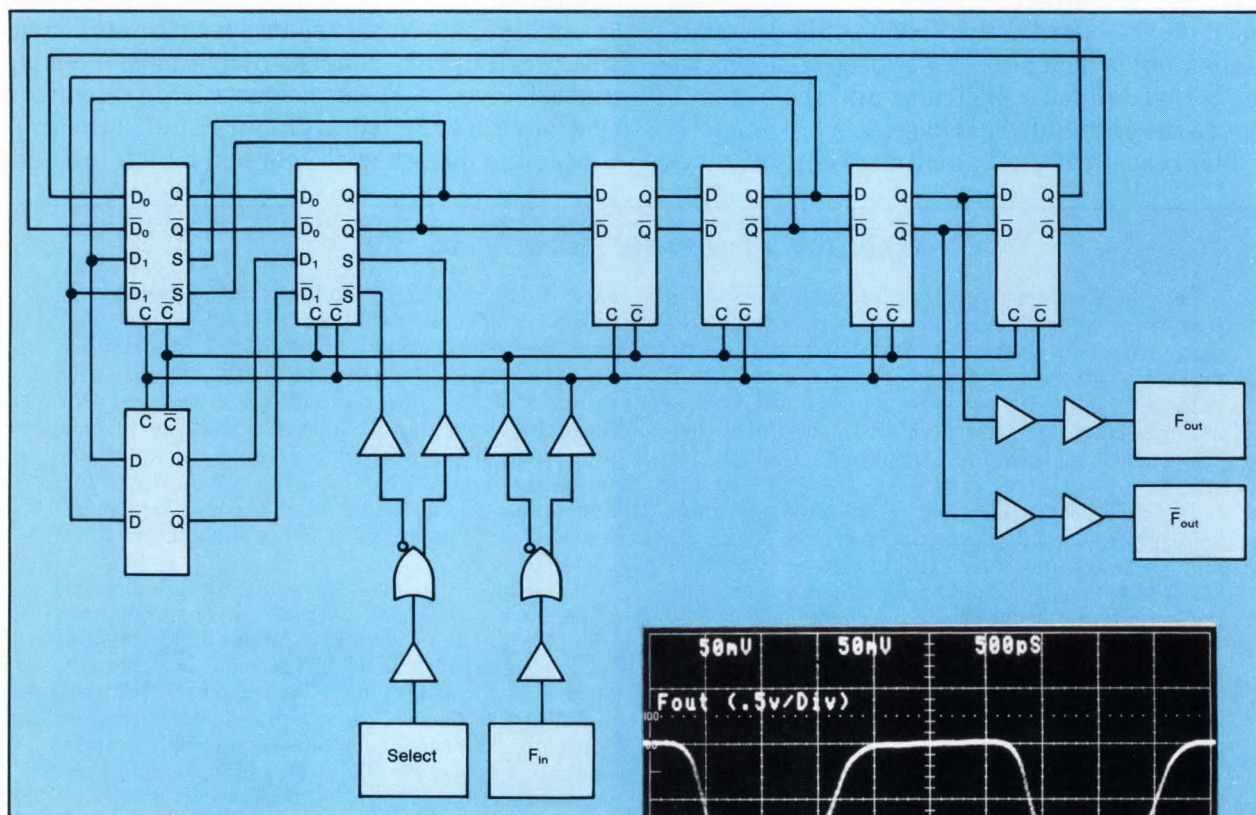
timing information. Afterward, an automatic placement and routing program completes the layout, integrating the cell arrangement and the original user-defined net list into the floorplan of the chip.

That program also extracts parasitic capacitances of the routed layout and feeds them back to the user for resimulation. (The logic delays added by parasitic loading alter the timing of the standard macro models.) Normally the layout and extraction of parasitic capacitances take a day. When the user is satisfied with the

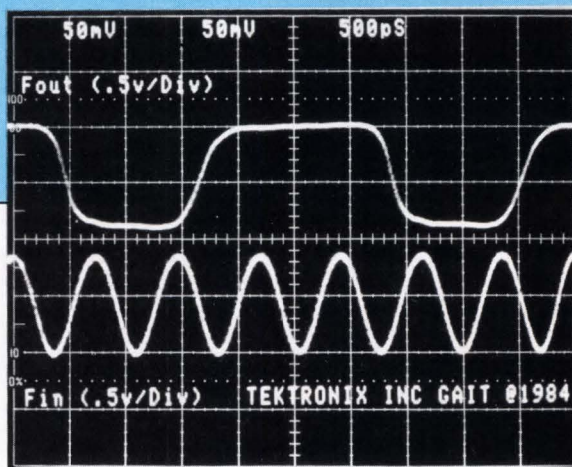
design and the simulation results, the mask and wafer fabrication processes begin, typically adding another eight weeks.

Though those design tools are found now only with the Quick Chip's manufacturer (which accepts user-supplied net lists), the digital macro design information will be installed in some workstations early next year. For designers working at the transistor level, an extended design manual will include Spice device models and transistor interconnection rules.

The high performance of the GaAs cell



2. A divide-by-4/5 counter circuit occupies one-third of the GaAs cell array (above). With a sine wave input frequency (F_{in}) of 1.4 GHz and set for divide-by-4 operation, the packaged chip produces a clean 350-MHz output with a rise time of nearly 300 ps (right).



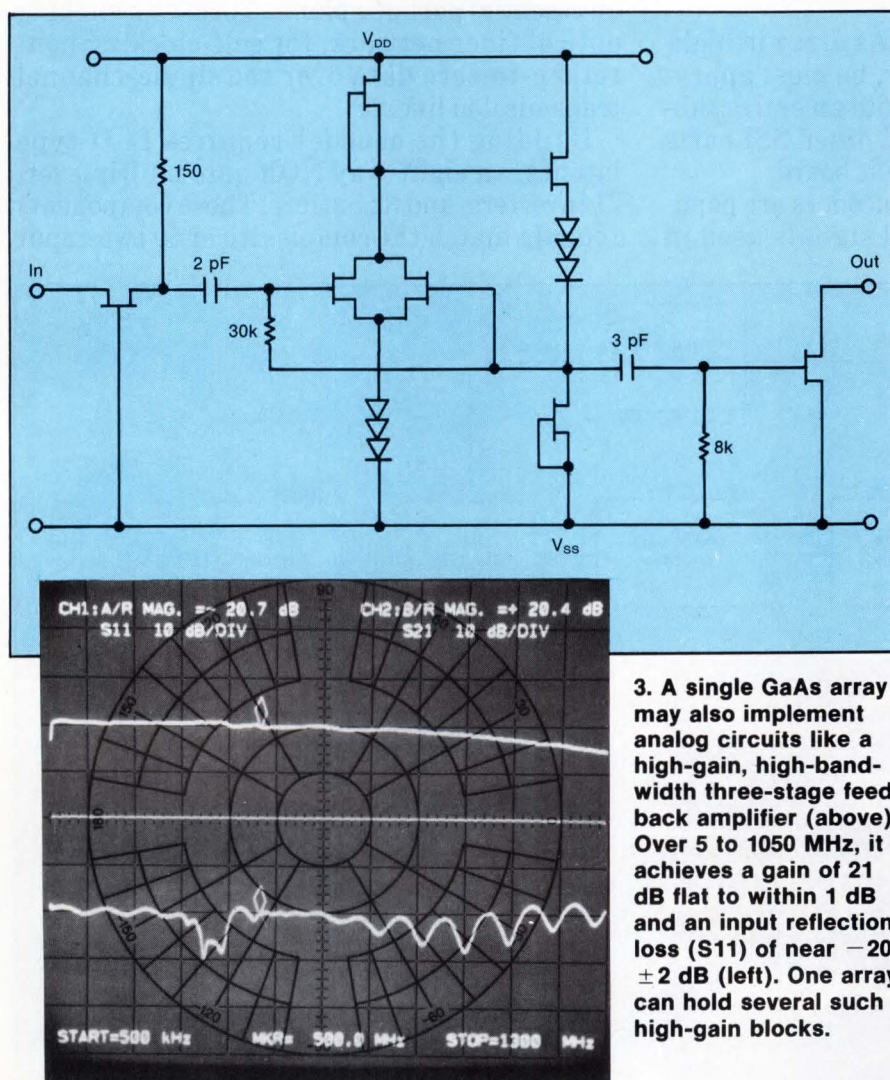
array is evident at the simplest level. A typical gate delay for a NOR gate with a fan-in and a fan-out of 3 is about 190 ps with 20-mW power dissipation.

Figures of merit

The next step up is a more complex building-block circuit that is designed for high speed. For example, a variable-modulus, divide-by-4/5 counter consists simply of several interconnected macrocells—seven complementary clocked latches and the appropriate I/O circuits

(Fig. 2, at top). It uses only nine core cells and four I/O cells, or about one-third the entire array.

When mounted in the leadless chip carrier and producing a divide-by-4 output from a 1.4-GHz input, the circuit produces a 350-MHz waveform that is very clean, with output rise times that are less than 300 ps (Fig. 2, bottom right). In contrast, the output waveforms of comparable silicon IC counters typically suffer from overshoot and other waveform distortions. (The counter's nominal voltage and



3. A single GaAs array may also implement analog circuits like a high-gain, high-bandwidth three-stage feedback amplifier (above). Over 5 to 1050 MHz, it achieves a gain of 21 dB flat to within 1 dB and an input reflection loss (S11) of near -20 ± 2 dB (left). One array can hold several such high-gain blocks.

GaAs cell array

power requirements are a V_{DD} of 4 V, a V_{SS} of -3 V, and power dissipation of 400 mW.)

Analog designs also can get a boost from the GaAs array. For instance, a three-stage feedback amplifier, which was designed to deliver 20 dB of gain over a 1-GHz bandwidth, attained an actual gain of 21 dB flat to within 1 dB over 5 to 1050 MHz (Fig. 3). The on-chip impedance-matching circuit held input reflection loss near -20 ± 2 dB over the same frequency range. This figure corresponds to a match of $50 \pm 5 \Omega$. A single Quick Chip can create several gain blocks of this class.

The performance of the GaAs array in high-speed systems will, however, be most appreciated when the device can build an entire subsystem, replacing, say, a half-dozen SSI parts mounted on an expensive circuit board.

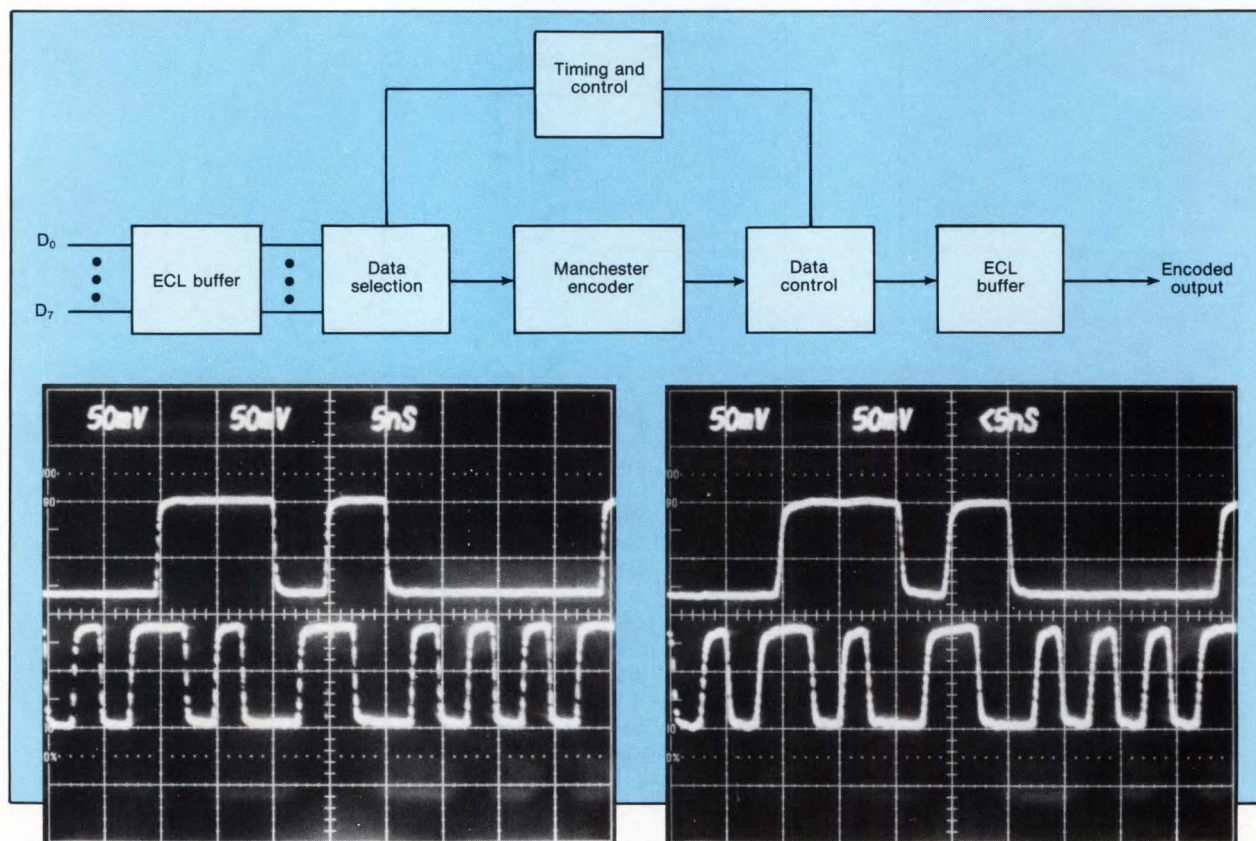
For example, Manchester encoders are popular for encoding the optical signals used in

fiber-optic communication links that work with data rates above 400 Mbits/s. Designers usually encounter difficulties in laying out an ECL-based circuit that can perform reliably at such speeds, and the fact that the 400-Mbit/s data rate requires an 800-MHz clock rate further complicates traditional design.

A speedy chip subsystem

RCA Corp.'s Advanced Technology Laboratories in Camden, N.J., has already built a Manchester encoder with the GaAs array. It will be an essential part of a planned packet-switching optical fiber network, for self-clocking non-return-to-zero data over the single-channel transmission lines.

Building the encoder requires 14 D-type latches, an eight-way NOR gate multiplexer, 21 inverters, and 32 buffers. Those components roughly match the complexity of 50 two-input



4. A Manchester encoder circuit is one of the many subsystems to which the GaAs cell array can be tailored (top). Its output waveforms demonstrate its reliable operation at output data rates 400 MHz (below, left) and at 800 MHz (below right); in the latter case, each time division is actually 2.5 ns.

THE \$4900 DEVELOPMENT STATION.

More than an emulator, the Relms Icebox is an upgradeable, portable development station. For \$25,000 less than you'd pay for a cumbersome development system, you can emulate, program proms, interface to your line printer and upload/download to your host machine.

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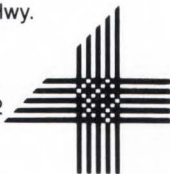
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CIRCLE 129

DESIGN ENTRY

GaAs cell array

NOR gates and are representative of a subsystem that uses up most of the array's cells.

The architecture and layout of the encoder follow a well-known design (Fig. 4, at top). The incoming 8-bit data, supplied by an ECL-based data generator, is applied to buffers that translate logic levels into values convenient for GaAs depletion-mode circuits—between 0.5 and -2.2 V. Data selection is controlled synchronously with the system clock. As a result, the encoder receives a steady stream of data, and the timing of the exclusive-OR encoding can proceed accurately with respect to the system clock. The encoder's output moves to a data control circuit, which ensures that the Manchester-encoded data is properly timed for transmission off chip. Finally, the voltage level is converted at the output ECL buffer, enabling the latter to interface with an ECL circuit that drives the fiber-optic input.

Fine-tuning for timing

Because of the fast switching times of the internal logic gates, inverter delay stages must be added at several points in the circuit. Without them, the pulse edge timing would be inaccurate at the encoder's high clock rate.

All input and output buffering occurs at ECL logic levels (-0.9 to -1.75 V) using 50-Ω transmission line interconnections. With that approach, the balance of the fiber-optic electronics, whose speed is less critical, can be built with standard ECL.

The Manchester encoder can easily run at 400 MHz with an 800-MHz clock (Fig. 4, bottom left). In fact, it can operate reliably to at least 800 MHz (Fig. 4, bottom right), with I/O characteristics that interface with an external ECL-based system. □

The authors would like to acknowledge the contributions of Tektronix engineers Gary McCormick, David Smith, and Eric Strid, RCA engineer Bill Heagerty, and in particular Bob Schellack, also of RCA, who was the designer of the Manchester encoder.

How useful?

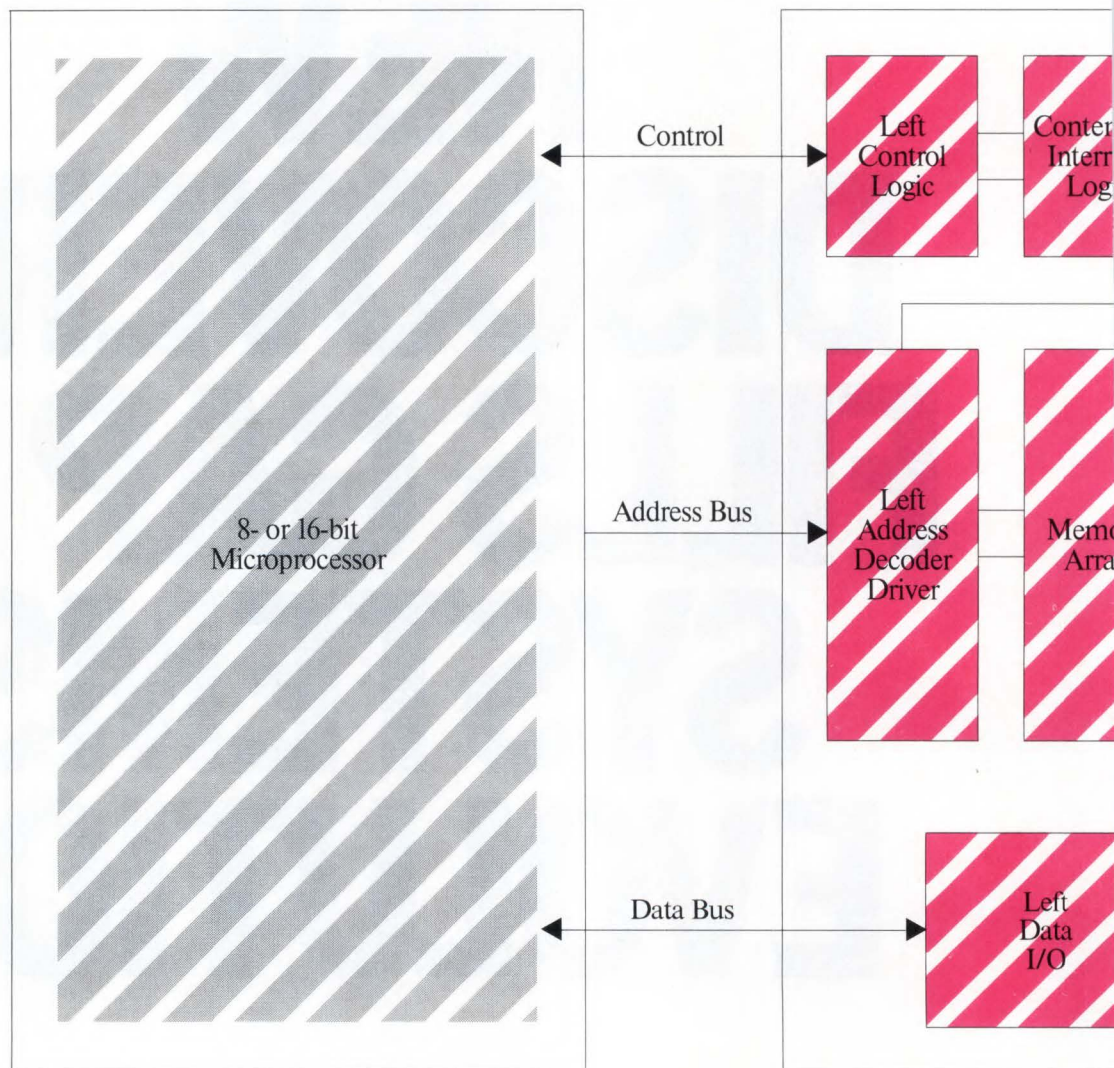
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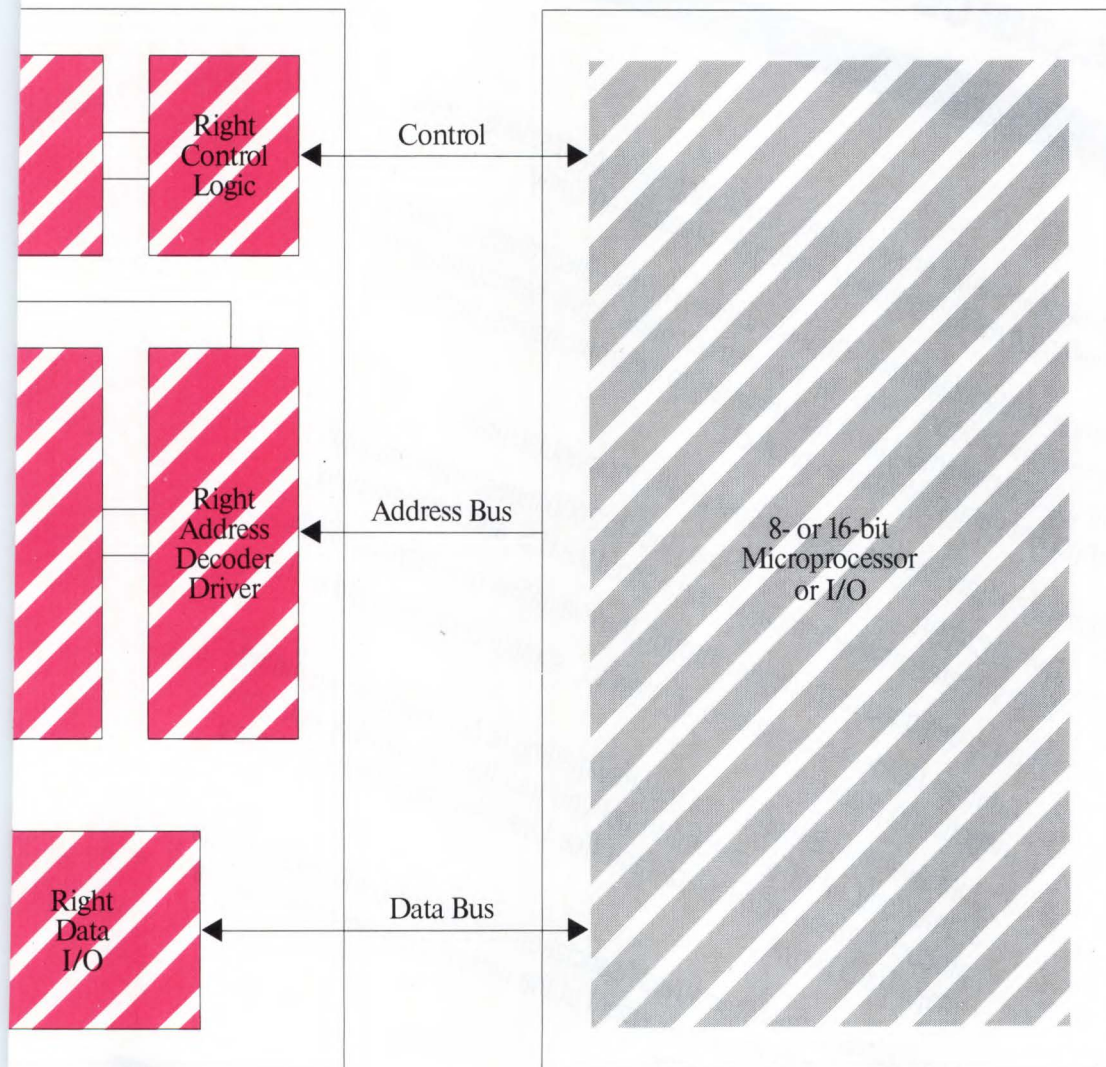
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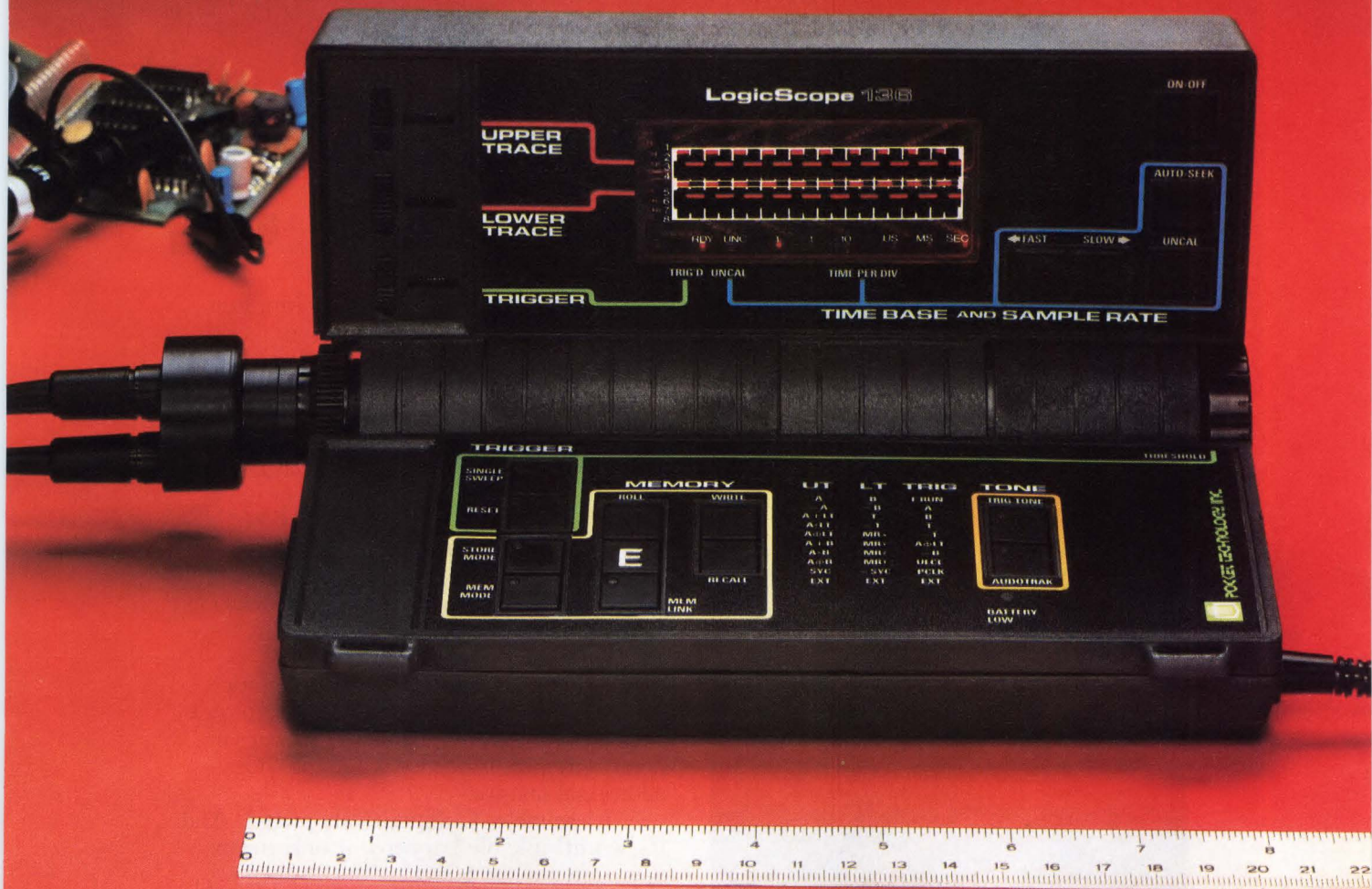


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With its paged structure, a 512k EPROM relaxes system storage constraints

The limits imposed by the addressing range of today's 8-bit microprocessors are removed by a page-addressed EPROM that acts like four 128-kbit chips.

Inventive system designers know that advanced software features could prolong the usefulness of their 8-bit microprocessor-based systems. Though the idea is an attractive one, adding those changes to program memory would often strain the 64-kbyte addressing range of the microprocessor.

Today's 512-kbit EPROMs have the higher capacity but would consume the entire address space of the 8-bit machines. A new twist—a 512-kbit EPROM organized as four 16-kbyte pages—quadruples the program storage available to an 8-bit system. Indeed, 16-bit systems can benefit from using it.

As important, the entire chip looks to the system like a 128-kbit EPROM, which it can easily replace. Upgrading a system in this way entails little or no software modification, while building a new one with the device reduces circuit complexity and permits the use of less costly and more mature system components.

The byte-wide 27513 is a paged version of the 27512 512-kbit EPROM. Only 14 of its 16 ad-

dress bits are needed to access its full 64 kbytes, since it reserves on-chip latches for the two highest-order bits. Its 16-kbyte page size satisfies a variety of system requirements. A smaller page would entail too frequent page changes. A larger one would leave too little room for addressing RAM—which in a representative 8085-based system requires 48 kbytes of the microprocessor's 64-kbyte address space (Fig. 1). In fact, the microprocessor treats the EPROM as if it were a fourth bank of 16-kbyte RAM and selects it by writing to a 2-to-4 decoder.

The main difference

The primary operational difference between the paged 512-kbit device and linearly addressed EPROMs, including the 27512, lies in page selection. First the microprocessor sends the EPROM 2-bit page data over the lowest-order data bits, D_0 and D_1 . Next it enables the memory by setting the Chip Enable ($\overline{CE}$) line low via the 2-to-4 decoder. Then it brings the Write Enable line ($\overline{WE}$) low also, thus clocking the page data into the chip's 2-bit address latch. Thereafter the newly selected 16-kbyte page can be accessed during conventional EPROM read cycles. The address inputs during page selection are in a "don't care" state.

During power-up, the EPROM automatically resets itself to page 0 as if the data 00 were being written into D_1 and D_0 . A circuit for clearing the page latch remains active until V_{CC} exceeds

Kurt Robinson, Intel Corp.

Kurt Robinson has served for five years with Intel's nonvolatile memory division, which recently moved to Folsom, Calif. Starting as an EPROM product engineer, he later joined the programmable memory marketing group as an applications engineer. Subsequently he advanced to senior product marketing engineer. His BSEE is from Cornell and his MBA from the University of Santa Clara.

512-kbit EPROM

4 V. Above that level, system control signals remain sufficiently stable to avoid inadvertent page selection.

The 4-V level is also low enough to prevent a low-going power-supply glitch from accidentally clearing the page latch. The worst-case voltage for V_{CC} is 4.5 V. The 4 V that clears the page also sets a 500-mV noise margin against supply undershoot, without presenting any danger of resetting the current page to 0.

Programming the 27513 utilizes a proprietary algorithm supplied with all 12.5-V HMOS EPROMs, including the 27512. This algorithm creates 1-ms programming pulses until the byte has been verified, after which it gives a programming overpulse margin of three times the number of initial pulses. A page-select write operation is included at the start of the program and at every subsequent page boundary thereafter. (Fig. 2).

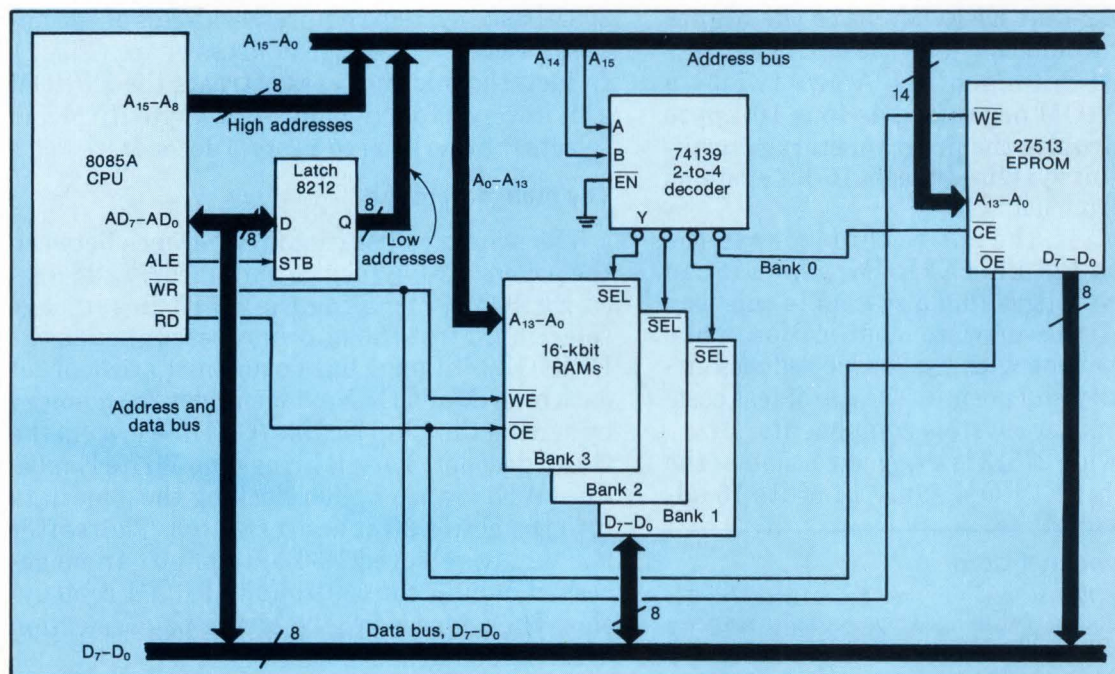
The chip's programming voltage, V_{PP} , is multiplexed with the Output Enable line (OE), and the combined line ($\overline{OE}/V_{PP}$) is brought to 12.5 V for programming and to a TTL low level for verification, as in a normal read. If the chip is disabled ($\overline{CE}$ goes to a TTL high) while $\overline{OE}/V_{PP}$

is at 12.5 V, programming stops.

After each page has been programmed, it undergoes a page-selection write operation, with the write parameters tested in a manner similar to that for static RAMs. Because the chip's page latch is a write-only register, the programmed data is not read back. Instead the memory must be checked for a successful page change. Unique data must appear in at least one physical address on each page; checking that address on each page and finding the unique data confirms that the page programming was successful. Though testing of the write cycle entails reading from specific addresses, an actual write operation is independent of the address inputs.

Simple to substitute

The EPROM chip has a socket footprint almost identical to that of a 128k EPROM, meaning that it can easily be substituted for the smaller device in an existing system. However, some changes in board design are required. For example, the 512k EPROM assigns pin 27 to the Write Enable control signal, as in the JEDEC standard for byte-wide RAMs. In contrast, a



1. An 8085-based system equipped with 48 kbytes of RAM has room only for a 16-kbyte block of EPROM. But the 27513 EPROM packs four such blocks into the space previously occupied by a 128-kbit part. The EPROM resides in memory space from 0000_{16} to $3FFF_{16}$; the RAM occupies addresses 4000_{16} to $FFFF_{16}$.

128k EPROM's pin 27 is set for the program function and is tied to 5 V or V_{CC} . The origin of the Write Enable signal of the 27513 varies, since the chip encounters situations in which code and data must share the same memory map but are selected independently through dedicated selection lines or decoded status signals from the processor.

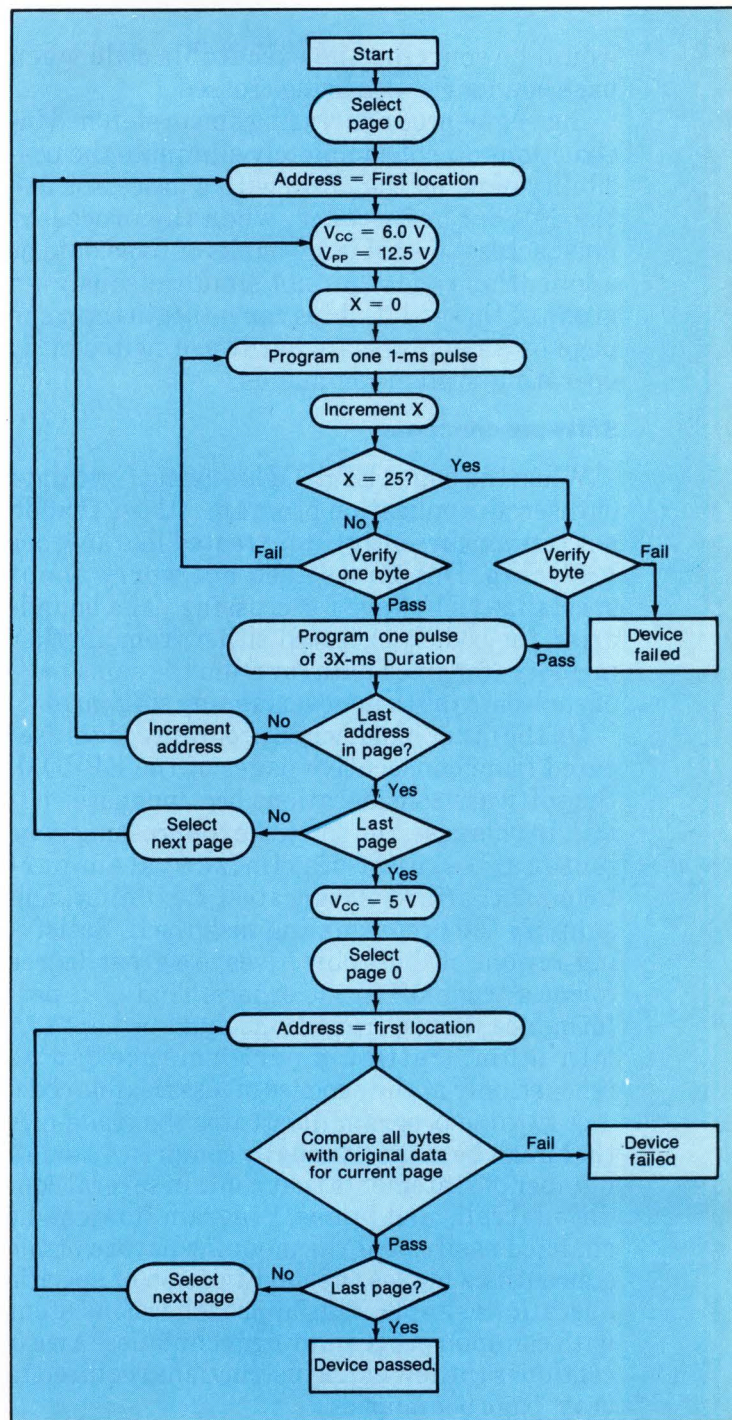
Upgrading a circuit to the 512k EPROM from one designed for a 128k EPROM is dramatically simplified if the socket has been laid out according to the so-called universal site for byte-wide memories. That arrangement brings address and control lines close to the socket, so that different configurations can be selected through jumpers. Designers can access V_{CC} (for tying the program pin of 64k and 128k EPROMs to 5 V) and WE (for byte-wide RAMs) through the universal pin 27. Thus if the socket follows this standard arrangement, the 27513 can be substituted for lower-capacity devices by changing just one jumper.

Superior 16-bit control, too

The paged EPROM can solve the limited addressing range of both 8-bit and 16-bit microprocessor-based systems. That holds true especially for firmware-intensive jobs that tax the 16-bit chip's seemingly adequate addressing range of a megabyte or more assigned to EPROM.

For example, a system tackling frequent transactions can actually eat up most of its total memory address space, which can reach about 16 Mbytes. It may use high-order address lines for specialized I/O and still have enough room for a megabyte each of RAM and EPROM. The code changes required to modify the extremely complex functions of transaction processing might cause even the megabyte of EPROM to overflow. With the 27513, code can be chopped to more manageable levels or rearranged into different memory configurations.

The 512k chip is not suited to all 16-bit systems. Indeed, executing code in the consecutive pages of the segmented chip poses a real challenge to the software programmer of, say, the 80186, which has internal segmented addresses. A high-performance processor like that also prefetches several instructions, making it difficult to know which page in the paged 512k chip



2. A proprietary programming algorithm performs a page-selection write operation at the end of each page in the 27513. The algorithm generates 1-ms pulses until 8 bits have been verified; an overpulse that lasts three times longer than the number of initial pulses gives an extra program margin.

512-kbit EPROM

would be sourcing the executable code when page boundaries are being crossed.

But segmented addressing and prefetched instructions do not completely eliminate the possibility of using the 27513 with a processor like the 80186. For instance, when the processor must access several large banks of fixed data or application code—but not simultaneously—a group of these 512k chips can be set to the same page by an appropriate hardware switch or by operating-system commands.

Software concerns

When the paged EPROM is storing fixed data or discrete application programs (those that do not run concurrently), it is treated like another 128k chip. Designers need not worry about specialized software for crossing page boundaries; the code is executed either from another memory (for fixed data) or from the same page of each chip (as in nonoverlapping software).

On the other hand, when program code is executed from consecutive pages of the EPROM, the software considerations become more critical. In this case, the software for crossing page boundaries must maximize system performance, afford the greatest flexibility, and simplify the programming task itself. Satisfying any one of those objectives to a great degree forms a trade-off in the others. That is, if performance jumps, transitions must be kept to a minimum. Optimum performance can be reached only at the expense of less flexible code.

A flexible program illustrates the trade-offs that must be made. It usually comprises a small number of statements that contain several conditional calls and jumps. Program flow can be changed easily, and the modular nature of the subroutines makes the modification of specific operations simple. This approach is consistent with common programming techniques. An exception is the few extra instructions required to cross page boundaries.

The flexible structure's call sequence is initiated by using the new page number and a lookup table, called offset, for the subroutine address (Fig. 3a). The command Call is issued and the new page selected. However, the current page number remains unchanged. Next, the subroutine Call Address is obtained from the new-page lookup table, as indexed by the

offset table. After a jump to Call Address in the new page, a return is made by jumping to the instruction RETR. The current page number is read, and the chip is reset to the previous page. Finally the program goes back to Return Address in the original page.

If the program branches to a new section of the program and there is no need to return to the previous page, a jump sequence begins. First, the offset table and the new page number are loaded, and the program moves to instruction JUMPR. The new page is now selected and its number stored in the current page location. The jump address is found in the new page lookup table, based on the offset table. A jump is then made to Jump Address in the new page.

Subroutine lookup tables are essential to this most advanced method of page selection, one that involves storing the lookup tables in the EPROM chip itself and reserving a small section of RAM for page-selection code. Although the technique demands more code for the page transitions, the overall amount is reduced by eliminating redundant instructions for common subroutines.

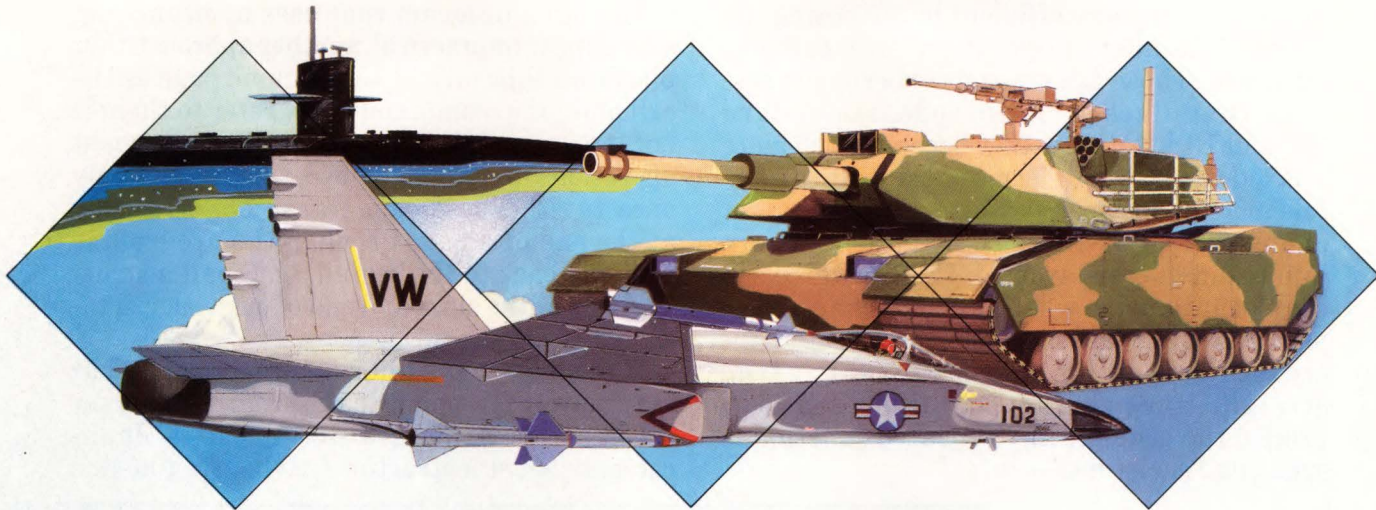
The look-up tables contain the page number and the offset address from which a given routine is called. Within the page containing the actual subroutine code, another lookup table, indexed by the offset value, holds the physical address of the routine. Thus the page number and offset information contained in the other pages remain constant, but the physical address of the actual subroutine can be relocated within its page, even if the code changes. The instructions for handling the page transitions are preloaded into a reserved section of RAM when the system is initialized.

Interrupts anywhere

Interrupt routines can be executed from any page of the EPROM if the current page information is retained. After the interrupt has been serviced, the EPROM is reset to the page and address that were current when the interrupt occurred. Here again, the instructions for handling the page transitions and for calling the interrupt subroutine are preloaded into reserved RAM.

As with the flexible programming structure, designers are typically trying to make their

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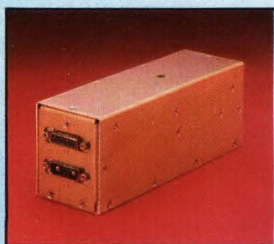
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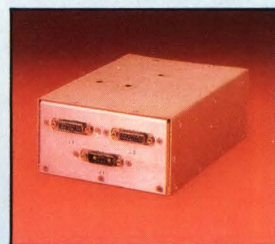
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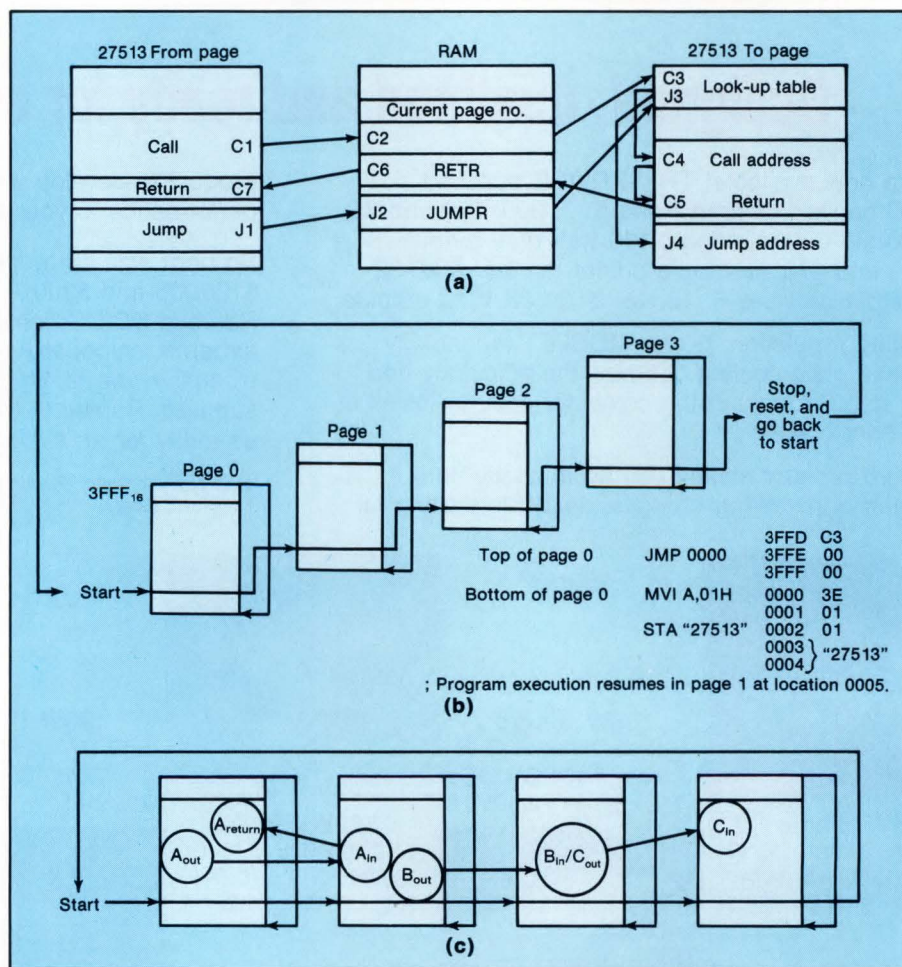
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512-kbit EPROM

program code more efficient by squeezing the greatest number of operations into each instruction. Those are critical concerns for systems that place program code in standard 128-kbit EPROMs, but they become much more relaxed when seen in terms of the 27513's four-fold increase in capacity. Some designers might choose straight-line programming where jumps and calls are avoided. The 27513 excels in that situation, i.e. where flexibility and compactness of code are sacrificed for an overall increase in execution speed (Fig. 3b). A true straight-line program contains no calls or jumps; the code for any repeated function is replicated each time.

Though a program that uses no branching may appear impractical, another approach that places all subroutines in the same page as the call and jump commands that refer to them is not impractical. With that technique, frequent operations are stored on every page—but only once. In either case, page transitions occur only at the end of a page or when the program is jumping back to the beginning. Small instruction sets at the start and end of each page actually shift the pages.

If the page transitions occur frequently but at relatively few points in the program, another scheme—one of moderate complexity—duplicates the set of instructions at the straight-line



3. The program structure of the 27513 can take three forms. A flexible program requires more code for page transitions and eliminates redundant instructions for frequently called subroutines (a). The straight-line approach affords the fastest performance (b). A modification of that structure maintains the speed but adds branching code to deal with jumps between page boundaries (c).

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512-kbit EPROM

program's page boundaries. In that manner, page transitions occur through dedicated portals of code (Fig. 3c).

Enlarging fixed storage

Though the 512k chip will undoubtedly be called to duty for code-expanding missions in popular 8-bit processors, its hardware interface proves equally suitable for applications requiring more storage of fixed data. Suppose that the chip is substituting for several 128-kbit EPROMs in an 8051-based dot-matrix printer. The chip itself provides enough extra storage space that designers can add three new character sets (for example, scientific marks, mathematical symbols, custom shapes). The Write Enable signal derives from the processor's Write/Read line, as with standard data memory.

Likewise, the software interface is not complicated, since the chip is not actually storing code. Pages are selected either by an external hardware switch or by a command from the host computer.

The 27513 is not limited to 8-bit jobs—it makes a valuable addition to a 16-bit system, since it can store firmware for several independent application programs. In fact, it could quadruple the number of programs in, say, an 8088-based system, without increasing the total

amount of physical address space allocated to EPROM. And because the programs are not used simultaneously, the system interface is simple. Each program is selected in much the same manner as for the 8051 character-set storage application.

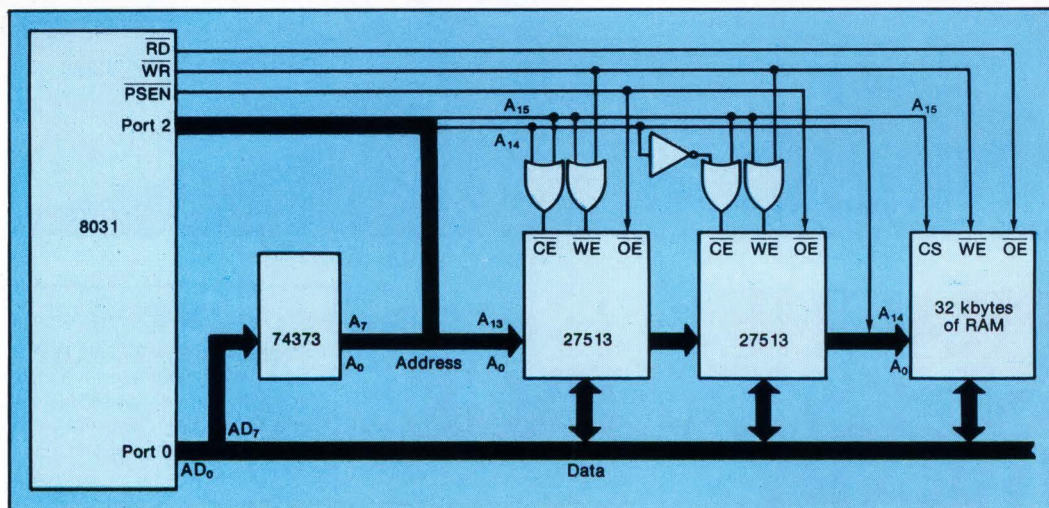
Even a complex chore, such as storing firmware-intensive 8031 applications, need not be a formidable task with the chip (Fig. 4). The 8031 has a special PSEN(Program Store Enable) signal to enable the output of external program memory. Because data cannot be written to the standard program memory, the designer must make sure that the 27513 is subjected to the necessary page-selection write operation.

If the external data memory of the 8031 is not fully used, the EPROM chip's page latch can be addressed as if it were a lower-order bank of external RAM. The A_{15} and $\overline{WR}$ signals can be ORed to generate $\overline{WE}$; alternatively, a specific RAM address can be decoded to generate $\overline{WE}$. That would reduce the amount of RAM address space allocated to the 27513 but at the expense of additional decoding circuitry. □

How useful?

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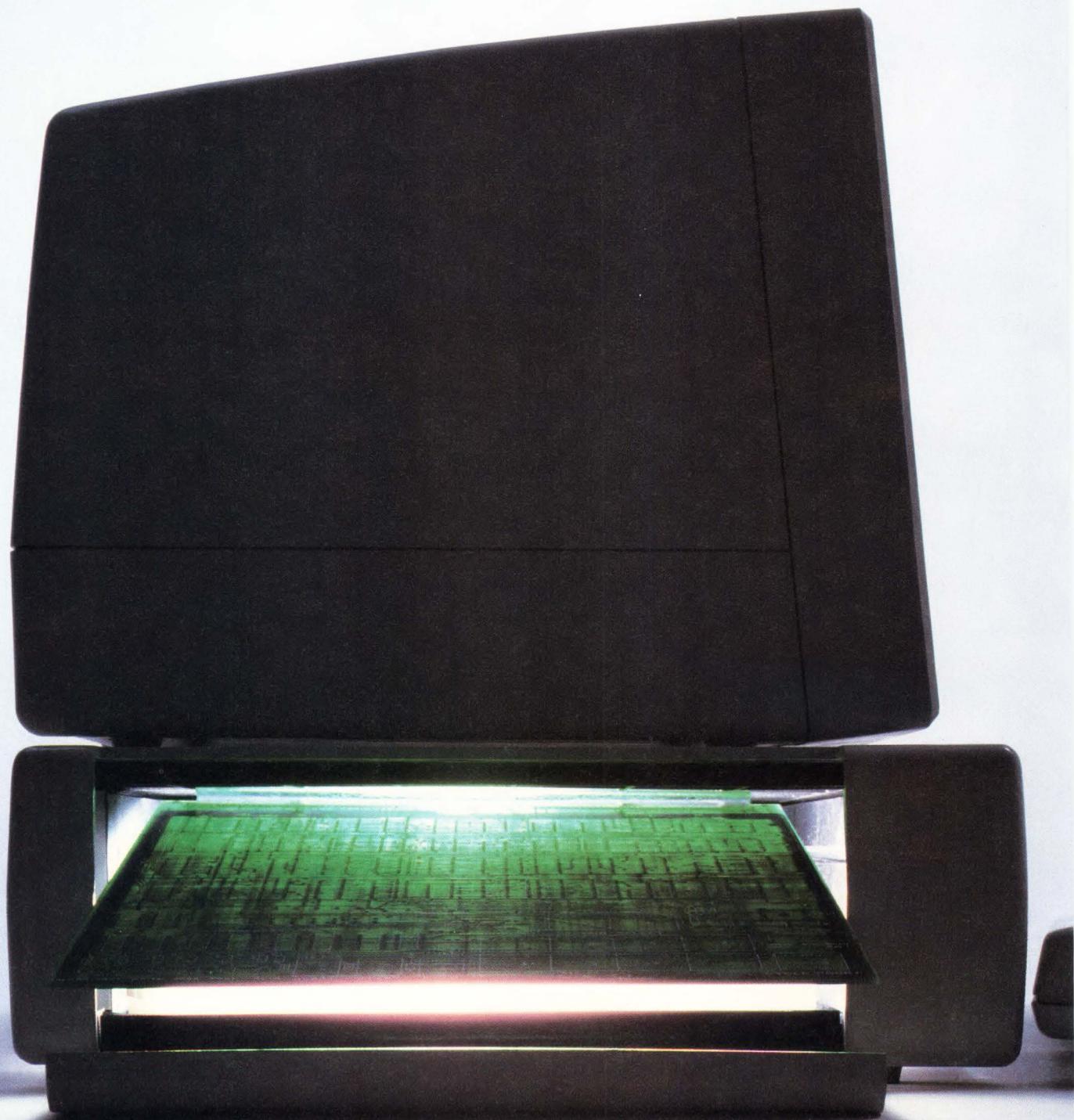
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Within the next year	551
Not applicable	552



4. Although some processors do not make a perfect match for the 27513, provision can be made for the EPROM's requirements. Here the memory's page latch is addressed as if the chip were a low-order bank of external RAM. ORing the processor's A_{15} and $\overline{WR}$ signals generates the 27513's $\overline{WE}$ signal; line A_{15} determines whether the RAM or EPROMs are selected. Chip-enable signals for the 27513s are decoded from lines A_{14} and A_{15} .

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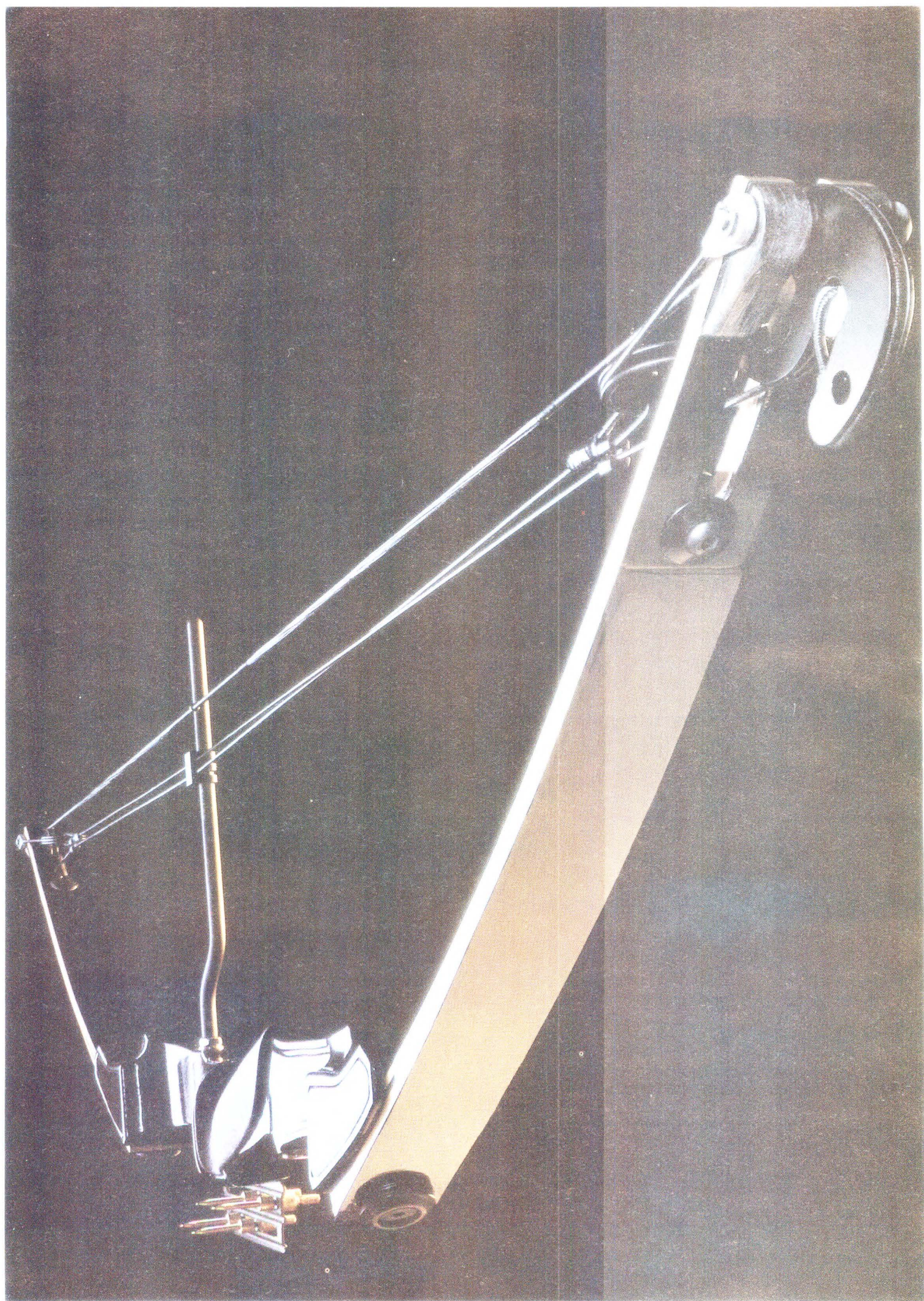
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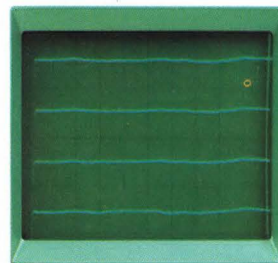
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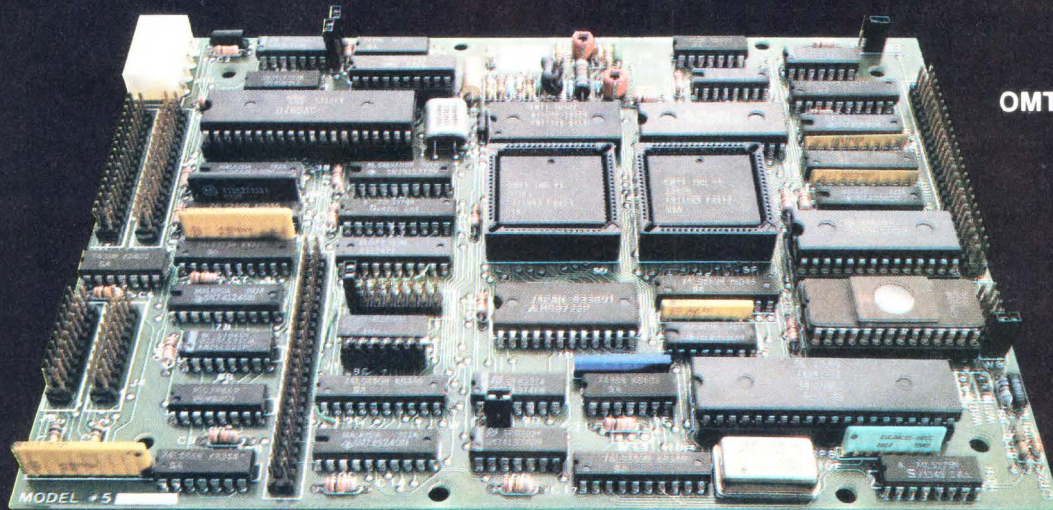


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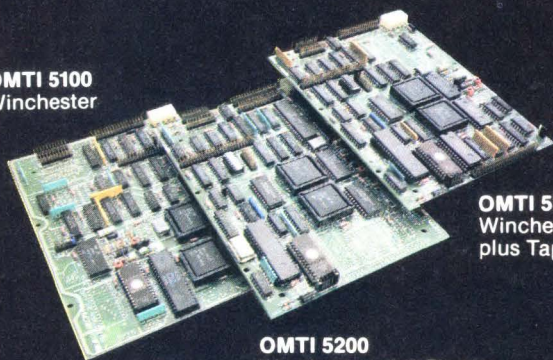
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Complementary MOSFETs make switched and linear power control easier

A single TO-220 package and a common heat sink also ensure that a pair of p- and n-channel power DMOS FETs remain matched as temperature changes.

Today's double-diffused power MOSFETs can handle a lot of power in linear and switching applications, some of which demand the use of paired p- and n-channel DMOS devices. But finding the right complementary pair is not easy, especially if the two must be matched for both dynamic and static characteristics. Moreover, to ensure that they stay matched as temperature varies, two power packages must then be mounted on one heat sink.

The members of the MPP500 family of power MOSFETs each contain two DMOS FET dice, one p-channel and the other n-channel. Instead of needing separate packages, the dice are seated side by side in one TO-220 package with five leads, and they share the same heat sink.

The result looks just like a CMOS logic inverter with the usual common drain

connection—except that it can dissipate 20 W. Also, since the two dice are the same size, their input capacitances are virtually identical, and the resulting symmetry of their waveforms when they switch on or off simplifies the design of gate-driving circuits in switching applications.

Each die can dissipate the full 20 W when required to do so, since at any given time only one of the transistors in a given pair should be conducting. However, the fact that the dice are the same size exacts a slight penalty: Because of the difference in carrier mobility between p- and n-channel transistors, their on-resistances are 1.5 Ω for the n-type die and 4 Ω for the p-type die. As for breakdown voltages, they run from 60 to 100 V for the three present members of the MOSFET family.

Applications for these power CMOS-like units range from linear circuits, such as fast high-power operational amplifiers, to digital setups in which logic signals must drive a highly capacitive load, such as the gates of 200-A MOSFETs. The complementary pair is also extremely useful in the design of switching-control circuits for ac motors, an application that may be viewed as solving analog design problems with digital techniques.

Essentially these units can be used as if each die of the pair was an independent device. Nonetheless, as with any other complementary power circuit, a little care must be taken. In par-

Ray Ruble and Mark Alexander, Siliconix Inc.

A well-known expert in switching power conversion, Ray Ruble designed one of the first commercially successful MOSFET power systems. Now working on power circuits with design engineers at Siliconix in Santa Clara, Calif., he has held positions at Litton Guidance Control Systems and EG&G Almond Instruments and published many papers on the subject.

Mark Alexander worked at Sangamo Canada and Motorola Canada after obtaining a bachelor's in electrical engineering from the University of Toronto. Now, as an applications engineer at Siliconix, he researches and writes about power MOS and analog circuit design.

Power CMOS-like pair

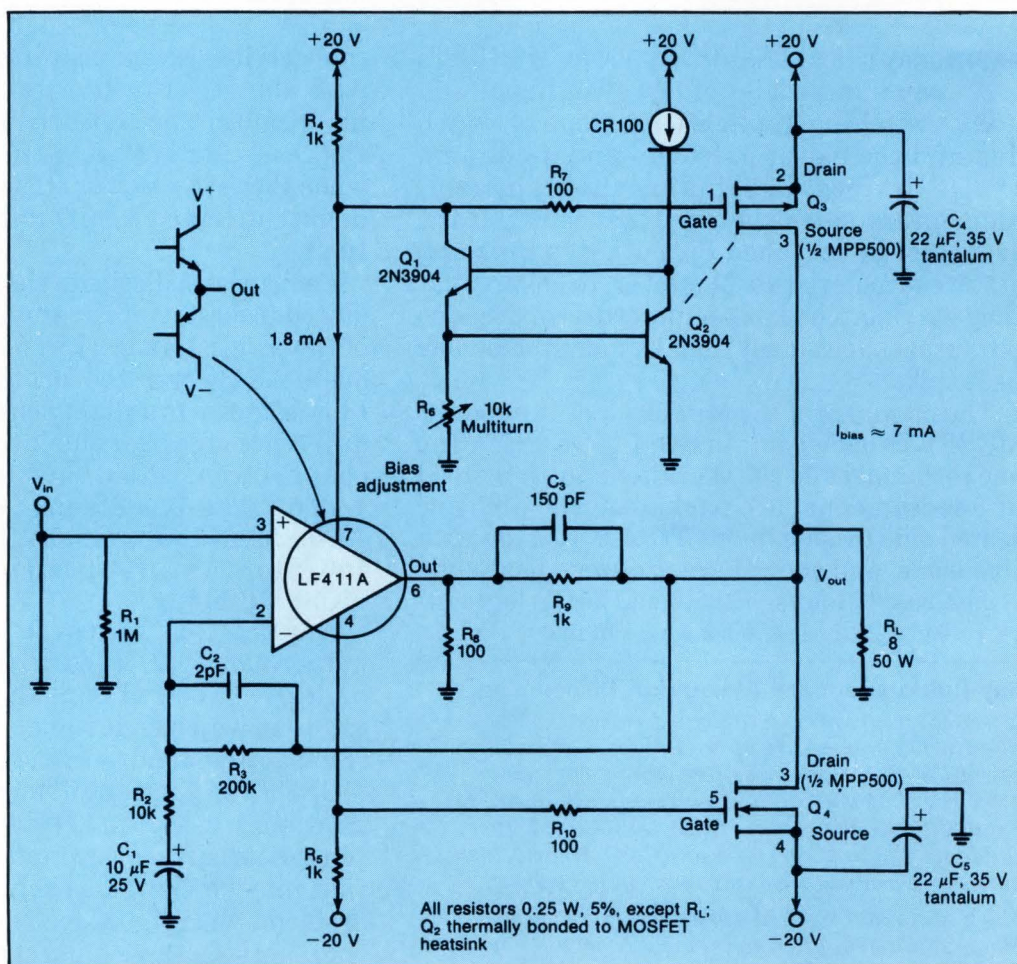
ticular, the gate drive in switching circuits must ensure that both devices are never on at the same time (or at least not on at the same time for very long or very often). In addition, when the package is used in linear circuits, a few analog design tricks are necessary to eliminate crossover distortion and maximize gate drive with minimum power-supply voltage.

Linear amplification at low cost

Many fast, high-gain, precision monolithic op amps are available today at low cost. But because of their miniature size, their output transistors are so small that they usually cannot deliver more to a load than 5 to 20 mA at about ± 10 V. Power hybrids are an option, but they are expensive. The MPP550 family, in contrast,

can be used to build a low-cost linear amplifier around a low-power biFET op amp with the help of a few discrete transistors and a few passive parts. A high-performance circuit results because the MOSFETs are inherently linear devices (Fig. 1).

This amplifier circuit, incorporating as it does an LF411A from National Semiconductor, may at first glance look familiar. But a closer look reveals something quite different—the gates of the complementary power MOSFET pair are driven from the power-supply terminals of the op amp, not from its output. This approach is mandatory because of the MOSFETs' built-in common drain connection, which forbids the conventional common-source-follower configuration. However, the



1. The MPP500 power CMOS pair can build a power amplifier when aided by a low-cost operational amplifier (the LF411A) and a few discrete parts. The final circuit can drive an 8- Ω load with 12 W at 20 kHz.

MPP500 circuit—a noninverting approach providing a closed-loop gain of 21—has several advantages over the more familiar designs.

The conventional source-follower circuit has a voltage gain of unity and a substantial dc threshold voltage. Both characteristics demand peak gate-drive voltages from the op amp that are several volts higher than the output at the sources of the FETs. Also, the output of most op amps swings only to within 2 V of the supply rails. Thus the peak voltage swing at the output of the power MOS follower amplifier is significantly less than the span between the supply rails—a waste of capability.

The circuit chosen suffers from none of these limitations. Both the op amp output stage and the MOSFET current booster provide voltage gain. The op amp's output stage becomes an inverting common-emitter phase splitter, while the MOSFET current boosters represent an inverting common-source output, a linear application of a CMOS inverter.

What makes this circuit possible is the fact that the collectors of the output transistors in nearly all monolithic op amps are connected directly to their respective power supply terminals. The collector load resistors— R_4 and R_5 —are connected between the op amp's supply rails. Gate-driving and gate-biasing voltages are developed across them. Since the bias voltages are referenced to the power-supply rails rather than to the output voltage, a much larger peak swing is possible.

In this application, peak gate-to-source enhancement voltages in excess of 10 V are applied to each FET. The output swing of the amplifier is limited only by the peak output current multiplied by the FET's on-resistance, $R_{DS(on)}$. For example, the circuit shown swings from -17 V to $+15$ V, supplying up to ± 2 A to the $8\text{-}\Omega$ load.

Compensation required

Although the LF411A op amp is compensated internally and has a stable unity gain, the circuit still needs two compensation capacitors, C_2 and C_3 . Without them, the amplifier would oscillate, because the additional gain from the FETs reduces the phase margin. Also, the output stage adds an extra pole, further reducing phase margin. The additional gain is set at

about 5 by R_8 and R_9 , and the new pole is at about 1.53 MHz. However, the compensation capacitors move that pole to 52 MHz. The final amplifier has a unity-gain frequency of 2.25 MHz and a phase margin of 90° —very stable operation. Potential parasitic oscillations are suppressed by the $100\text{-}\Omega$ resistors in the gate leads of each FET.

The network R_2 - C_1 limits the amplifier's low-frequency response to about 1 Hz, where it starts to drop off at 6 dB/octave. If dc response is required, this network can be eliminated, but provisions must be made to zero the offset of the op amp. To run the FETs at more than ± 20 V, a zener diode must be inserted between each collector load resistor and its respective op amp supply pin. For example, if the drain voltage is raised by 20 V, the designer must use 20-V zeners.

Quiescent bias current for the op amp flows through collector load resistors R_4 and R_5 . However, the low supply current of the LF411A (typically 1.8 mA) ensures that the voltage across them can be reduced to less than the typical MOSFET threshold of ± 2 V. When the bias-adjusting trim potentiometer (R_6) is set

Table 1. Performance of amplifier built with MPP500 and biFET op amp*

Parameters	Values
Output voltage swing	$+15$ V, -17 V (12 W into $8\text{ }\Omega$)
Slew rate	$37.5\text{ V}/\mu\text{s}$
Overshoot	None
Bandwidth, -3 dB	360 kHz
Dc offset	0.22 mV
Noise (100-Hz band)	100 dB (below 1 V out)
Harmonic distortion (12 W output)	0.0036% at 100 Hz 0.0200% at 1 kHz 0.2000% at 10 kHz 0.3800% at 20 kHz

*Applies to circuit shown in Fig. 1

Power CMOS-like pair

for minimum bias, the FETs should be non-conducting. In some circuits the values of R_4 and R_5 may also have to be adjusted to ensure that the MOS transistors do turn off.

Stabilizing zero

Transistors Q_1 and Q_2 form a variable, supply-independent current sink tied to the positive supply pin of the op amp. As the value of R_6 is reduced from its maximum, the additional current drawn through R_4 by Q_1 increases. When the voltage across R_4 reaches the threshold voltage of the p-channel FET, its current starts flowing, forcing the output of the amplifier positive if the n FET is conducting less current than the p FET, and vice versa. Since the amplifier's output is dc-coupled back to its inverting input, the voltage across R_5 forces the n FET to conduct the same current as the p FET. As a result, the circuit's no-signal output sits at zero volts.

Transistor Q_2 also compensates for the changes in MOSFET idling current that occur with temperature when the gate-to-source voltage is constant. Because threshold voltage de-

creases by about $5 \text{ mV}/^\circ\text{C}$, idle current increases correspondingly. This situation can be remedied if Q_2 is attached to the MOSFET pair's heat sink. Then, as Q_2 's base emitter voltage decreases (by about $2.2 \text{ mV}/^\circ\text{C}$), the collector current of Q_1 falls, raising the gate voltage of the p FET and keeping its idle current constant.

For a total quiescent current of 10 mA in the amplifier, the ratio of R_4 to R_6 is chosen to be about 1.5 to 1, producing a voltage change across R_4 of $-3.3 \text{ mV}/^\circ\text{C}$. For instance, after 12 W has been put into an 8- Ω load for half an hour in an ambient temperature of 25°C , the MOSFET case rises to 70°C and the heat sink to 54°C , but idling current increases only by 2.2 mA.

The overall performance of this amplifier, built with just four active devices and for less than \$25, is significant (Table 1). Of particular note are the high slew rate and low distortion when the amplifier is driving a low-impedance load.

For efficiency's sake, digital data transmission schemes and power control circuits require that large capacitive loads be driven while the pulse rise and fall times remain very short. Examples include superlarge power MOSFETs, coaxial cables, piezoelectric transducer arrays, and laser diodes. Also required in most of these drives are logic compatibility and a peak output sink or source current that is large enough to ensure rapid transition of voltage changes across the load.

Fast delivery

To solve these problems, the new switch may be configured as a power CMOS logic inverter that delivers high output current quickly (Fig. 2a). This circuit easily generates a peak output current of several amperes with a very short propagation delay. As shown, though, it has one disadvantage. Because the gates of both FETs are tied together and driven by one waveform, substantial crossover current flows while one FET is turning off and the other is turning on. On the average, that current is proportional to the operating frequency of the circuit, and it may destroy devices if allowed to reach an excessive value.

A somewhat more complex circuit employing

Table 2. Switching times of MPP500 using anticrossover-current circuit*

Load capacitance (pF)	Output rise time (ns)	Output fall time (ns)
0	6	5
100	7	5
300	9	7
1000	15	11
2000	23	17
4700	37	28
10,000	72	46
20,000	132	78
50,000	280	130

*Applies to circuit shown in Fig. 2b

three standard ICs eliminates the crossover circuit (Fig. 2b). Here the waveforms driving the gates of the FETs do not overlap: One FET is always fully turned off before the other is turned on. The required dead time between gate waveforms is generated by a circuit often used to produce two-phase, nonoverlapping clock

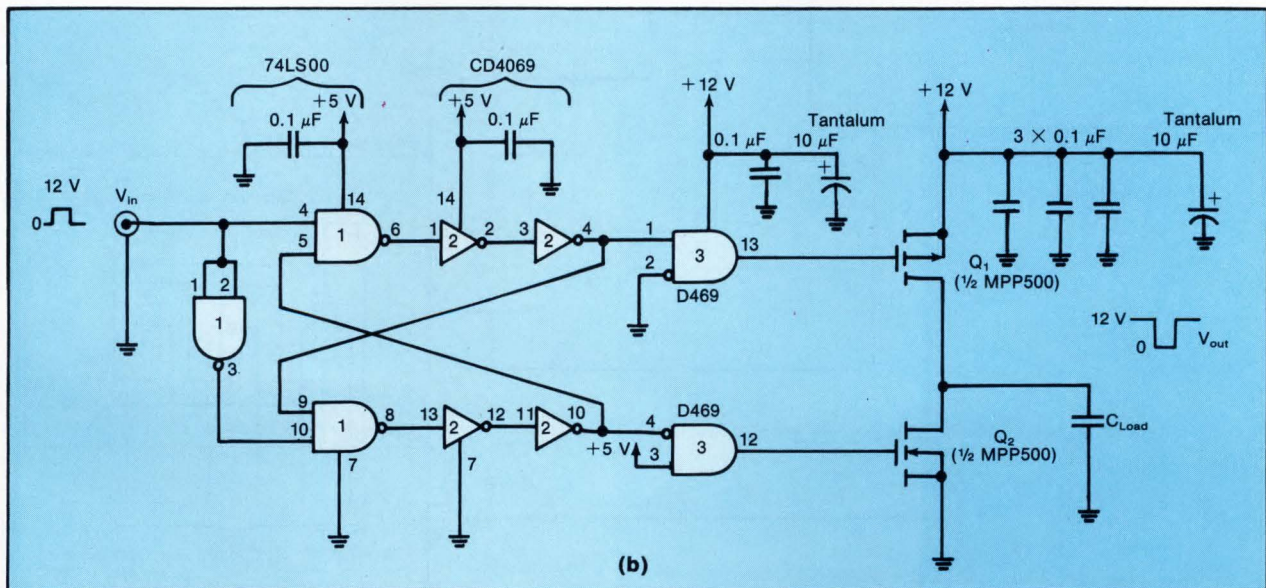
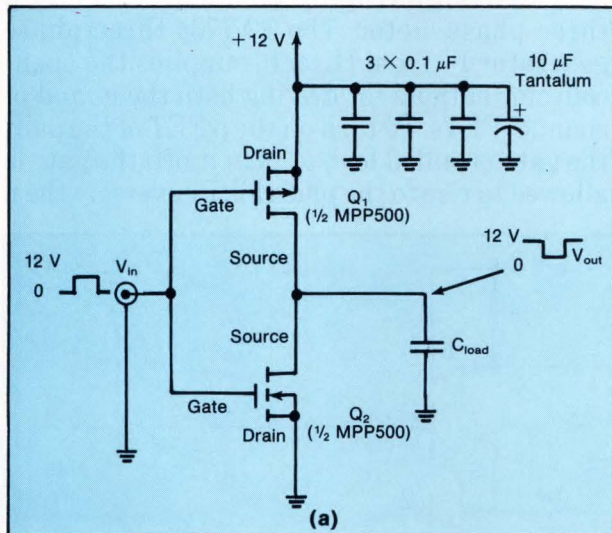
signals in MOS logic systems.

The 74LS00 forms the basic cross-coupled NAND-gate pair, while the four sections of the CD4069 become a dual delay line. The waveforms at the outputs of each of the inverter pairs have approximately 40 ns of dead time between them, and they are 180° out of phase. Two sections of a Siliconix D469 quad driver then buffer the outputs of the delay lines and invert one so that the gate waveforms are both in phase.

The results are impressive (Table 2). Even when the circuit is driving a capacitance of 50,000 pF, the rise time is 280 ns and the fall time 130 ns. At 100 pF, the respective times are merely 15 and 11 ns. An additional propagation delay of 170 ns occurs as the waveform passes through the hex inverter and the quad driver.

Ac vs dc

In many applications ac motors have significant advantages over dc. Not only do the brushes and commutators of dc machines cause noise and maintenance problems, but multiple motors can also be virtually impossible to synchro-



2. One MOSFET pair can easily drive a high-capacitance load, such as a coaxial cable (a). Since both gates are driven by the same signal, destructive crossover currents could occur when one FET turns off while the other turns on. A revised circuit produces a delay in the gate-drive waveform for each FET, so that the transistors are never conducting current simultaneously (b).

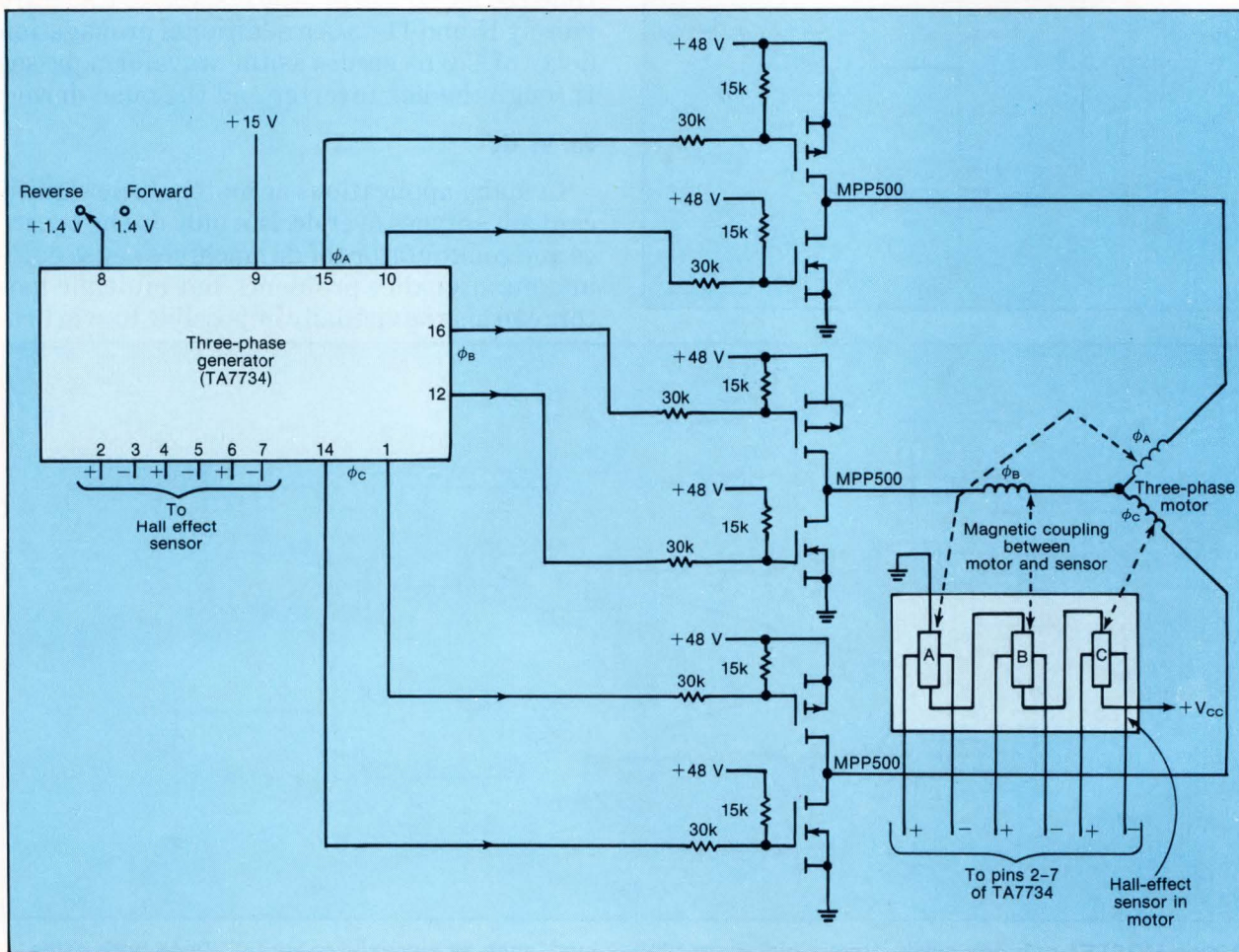
Power CMOS-like pair

nize. On the other hand, ac motors synchronize handily, but controlling their speed has, until recently, been very difficult to achieve. Several switching types of control ICs can now set and even vary the speed of polyphase ac motors.

A major handicap of these controller chips, however, is that they typically can handle only a few hundred milliwatts to a few watts of power. But when a paired MOSFET switch is added to each of the three-phase outputs of the controller chips, a different story unfolds. Speed control of ac motors is now easy and reliable because power MOSFETs turn off fast every time—without complex turn-off circuits. In ad-

dition, the current required to drive the FETs is small enough for many paired MOSFET switches to be driven in parallel from the same controller. Thus two or more motors may be driven in synchrony.

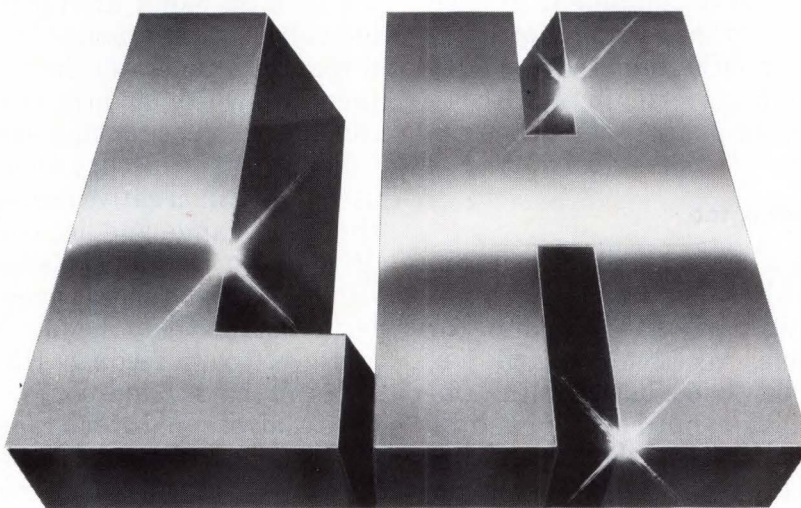
A simple open-loop, constant-speed control system with forward and reverse capability is easy to design (Fig.3). It can drive a 1/4-hp three-phase motor. The TA7734 three-phase generator IC from Hitachi supplies the open-collector outputs for driving both the n- and p-channel FETs. To turn on the p FET of the pair, the gate is pulled low; to turn it off, the gate is allowed to rise to the plus rail. Conversely the n



3. Three complementary pairs of power p-channel and n-channel MOSFETs, driven by a TA7734 three-phase generator, can run a 1/4-hp three-phase motor.

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Power CMOS-like pair

FET is turned on when its gate is high and off when low. In this circuit the p-channel device has the job of sourcing field current through the motor, while the n-channel device sinks the field current.

The more phases driving an ac motor, the higher the motor's efficiency. To take advantage of this feature—and of solid-state electronics—six-phase motors with fractional horsepower are under development. If each open-collector output of the control chip drives an inverter (such as a 74C04 followed by a D169 dual-drive IC), and this inverter in turn feeds a pair of MPP500s, a six-phase motor-drive circuit results (Fig. 4).

Variable speed-control, too

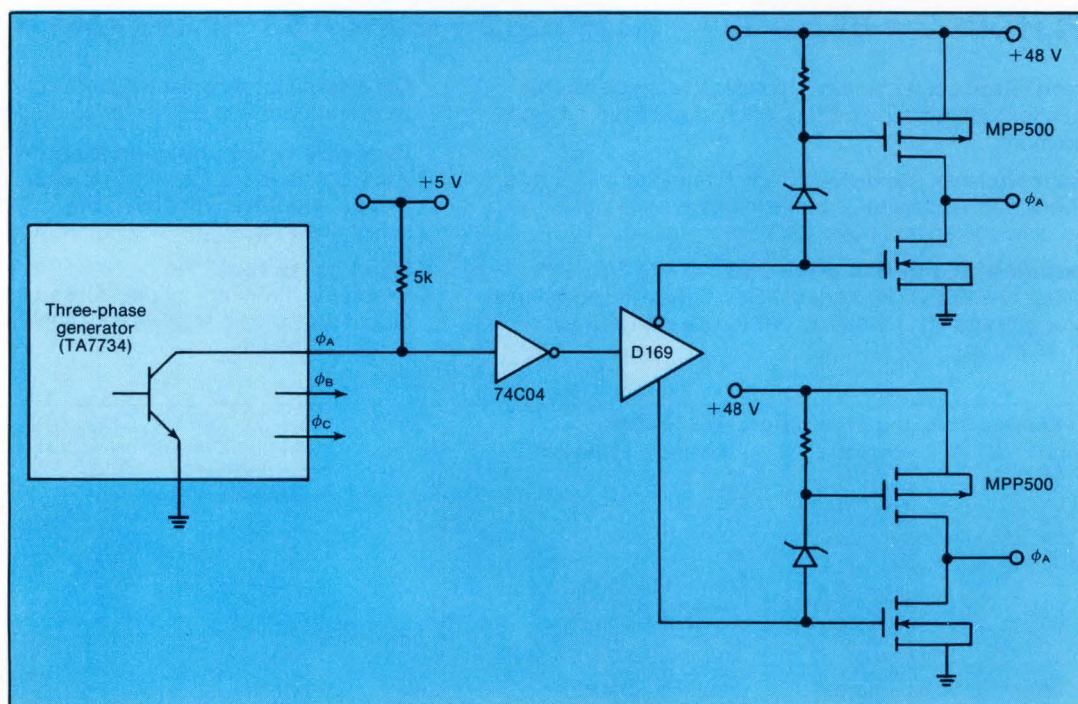
In these systems, a power MOSFET pair controls each motor phase, and a single three-phase generator chip drives all three pairs. For the simplest systems, this circuit does the job. When speed must be varied, however, the amplitude of the voltage applied to the motor windings must rise and fall as the frequency of the drive rises and falls, since the drive sets the

speed. Otherwise either the iron in the motor will saturate at low speed, increasing losses, or only limited power will be available at high speed.

This variable voltage is obtained from an extra pair of power n and p MOSFETs and a PWM25 pulse-width modulator, which creates a full-bridge dc-to-dc converter. The converter (blocks A through E in Fig. 5) supplies the drains of the motor-driving FETs with a variable voltage that tracks the frequency of the three-phase generator. Both the converter and the pulse-width modulator are driven from a common reference or command voltage.

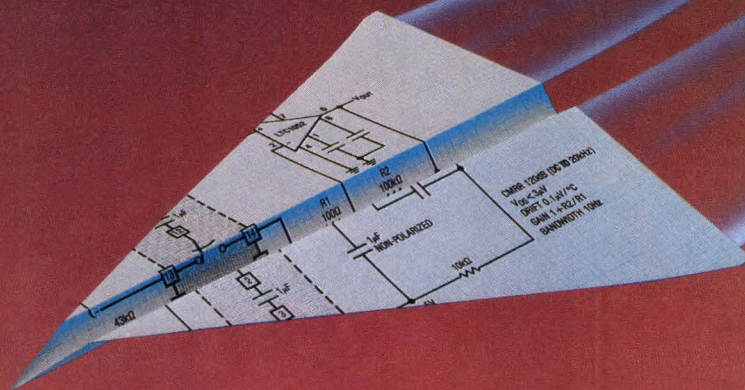
For variable speed, either technique may be used to obtain negative feedback, depending on the speed range and accuracy required. For drive systems needing between $\pm 1\%$ and $\pm 3\%$ regulation over a speed range of 20 to 1, Hall effect sensors will do the job. A variable dc control level (coarse feedback) to the two generator ICs is all that is required.

To control speed over a range of 1000 to 1 or to hold it to an accuracy of 0.01%—or both—a little more is needed. In these cases, the inductive



4. All that a three-phase generator chip needs to drive a six-phase rather than a three-phase motor is an additional phase-splitting circuit composed of an inverter and a D169 driver. This circuit is one of six possible phase splitters.

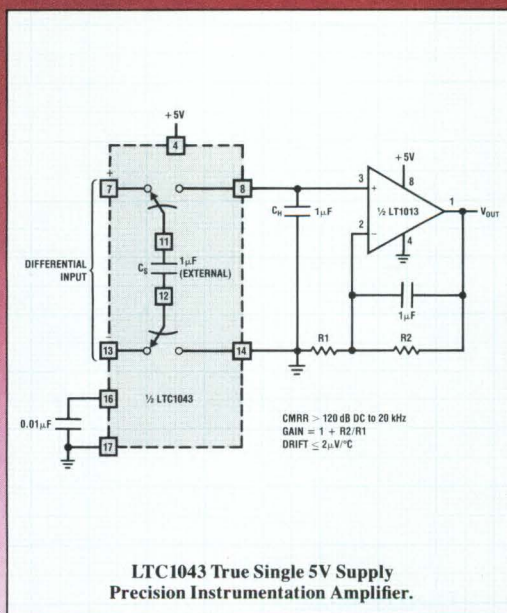
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Power CMOS-like pair

pickup and phase-locked loop are used.

If more than one motor must be driven by the system, several approaches are possible. First, two or more motors can simply be connected in parallel to the three-phase lines. Second, if that setup overpowers the MOSFET pairs, other pairs can be added in parallel, as with any other power MOSFETs. On the other hand, the TA7259 can easily drive as many as 100 sets of MPP500s. Each trio of FETs is then dedicated to its own individual motor. As shown in Figure 5, these techniques can be combined.

Finally, it is possible to build a control system in which the individual motor shafts turn at several different speeds. To do this, frequency dividers are interposed between the three-phase generator and some of the motor-driving

pairs. One or more dc outputs with lower voltages are added to the dc-dc converter. Though the speeds of the motor shafts vary, the shafts are synchronized without use of gearing, and all motors have the same number of poles. Thus identical motors can be used throughout a multispeed system. □

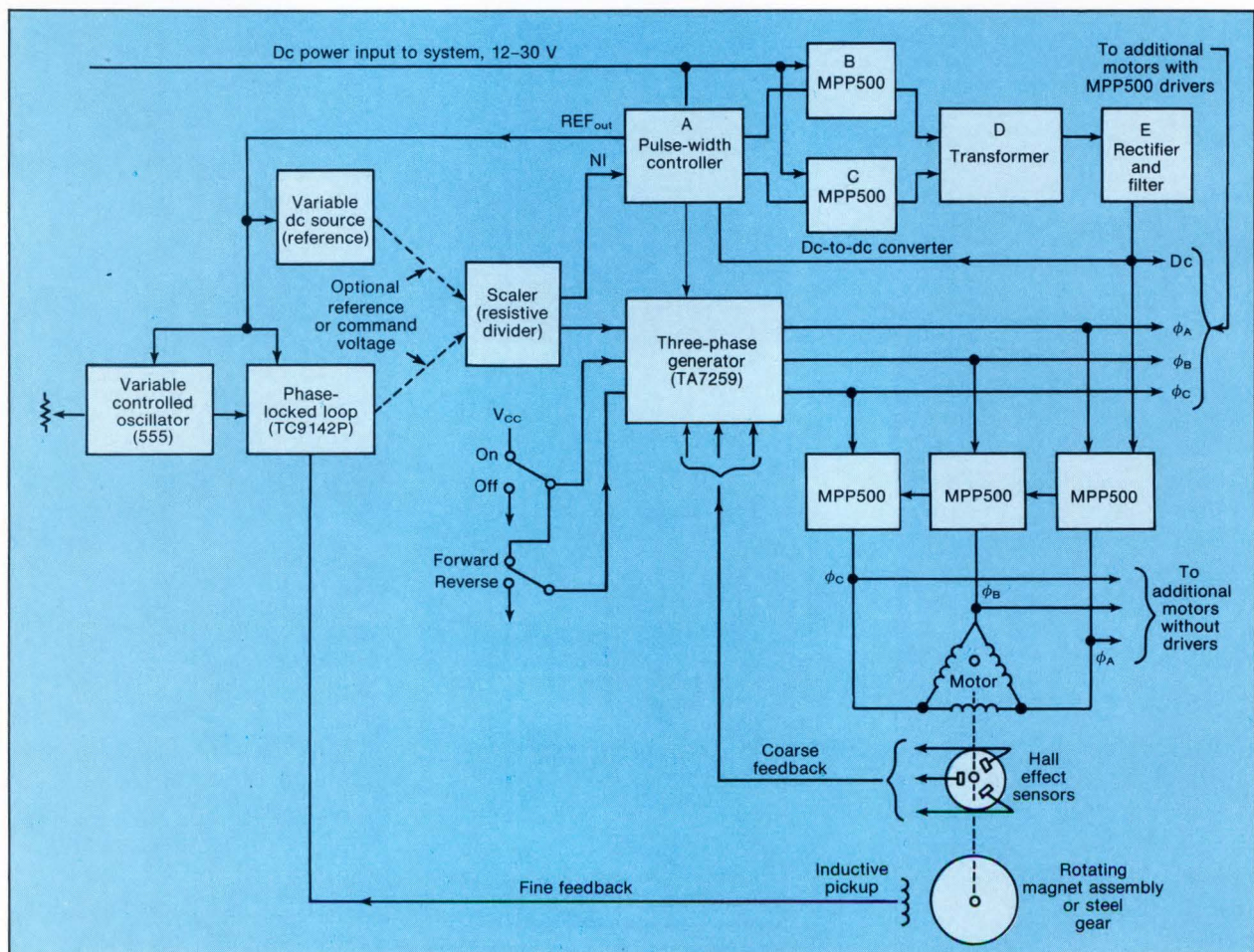
The authors wish to thank Dick Blanchard, vice president of design and advanced technology development, and Ed Orner, staff engineer, for their support and contributions.

How useful?

Circle

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553
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555



5. To build a variable-speed control system, a dc-to-dc converter with a variable voltage output is added to a constant speed system. The resulting outputs varies the voltage on the motor windings as a direct function of speed. That voltage is then applied to the windings through the MPP500 power n and p MOS drivers.

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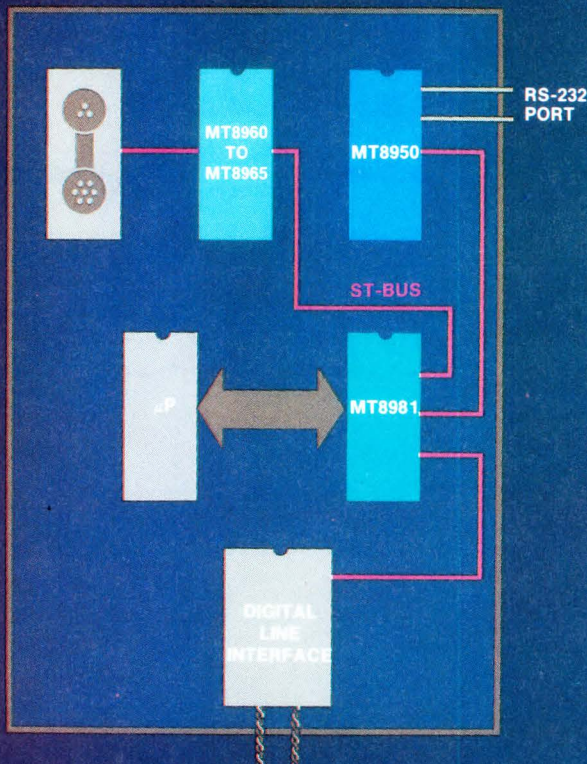
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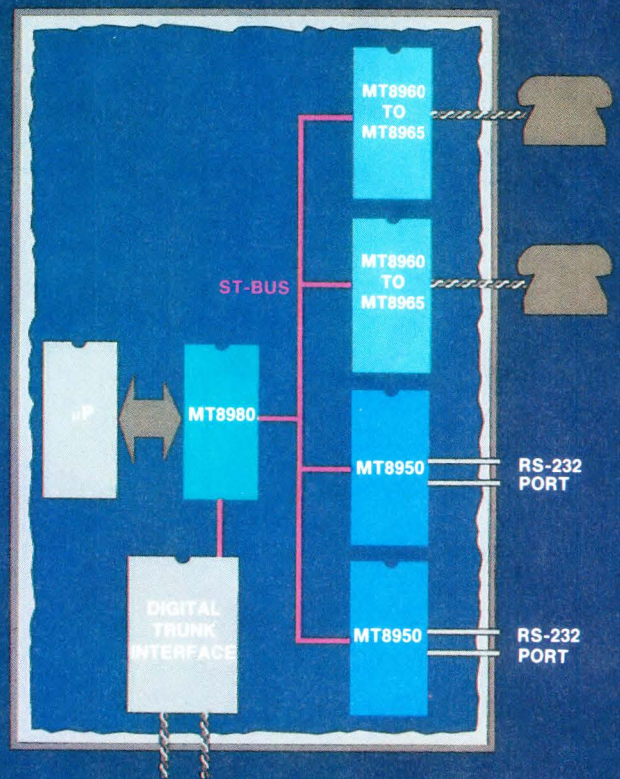
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Systolic array chip recognizes visual patterns quicker than a wink

Simultaneously processing a host of pixel values, a monolithic systolic array gives pattern recognition systems the get up and go to work in real time.

The third article in a series dedicated to the first commercial systolic array processor focuses in on pattern recognition. The first (Oct. 31) introduced the chip and the second (Nov. 15) investigated its use in image manipulation. Forthcoming discussions will explore using the chip as an associative memory unit and an associative processor, as well as data-base management.

Pattern recognition is a simple concept that lets automatic inspection and image-processing systems emulate the cognitive talents human beings take for granted. Working with it, a system looks at an object, determines what it is—often improving the image sent to it in the process—and establishes if the object under scrutiny meets specific criteria.

A multitude of algorithmic approaches and

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Paul Sullivan is the business unit director for the digital signal-processing devices group at NCR's Microelectronics Division in Fort Collins, Colo. He holds a PhD and a MSEE from the University of Southern California and a BSEE from Colorado State University. Before NCR, he worked for Hughes Research Laboratories.

hardware architectures have been tried in the attempt to let machines quickly convert data from sensors into information that can be used to decide on the next action. The Geometric Arithmetic parallel processor (GAPP), a CMOS chip that carries 72 single-bit microprocessors that run in parallel, is suited to many of these schemes.

Its multiple data paths make it right at home in a range of settings, allowing designers to turn to a single device instead of to a number of dedicated pieces of hardware. Further, specific algorithms can be assigned to various tasks, since the software for the array has more in common than do programs designed for unrelated hardware.

Despite the assortment of algorithms devoted to pattern recognition, the approach can generally be broken down into two categories—template matching and feature matching. The first scheme is the most straightforward. Using it, a system simply compares an incoming image to those stored in memory until the matching pattern, or template, is found.

Feature matching is more sophisticated and thus demands more processing power. In it, the system views the length, width, and other characteristics of an object to determine what it is without comparing it to a template.

Either technique can be readily handled by the systolic array. Both comprise four basic tasks, or blocks—improving, screening, ex-

Systolic array chip

tracting, and deciding (Fig. 1). Each may be processed by a dedicated hardware component, or two or more tasks can be processed by the same hardware.

The improver block accepts raw data from the sensor, in many cases, a camera. Then it either restores the signal, correcting degradations caused by the sensor, or enhances it, boosting the quality of the image to facilitate further processing. Signal restoration typically encompasses image deblurring, while enhancement includes edge enhancement or smoothing.

The data is then passed along to the screening block, which removes the information not required for the sophisticated algorithms that follow. Among this extraneous data is both noise and pixels below a given threshold.

The extractor pulls out the primitive characteristics that can be used by the decider to recognize the object. And the final block, the decider, looks at all the characteristics and attributes gathered concerning the object and its surroundings, compares them with its understanding of the object's features, and decides whether it recognizes the object.

The systolic array chip can be put to work in any of these blocks and is easily configured to process all of these sequential steps at the real-time rate of most video cameras (10 MHz). At

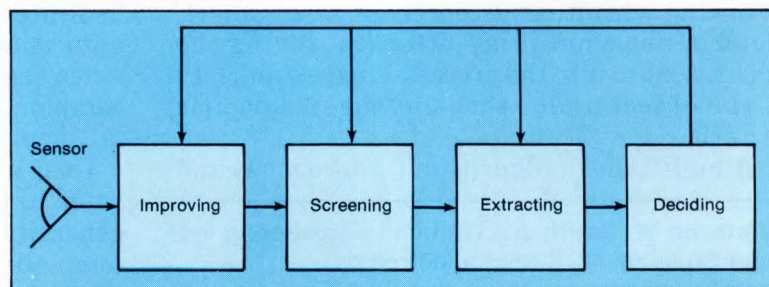
present, they are handled by the hardware architecture deemed most appropriate for the task at hand. Both improving and screening are high-speed computations that involve a small number of dedicated algorithms, so they are generally handled by pipelined processors. Extracting and deciding are usually taken care of by parallel microcomputers because of the wide variety of algorithms and different types of computations they involve.

Process in parallel

Another scheme, massively parallel processing, dedicates one processor to every pixel in an image, thus ensuring very high speeds. The systolic array goes with this approach; consequently, designers have that particular architecture available in relatively small systems.

In practice, arrays can be grouped together until the number of processor elements matches the number of pixels being processed. Further, each of the chip's 72 processor elements has 128 bits of dedicated RAM, which gives it an additional level of flexibility. This internal memory also increases throughput by eliminating the time-consuming data fetches required with typical von Neumann processors.

The array's single instruction, multiple-data



1. After data is picked up by a sensor, the typical pattern recognition system processes it in four sequential tasks—improving, screening, extracting, and deciding. Any of the four can be handled by the Geometric Arithmetic Parallel Processor, set up as a dedicated hardware component. Alternatively, two or more tasks can be shared by the same hardware.

path is particularly well suited to the aforementioned task of improving, since the algorithms used for it demand pixel processing using only local comparisons to determine the value of a pixel. This so-called neighborhood processing takes advantage of the structure of the chip, in which each processor element communicates with its nearest neighbors on the north, south, east and west.

Back to basics

One of the most fundamental algorithms used in restoration consists mainly of adding successive frames of the same image (on a pixel-by-pixel basis) to yield a running average. Doing so improves the signal-to-noise ratio of the image, making it easier for the system to process and making it more visually pleasing to the operator overseeing the task on a display.

The actual code used to add two 8-bit images (see Program 1) assumes that the first is stored in RAM locations 0 to 7 (with the MSB at the highest location) and that the second is stored in RAM locations 8 to 15 (the MSB here is held in location 15). It also takes for granted that both words are positive. Simple extensions, though, allow negative numbers to be added or subtracted.

When the 25 instructions are finished, the two input images remain in the same RAM locations, while the sum of the images is stored in locations 16 to 24. The number of instructions needed to add an m-bit number to an n-bit number, where $n \geq m$, can easily be determined with the equation $3m + 2(n - m) + 1$. When both numbers are 8, as in the above example, the result is 25.

Another common algorithm, this one used in image enhancement is a finite-impulse-response filter. The equation:

$$Y(n) = \sum_{i=0}^{N-1} a(i) I(n-i)$$

represents the output, $Y(n)$ in terms of the input, $I(n)$. It consists of both adds and shifts.

The objects being observed are generally well defined in contrast to the background, making it easy for the system to pull out the characteristics needed to recognize a pattern. When the data is received by the screening block, however, one of its key tasks is to replace the weak

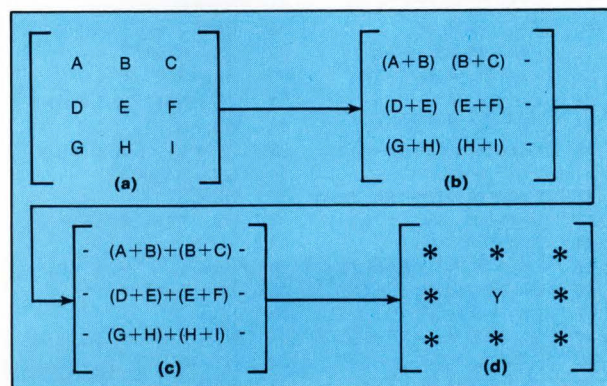
signals along the edges of the object with stronger signals.

A common technique used for edge enhancement calls for a Sobel filter, a two-dimensional finite-impulse-response filter with a thresholding algorithm. The Sobel filter takes an existing image and creates a new one comprising the magnitude and direction of all the strong edges of the object.

The filter works with neighborhood processing, determining the value of a pixel by examining those adjacent to it. With a 3-by-3-pixel grouping, consisting of pixels A through I,

**Program 1. Double vision:
Adding two 8-bit images**

Line	Code	Line	Code
1	NS:=RAM 0; C:=0	14	EW:=RAM 12
2	EW:=RAM 8	15	RAM 20:=SM; C:=CY
3	RAM 16:=SM; C:=CY	16	NS:=RAM 5
4	NS:=RAM 1	17	EW:=RAM 13
5	EW:=RAM 9	18	RAM 21:=SM; C:=CY
6	RAM 17:=SM; C:=CY	19	NS:=RAM 6
7	NS:=RAM 2	20	EW:=RAM 14
8	EW:=RAM 10	21	RAM 22:=SM; C:=CY
9	RAM 18:=SM; C:=CY	22	NS:=RAM 7
10	NS:=RAM 3	23	EW:=RAM 15
11	EW:=RAM 11	24	RAM 23:=SM; C:=CY
12	RAM 19:=SM; C:=CY	25	RAM 24:=C
13	NS:=RAM 4		



2. Edge enhancement using a Sobel filter furnishes a new value for pixel E by comparing it with those (A through D and F through I) that surround it (a). Pixel values are added together in parallel (b,c) to yield the value (d). All values are added in parallel.

Systolic array chip

Program 2. Sobel-filter to establish pixel value			
Line	Code	Line	Code
1	EW:=RAM 0; C:=0	54	NS:=RAM 25
2	EW:=E; NS:=RAM 8	55	NS:=S; C:=0
3	RAM 16:=SM; C:=CY	56	NS:=RAM 25; EW:=NS
4	EW:=RAM 1	57	NS:=N
5	EW:=E; NS:=RAM 9	58	RAM 35:=SM; C:=BW
6	RAM 17:=SM; C:=CY	59	NS:=RAM 26
7	EW:=RAM 2	60	NS:=S
8	EW:=E; NS:=RAM 10	61	NS:=RAM 26; EW:=NS
9	RAM 18:=SM; C:=CY	62	NS:=N
10	EW:=RAM 3	63	RAM 36:=SM; C:=BW
11	EW:=E; NS:=RAM 11	64	NS:=RAM 27
12	RAM 19:=SM; C:=CY	65	NS:=S
13	EW:=RAM 4	66	NS:=RAM 27; EW:=NS
14	EW:=E; NS:=RAM 12	67	NS:=N
15	RAM 20:=SM; C:=CY	68	RAM 37:=SM; C:=BW
16	EW:=RAM 5	69	NS:=RAM 28
17	EW:=E; NS:=RAM 13	70	NS:=S
18	RAM 21:=SM; C:=CY	71	NS:=RAM 28; EW:=NS
19	EW:=RAM 6	72	NS:=N
20	EW:=E; NS:=RAM 14	73	RAM 38:=SM; C:=BW
21	RAM 22:=SM; C:=CY	74	NS:=RAM 29
22	EW:=RAM 7	75	NS:=S
23	EW:=E; NS:=RAM 15	76	NS:=RAM 29; EW:=NS
24	RAM 23:=SM; C:=CY	77	NS:=N
25	RAM 24:=C	78	RAM 39:=SM; C:=BW
26	EW:=RAM 16; C:=0	79	NS:=RAM 30
27	EW:=W; NS:=RAM 16	80	NS:=S
28	RAM 25:=SM; C:=CY	81	NS:=RAM 30; EW:=NS
29	EW:=RAM 17	82	NS:=N
30	EW:=W; NS:=RAM 17	83	RAM 40:=SM; C:=BW
31	RAM 26:=SM; C:=CY	84	NS:=RAM 31
32	EW:=RAM 18	85	NS:=S
33	EW:=W; NS:=RAM 18	86	NS:=RAM 31; EW:=NS
34	RAM 27:=SM; C:=CY	87	NS:=N
35	EW:=RAM 19	88	RAM 41:=SM; C:=BW
36	EW:=W; NS:=RAM 19	89	NS:=RAM 32
37	RAM 28:=SM; C:=CY	90	NS:=S
38	EW:=RAM 20	91	NS:=RAM 32; EW:=NS
39	EW:=W; NS:=RAM 20	92	NS:=N
40	RAM 29:=SM; C:=CY	93	RAM 42:=SM; C:=BW
41	EW:=RAM 21	94	NS:=RAM 33
42	EW:=W; NS:=RAM 21	95	NS:=S
43	RAM 30:=SM; C:=CY	96	NS:=RAM 33; EW:=NS
44	EW:=RAM 22	97	NS:=N
45	EW:=W; NS:=RAM 22	98	RAM 43:=SM; C:=BW
46	RAM 31:=SM; C:=CY	99	NS:=RAM 34
47	EW:=RAM 23	100	NS:=S
48	EW:=W; NS:=RAM 23	101	NS:=RAM 34; EW:=NS
49	RAM 32:=SM; C:=CY	102	NS:=N
50	EW:=RAM 24	103	RAM 44:=SM; C:=BW
51	EW:=W; NS:=RAM 24	104	NS:=0;EW:=0
52	RAM 33:=SM; C:=CY	105	RAM 45:=SM
53	RAM 34:=C		

(Fig. 2) the equation that determines the Y axis values is

$$Y = (A + 2B + C) - (G + 2H + I)$$

$$= [(A + B) + (B + C)] - [(G + H) + (H + I)]$$

The X axis values are established by

$$X = (C + 2F + I) - (A + 2D + G)$$

$$= [(C + F) + (F + I)] - [(A + D) + (D + G)]$$

The code for processing the first equation (see Program 2) reveals the unusual aspects involved in programming the systolic array. The true key to the chip's speed lies in the simultaneous computations it carries out. The first 25 instructions add each pixel to its neighbor to the west to form a new image.

Likewise, instructions 26 through 53 add this new image to the eastern neighbors, forming a second image. Instructions 54 to 105 add each pixel in that new image to its neighbor to the north and finally add each pixel in this third image to its southern neighbor. The resulting data, which is determined for every pixel in the image, can have as many as 10 bits, as well as a + or - sign. The latter denotes whether the edge gradient is changing from black to white or white to black. The fact that each of these values is computed in parallel results in fast throughput, since the value for the middle row is shifted upward, where it becomes the bottom row of the 3-by-3-pixel grid being processed in an adjacent processor element. The value also is shifted downward to the adjacent processor element, where it becomes the top row for the grid being processed there—a 3-by-3-pixel group centered around H.

The following Sobel operations are performed within individual cells of the array. First, a reasonable approximation of the magnitude of the gradient vector is computed by adding the absolute values of X and Y. To obtain that result, the sign bit plane for X determines whether to invert it and add one to it to form the absolute value. Processing the absolute value of a number takes $3m + 8$ instructions, where m equals the number of bits.

Next, the direction of the gradient to the nearest 45° line is determined. This must be done so that data can be processed by the extractor block and is accomplished by using the signs of both X and Y to determine which quad-

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Systolic array chip

rant contains the gradient. Once the direction is established, another process, consisting of $18m + 76$ instructions, is performed to bring the vector in line with the nearest 45° angle.

In thresholding, the final step, the value is compared with a predetermined constant. The result of this operation is used to pass or reject the direction vector, a step necessary to ascertain that it is valid data and not simply noise. If the vector information is below the threshold, the resulting word consists of 8 zeros. If it is valid, the location of a single 1 in the 8-bit word will denote which of eight directions the vector lies closest to. Thresholding requires $m + 13$ instructions, with another 18 instructions needed to properly place the 1 in valid words.

The last word

The resultant word is then passed to the extractor. At this point, a spoke filter is called into play. It is used to detect objects of various shapes and to extract length, width, and other data from the image. For example, the filter can be used to determine how many of the radial spokes along eight axes have Sobel gradients that point to or away from a specific pixel. The expected size and shape of the object determines the lengths of the spoke's arms, which can range from a single pixel to very large pixel blocks.

The final block in a pattern recognition system handles the task of deciding. This is typically carried out by a group of microprocessors or bit-slice processors that receive, store, and then manipulate the object characteristics that have been extracted in the preceding series of operations. These manipulations generally involve projecting a feature into a previously determined and segmented space to determine what type of object makes up the image. Although systolic arrays can perform this chore, it will probably remain the realm of standard processors. Algorithms are in plentiful supply that make good use of standard von Neumann architectures, which are well suited to the task.

However, one of the most challenging aspects of implementing the decider hardware is linking it with the high-speed front end hardware. Often, this means adding several microcomputers, hence demonstrating the inherent networking inefficiencies of these architectures.

The best configuration for transmitting data from the systolic array blocks is to use a so-called corner-turning block, a small group of systolic arrays that reformats data for the microprocessor. The systolic array normally sends out data in bit planes instead of the 8- or 16-bit words microprocessors work with so readily. The corner-turning block formats the bit planes into the gray scale values that make up a pixel. At the same time, the arrays can postprocess the pixels before passing the final decider data on to the microcomputer network.

Flexibility is the key

Each of the four tasks—improving, screening, extracting, and deciding—can be handled easily by systems built around the systolic array chip. The IC can be incorporated into a number of setups, ranging from those that recognize moving objects, through those that work with an assembly line robot, to those that recognize characters. Indeed, the chip's flexibility can be quickly grasped by these examples. Although all use roughly the same overall system architecture, the array can be programmed to meet the various algorithmic and speed demands called for by particular tasks. Thus a generic system can work in a variety of applications, giving it the flexibility associated with traditional microprocessors (Fig. 3).

The system itself is centered on the main block of chips, but it also employs the array to take care of reformatting. These blocks will typically be used to format data for input as well as for output.

On automatic pilot

One example of this generic approach is an automatic inspection system that scans parts as they move along a production line. The system's data rate runs from 8 to 16 million words/s, with real-time response required. Improving and screening would require 1 or 2 algorithms; the extractor would execute from 10 to 20 algorithms. The decider would perform 1 to 3 algorithms using the resultant data.

The major design tradeoff that must be considered when building this or any other generic system is deciding how many processor elements are needed and how they should be arranged. That, in turn, hinges on the throughput

THE TRIPLETT

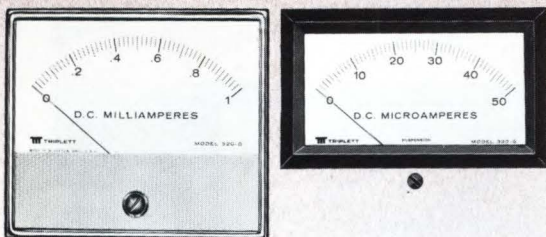
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Systolic array chip

rate and the number of instructions that must be performed.

For automatic inspection, as many as 3300 instructions might be performed on each frame of data. Using a 10-MHz chip, these can be processed in 330 μ s. Since a standard 30-Hz frame is sent only every 33 ms, the chip would be operating only 1% of the time if an individual processor element were dedicated to each of the 512 by 512 pixels. It is thus possible to trim costs by building a smaller block of systolic array chips and passing the data through the block several times.

On the tube

To process 3300 instructions, the block would require roughly 2623 processor elements, or about 37 chips. Since data comes from the sensor in the standard TV-line format, the most natural way to arrange the chips, which are themselves laid out as 6 by 12 processor elements, is to work with a grid of 6 by 516 elements. Thus the system could handle six incoming rows of data at once because the array's

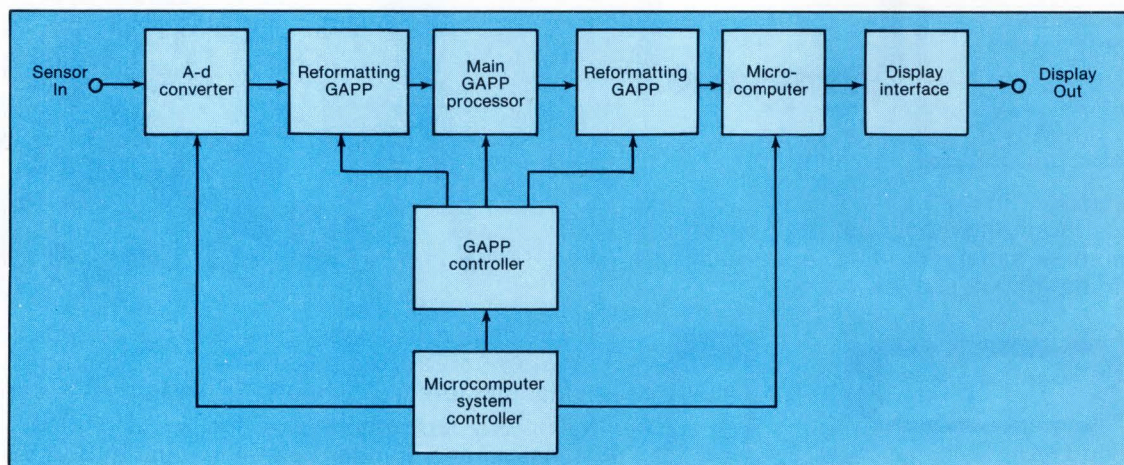
communication registers, which move data in and out, could easily handle the 512 useful samples of data coming from a 10-MHz TV camera.

However, if the spokes employed in feature extraction are 10 pixels long, the span of the spoke wheel is 20 pixels vertically. With only six cells aligned vertically, that causes severe complications in implementing the spoke algorithm.

Three solutions

There are three ways out of this problem. The simplest is to add two or three more rows of chips so the block is 18 to 24 elements deep. There will be some overlap problems, but the added processing power makes them fairly easy to solve.

Alternatively, two frame buffers could be added before the input reformatting block. That lets the system send rectangular arrays of data into the main block of chips. Overlap problems would be less severe, but this solution drives cost up since more hardware is used. The



3. A generic system based on the systolic array chip can be used in many applications. Systolic arrays are not only the main system building block, but are employed to reformat data going into and coming out of the main array. The last performs the processing needed to determine the characteristics of the object under scrutiny.

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CIRCLE 130

DESIGN ENTRY

Systolic array chip

tradeoff between the two solutions comes down to the cost and time needed to design in the requisite buffers, on the one hand, and the added software needed to process the spoke-filter algorithm when only six rows of cells are used, on the other.

The third time's the charm

The ultimate solution goes with the 6-by-516-cell layout, but stores three or four sets of six video lines in the cells using each element's 128 bits of RAM. Four sets of six rows would occupy only 32 RAM locations when 8-bit words are used. If this scheme leaves enough RAM to perform the necessary computations, it is an attractive solution, since 24 video lines can be processed simultaneously with a single row of chips.

Other systems can be configured using the same basic approach. Varying data input rates and the type of data being processed, though, will force minor changes in the actual arrangement of the blocks. One variation on the basic system enables it to be put to work enhancing images in computer-aided tomography. Improving the quality of the images from a CAT scanner has the obvious advantage of giving the physician a better chance to locate and identify abnormalities.

Since input from the scanner comes in large blocks of data—every few minutes or seconds—the system also requires an input buffer. It must have a high-speed input port, although it can send data to the block of arrays at a slower rate.

The variety of algorithms needed for the many chores of a physician mandate a fairly large memory buffer for the controller. The main block of processor elements should be rectangular; the total number of cells will again depend on the algorithmic load and the frequency of input. It might also be a good idea for the system to have an interactive interface so that the doctor can refine the image while it is being viewed. □

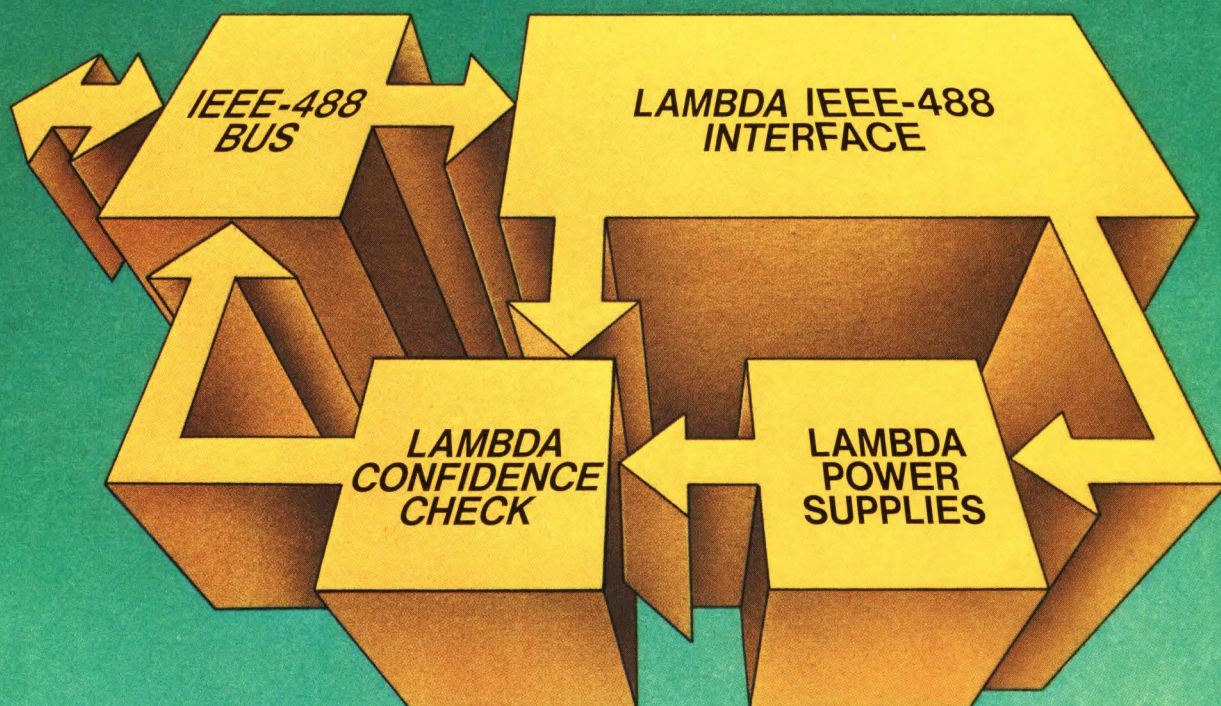
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Within the next year
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Circle

556
557
558

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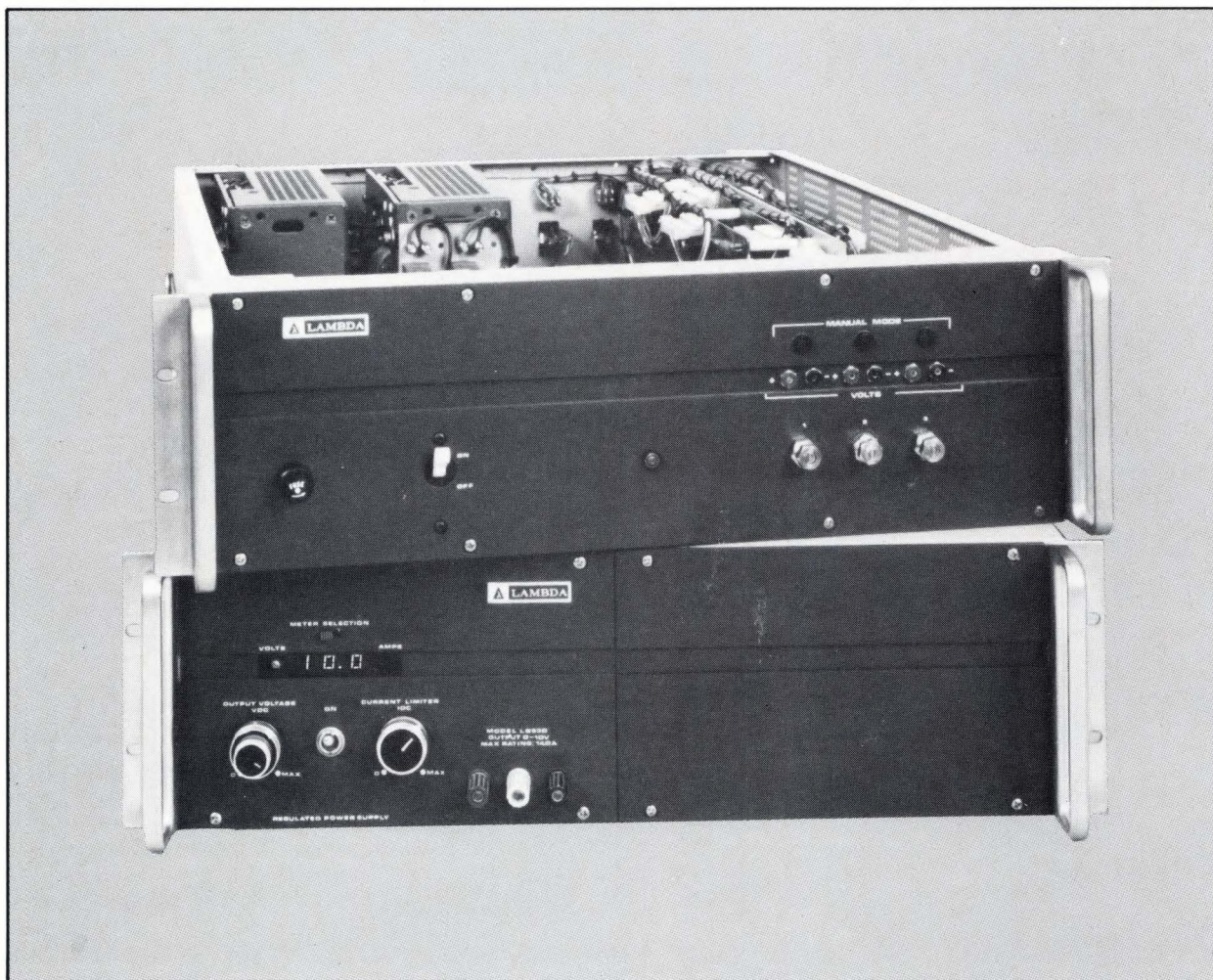
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Confidence check—verifies the program requested.

One primary address controls 6 secondary addresses.

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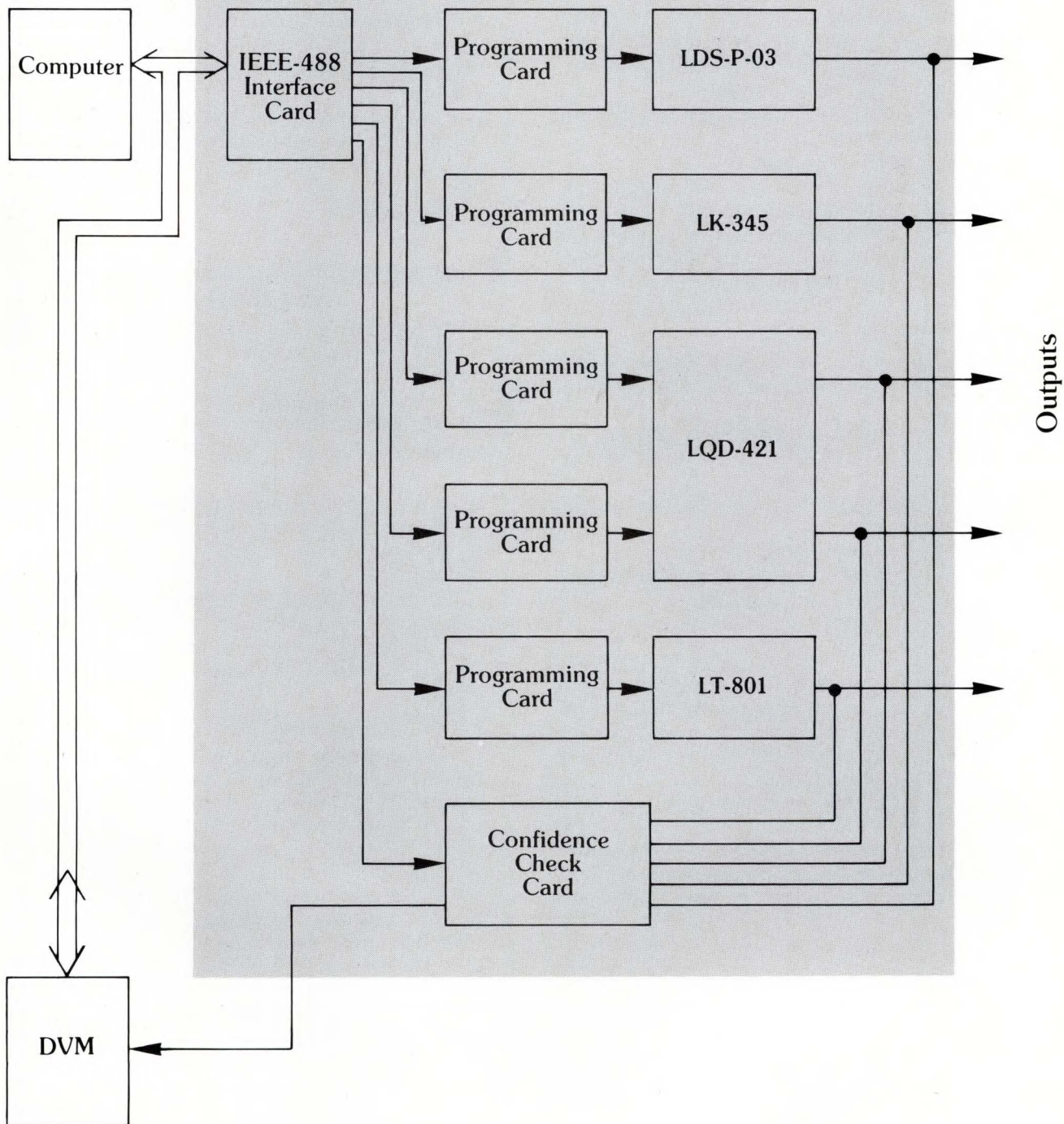


Figure 1

SYSTEM DESCRIPTION AND PROGRAMMING

The Lambda IEEE-488 Power Supply System provides communication between an end user's control system (computer) and standard Lambda Power Supplies. The bus protocol and timing relationships are as defined by the IEEE-488 Standard.

SYSTEM DESCRIPTION

The system is a modular design that permits maximum user flexibility in tailoring a system to your specific needs and costs. System elements include:

- *Lambda standard power supplies
- *Lambda standard rack adapter and the following printed circuit cards:

- a. IEEE-488 interface card
- b. programming card(s)—one per power supply
- c. confidence check card (optional)

The IEEE-488 Power System includes all interconnection wiring and comes completely assembled, tested and guaranteed by Lambda. A system block diagram is shown in figure 1.

The Lambda system features:

1. Standard-pick the system to suit your needs from off-the-shelf modules with a wide range of options.
2. Controls Lambda standard power supplies.
3. Confidence check—verifies the program requested.
4. One primary address controls 6 secondary addresses.
5. Simplicity in programming.
6. Manual/Auto mode select switch—for ease of maintenance and system set up.

A. IEEE-488 Interface Card

The IEEE-488 Interface Card is a dedicated microprocessor which performs the tasks of bus communication, instruction decode and secondary address selection. Instructions and data are formulated in accordance with the 1978 IEEE-488 Standard. One interface card is required for each primary address and controls both programmer and confidence check cards (described in sections B and C) up to a maximum of 6 secondary addresses. Secondary addresses are determined by connections from the interface card to the programming card.

B. Programming Card

The programming card converts the decoded ASCII instructions into power supply control voltages for voltage output or current limit setting. It also provides the isolation between the bus and the power supply.

A power supply programmed voltage range may be selected from a minimum of zero volts to the maximum rated output of the power supply, up to a maximum of 100 volts. (Minimum voltage interval in the 0 to 100 volts full range is .0244 volts or 100 volts 12 bit DAC.)

4095 bits

The divider network and associated circuitry to accomplish this are factory-installed and calibrated. All offsets and tolerances in the programmer, as well as the individual power supplies, are compensated for.

UNIVERSAL PROGRAMMING IN VOLTAGE AND CURRENT

Power supplies are voltage programmed using four decimal digits, resulting in a resolution to better than 0.1%. Zero volts is represented as 0000 and V_{OUT} maximum as 9999. Any intermediate value of voltage is determined by the relationship:

$$\text{Voltage Scale Factor} = 9999 \times \frac{V_{\text{desired}}}{V_0 \text{ max}}$$

For current limit programming the range is 00 to 99. 00 represents the minimum value of current. 99 represents power supply full load current limit setting. Any value between 00 to 99 represents a percentage of full scale current limit with a relationship similar to that of the voltage scale factor.

Lambda power supplies used in this application are trimmed at the factory requiring no user action.

C. Confidence Check Card

A confidence check card can be configured within the system to verify that the programmed supply outputs are equal to the programmed values. (This requirement is termed "Confidence Check.") The confidence check card occupies one secondary address and is capable of routing output voltage and/or current by means of relays of up to five supplies to a user furnished digital voltmeter. Either output voltage or load current may be measured. By using an IEEE-488 compatible meter the user is capable of machine reading the outputs. The outputs are isolated from the meter until the confidence test check is invoked.

★ UNL

Unlistens Interface Card

All secondary addresses of a primary address may be programmed successively by deleting the UNL unlisten command. After transmittal of the E command the programmer transmits a new secondary address and repeats the new data followed by an E command (end of string command). Upon completion of all programming to the primary address a UNL, unlisten command, is given and the IEEE-488 adapter card is again in a monitoring state.

Note: A missing or incorrect termination character or improper format inhibits confidence check.

TYPICAL EXAMPLE OF A PROGRAMMING FORMAT

1 System listen address

switch address

2 Secondary address

50 Refers to Power Supply

(Letter P in ASCII)

37 7 in ASCII	} Programmed voltage in %. Unit programmed to 75% of V_o max.
35 5 in ASCII	
30 0 in ASCII	
30 0 in ASCII	

39 9 in ASCII	} Programmed current in %. Unit programmed to 99% to I_o max.
39 9 in ASCII	

45 End of String Command

(Letter E in ASCII)

The above sequence will program the power supply at secondary address 2, to 75% of V_o max and 99% of I_o max value. To measure programmed output, the following sequence of commands will initiate confidence check system to measure the output. Assume that primary address is still active.

06—Secondary address for confidence check.
(Binary Format)

43—Refers to confidence check system.
(Letter C in ASCII)

56—Measuring parameter-voltage.
(Letter V in ASCII)

02—Power Supply to be monitored.
(Binary Format)

45—End of String Command.
(Letter E in ASCII)

UNL

Unlisten command.

COMMAND STRING TO CLEAR ONE SECONDARY ADDRESS

★ My Listen Address

1-30 selected address (Binary Format)

★ My Secondary Address

Assigned secondary address (Binary Format)

★ Selected Device Clear

- This command to a power supply sets voltage and current limit to minimum value.
- This command to a confidence check circuit opens all relays disconnecting the monitored power supply and monitoring meter from the confidence check card.

★ Unlisten

TERMINATION OF AN ERRONEOUS COMMAND STRING

Inserting any character not recognized by the adapter, e.g. (Q or Z) etc. will terminate and abort a command string.

Reset of all functions is automatic at power up or upon receiving the bus command of "DEVICE CLEAR". Manual reset, although provided, is not required for this operation.

ASSEMBLY SPECIFICATION

The IEEE-488 Power Supply System unit is available only as a completed assembly.

SYSTEM SPECIFICATIONS

Number of Outputs

- 6 outputs total
- 6 independent voltage sources
- 5 independent voltage sources plus one confidence check.

SUPPLIES

Most standard Lambda Power Supplies

SYSTEM PERFORMANCE

Voltage Range and Output from zero to the published V_{OUT} maximum of the power supply up to a maximum V_{OUT} of 100 volts.

VOLTAGE REGULATOR MODE

Line Regulation/Load Regulation

Individual power supply specifications apply.

Ripple

RMS—Individual power supply specifications plus 1mV RMS for linear power supplies.

Peak to peak—individual power supply specifications + 3mV peak to peak for linear power supplies.

PRIMARY AND SECONDARY ADDRESSING

The IEEE-488 interface can only handle 15 instruments. To expand the system capabilities, secondary addresses are used. The Lambda IEEE-488 Power Supply Interface can handle up to six secondary addresses for each primary address. This gives the system designer flexibility in matching his needs in terms of cost and performance at each primary address. A confidence check card provides efficient usage of primary addressing. One confidence check card may be used for each primary address.

OPERATING THE GPIB ASSEMBLY

The Lambda IEEE-488 Power Supply Assembly is provided as a completed system as specified by the user. The user is required to apply input power, connect the IEEE-488 interface cable, set the primary address switch, and connect the load circuits to the proper power sources. The Lambda IEEE-488 Power Supply Assembly conforms to the 1978 IEEE-488 specifications. The system conforms to the extended listener configuration subgroup #2 (LE2).

Bus Connector

The assembly is equipped with a standard IEEE-488 receptacle located on the rear panel. The controller/computer IEEE-488 mating package is simply connected to this receptacle.

Primary Address Selection

A five bit switch is part of the rear panel assembly, and its address must be selected by the user. The adapter will respond to commands bearing this address. Addresses may be selected from 0-30. The selected address is recognized at power up.

Secondary Address

These addresses are assigned to each power supply at time of assembly either on recommendation by the user or by Lambda.

COMMAND SEQUENCE TO ADJUST POWER SUPPLY VOLTAGE OR CURRENT

Definition of Terms

MLA

My listen address—switch selected primary address.

MSA

Secondary address numbers 1-6.

P

Represents power supply.

C

Represents confidence check.

V₁, V₂, V₃, V₄

Represents percent of full scale voltage.

These numbers are transmitted in ASCII format. 99.99% is controller transmitted as 39,39,39,39.

I₁, I₂

Represents percent of full scale current I₁, I₂% of full scale. These numbers are also transmitted in ASCII format; 50% is transmitted as 35,30.

E

Represents end of string command. Please note a wrong terminator or an incorrect number of the data string digits will result in no change of assigned power supply output.

UNL

Represents GPIB unlisten command.

VOLTAGE OR CURRENT PROGRAMMING

This is best explained with the following example. An asterisk refers to the GPIB implementation of the noted mnemonic Programming Format for Power Supply.

★ My Listen Address:

1-30 selected primary address (Binary Format)

★ My Secondary Address:

1-6 power supply address (Binary Format)

P Represents Power Supply

V₁ = 37

V₂ = 35

V₃ = 30

V₄ = 30

} Assume power supply is programmed to 75.00% full scale voltage

I₁ = 39

I₂ = 39

} Assume power supply is programmed for full scale current

E = End of String Command (Letter E in ASCII)

★ UNL: Unlistens Interface Card

CONFIDENCE CHECK PROGRAMMING

The confidence check programming is similar in format to power supply programming. An external meter must be connected to the Confidence Check Output to measure the selected power supply output voltage or current as required. Please note this meter should possess IEEE-488 listener and talker capability and have its own primary address of outputs to be computer interpreted.

★ My Listen Address

1-30 selected address (Binary Format)

★ My Secondary Address

Assigned address in Binary Format (generally 6)

C represents confidence check

V = voltage measurement

I = current measurement

Secondary Address of power supply to be monitored (1-5)

E = End of String Command

Accuracy of Programming

0.1% of full scale

Resolution of Programming

0.1% of full scale

Temperature Coefficient

TC of Supply + .01%/°C

Overshoot

0.25 Volt maximum at turn on/turn off/recovery from short circuit.

Programming Range

00.00% to 99.99% of V_{OUT}

Programming Time

Voltage up programming 50 milliseconds typical.

Remote Sensing of Power Supplies

Provisions are made for remote sensing of power supplies. For connections, see instruction manual of individual power supply.

CURRENT REGULATOR MODE**Line Regulation/Load Regulation**

Power supply specifications apply.

Accuracy

2% of programmed value plus 1% of full scale.

Resolution

1% of rated current.

INPUT DATA FORMAT

Communication is conducted in accordance with IEEE-488/1978 standards. All data is transmitted in ASCII format.

The system is capable of a listen only function.

It uses secondary addressing extensively.

Voltage Programming format. See page 5.

Input connector is wired per IEEE-488 specifications. All communication, control and data entry through this connector.

The following control signals are recognized: ATN, IFC, NRFD, NDAC and DAV. REN is not recognized.

Protection

In addition to all protection circuits inherent to each power supply, protection circuits are added which limit each output voltage to less than 5V in case of programmer failure.

Power On Operation

All outputs are set to zero volts. No overshoot at power on, power off or power failure.

AC Input

105-132 VAC 50/60 Hz

187-242 VAC 50/60 Hz available as an option.

205-265 VAC 50/60 Hz available as an option.

Operating Temperature Range

0-60°C

Storage Temperature Range

-55°C to +85°C

CONFIDENCE CHECK SYSTEM

1. Number of power supplies that may be monitored. (5)

2. Number of power supplies that may be monitored at one time. (1)

3. Power Supply-Output functions that may be monitored at one time. (1)—either output voltage or a measure of output current.

4. Location of voltage and current measurements.
a. Output voltage of power supply at terminals of assembly.

b. Output current is taken across internal shunt.

5. Accuracy of output voltage measurement.

Measurement meter accuracy plus effect of 50,000 ohm source impedance on meter accuracy.

6. Accuracy of current measurement.

1% plus accuracy of meter plus effect of 50,000 ohm source impedance on meter accuracy.

7. Switching Relay voltage insulation.

a. Voltage rating between contacts = 200 volts.

b. Voltage rating contact to coil = 1,000 volts.

Power On Operation

All relay contacts open.

AC Input

Same as IEEE-488 adapter card and programmer card.

Operating Temperature Range

0-60°C

Storage Temperature Range

-55°C to 85°C

Protection

All relay contacts buffered with 25,000 ohms.

MECHANICAL CONFIGURATION

Two basic configurations are available with modular power supplies.

a. blank front panel with on/off switch, pilot light and fuse.

b. same as above with front panel voltage adjust pots and test points.

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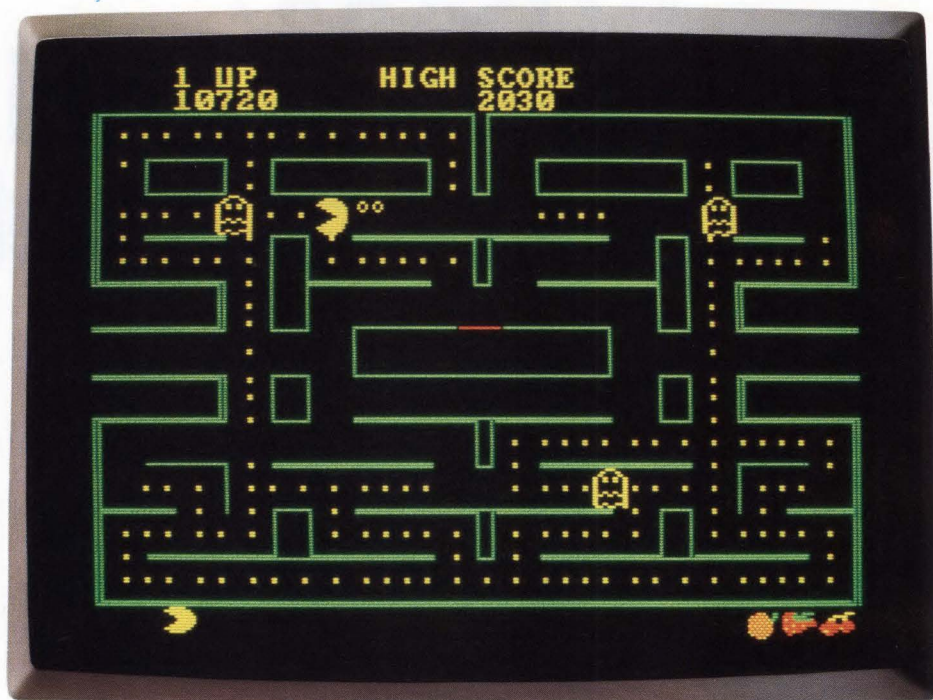
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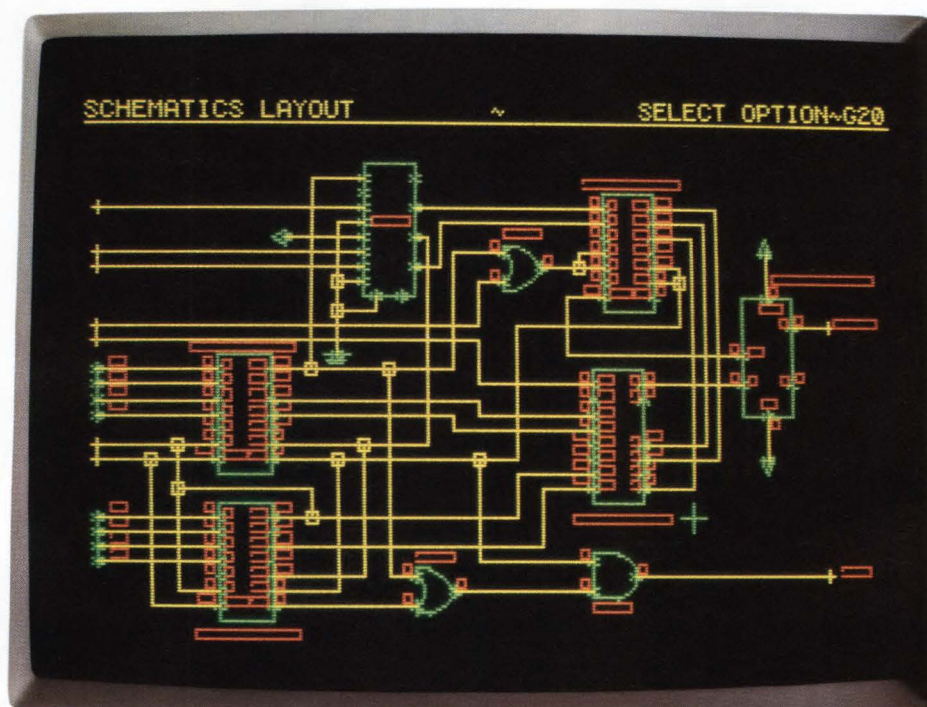
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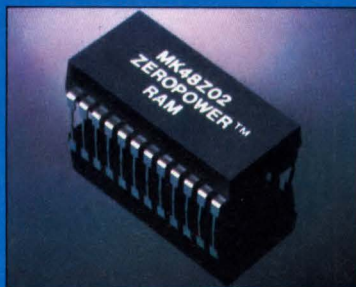
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DESIGN SOLUTIONS

Single control adjusts variable oscillator over four-decade range

Andrew M. Siegel

Tufts University
Medford, Mass. 02155

The frequency of a variable duty-cycle oscillator is adjustable over a span of greater than four decades without the need for a range switch. Instead, a single low-resistance potentiometer covers the entire range linearly. Further, it can be remotely mounted without shielded cable or the fear of picking up noise.

Basically, the circuit consists of a variable current source that charges a capacitor, which is rapidly discharged by a Schmitt-trigger comparator (see the figure). The sawtooth waveform thus produced is fed to another comparator, one with a variable switching level. The output from the second comparator is a pulse train with an independently adjustable frequency and duty cycle.

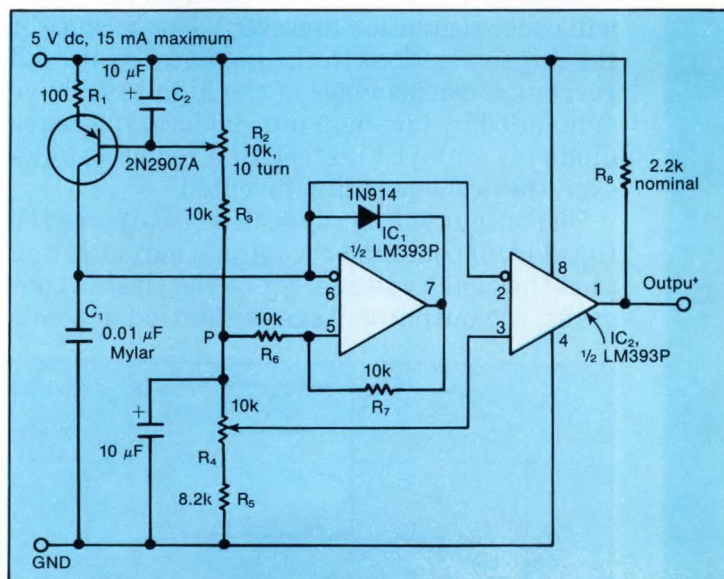
The variable-frequency ramp generator consists of capacitor C_1 , which is charged by a variable and nonlinear current source. The latter comprises a 2N2907A pnp transistor, plus resistor R_1 and potentiometer R_2 . Capacitor C_2 eliminates any ripple or noise at the base of the transistor that might cause frequency jitter at the output.

When the voltage on C_1 reaches the upper threshold of Schmitt trigger IC_1 , as set by resistors R_6 and R_7 and the voltage at point P, the chip's output saturates to ground potential and drains the charge from C_1 through a forward-biased 1N914 blocking diode. When the voltage falls below the lower threshold, IC_1 's output floats, reverse-biasing the diode and allowing C_1 to charge once again.

The duty cycle of the sawtooth waveform is

controlled by comparator IC_2 and adjusted by potentiometer R_4 . The potentiometer varies the switching level of IC_2 over the entire voltage range of the waveform. Since the switching level depends solely on voltage, the duty-cycle setting will not affect the output frequency.

The output frequency is somewhat temperature sensitive. However, short-term stability should be adequate for many testing purposes.



Just one potentiometer adjusts the frequency of a variable duty-cycle oscillator over a four-decade range. Because a low-resistance potentiometer is used, it can be remotely mounted without fear of noise.

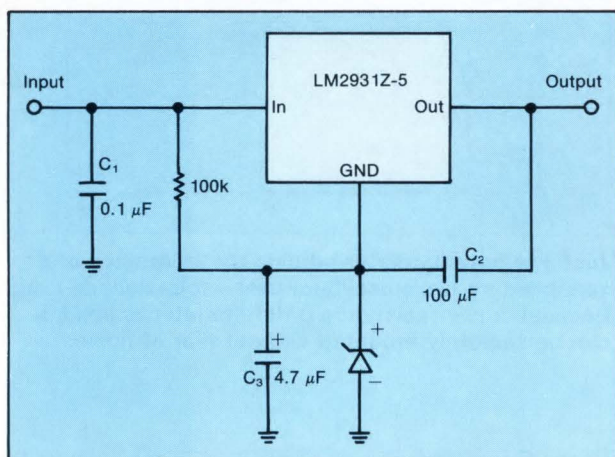
Zener diode increases a fixed pnp regulator's output voltage ratings

Fred Cheng

Senior Design Engineer
National Semiconductor Corp.
M/S C2500, 2900 Semiconductor Drive
Santa Clara, Calif. 95051

Increasing the output voltage of a three-terminal regulator that uses an internal pnp pass element is not simply a matter of tying a resistor in series with the ground pin. Doing so will cause regulation to be very poor because of the large variations in the regulator's internal current, a consequence of the high base drive demanded by low-beta pnp devices. If a zener diode is employed instead of a resistor, however, the problem is circumvented.

The output voltage of such a circuit (see the figure) will equal the regulator's output rating plus the zener voltage. Since the first is constant, the output voltage regulation depends



A zener diode in the ground lead of a fixed pnp regulator varies the voltage output of that device without a significant sacrifice in regulation. The technique also allows the regulator to operate with output voltages beyond its rated limit.

mainly on the zener voltage and the diode's dynamic impedance.

The diode's voltage varies only slightly with current flowing through it. When the regulator's load changes from 50 to 150 mA, for instance, the zener current increases by 12.5 mA and its voltage varies by just a few hundred millivolts—far less than the change of several volts that would result if a resistor were used.

The maximum input voltage of the regulator, with respect to its ground pin, is limited by the breakdown rating of its internal circuitry. With the zener in place, though, the highest permissible input is the sum of the zener voltage and the breakdown rating.

The 5-V regulator shown has a maximum operating input voltage of 26 V. With a 51-V zener diode, the device can be converted into a 56-V regulator with a maximum input voltage rating of 77 V. Further, the pnp regulator's low voltage drop allows the input to be as low as 56.6 V with load currents of 150 mA or less.

A word of caution: The circuit is not meant as a cure-all for all regulator problems. The device's inherent short-circuit protection may or may not be available, depending on the output voltage and the output pass transistor's safe operating area.

Although capacitors C_1 and C_2 have the values specified for normal operation, their maximum operating voltage ratings should exceed the input voltage. The value of capacitor C_3 will vary for different types of zener diodes, since the impedance of those devices, as well as their noise characteristics, will not be the same. The capacitor's value must be found by trial and error; however, it will generally fall between 0.1 and 5 μ F. Regardless of the value, the capacitor should be located as close as possible to the ground pin to ensure good decoupling and stable operation.

Radial-Lead Precision Film Resistors from Caddock combine high values and tight tolerances with a choice of two high-power densities or three low TCs.

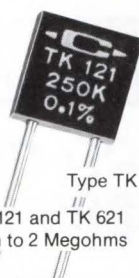


Type MK Radial-Lead Precision Power Film Resistors

MK 132 and MK 632
10 ohms to 100 Megohms

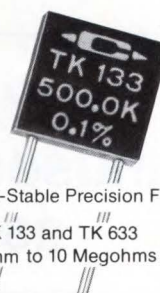


MK 120 and MK 620
30 ohms to 40 Megohms

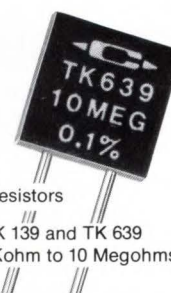


Type TK Temp-Stable Precision Film Resistors

TK 121 and TK 621
1 Kohm to 2 Megohms



TK 133 and TK 633
1 Kohm to 10 Megohms

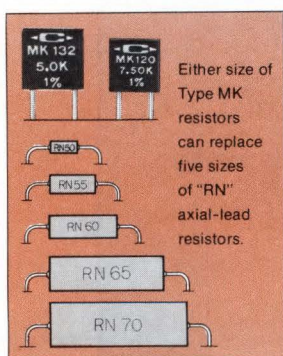


TK 139 and TK 639
1 Kohm to 10 Megohms

Type MK Radial-Lead Precision Power Film Resistors utilize Caddock's Micronox® resistance films to achieve high power density and an extended range of resistance values:

Available in two rectangular radial-lead packages that include values as high as 100 Megohms, these high-density film resistors permit electronic circuit designers to optimize packaging and PC board layouts with resistors that meet all these specifications:

	MK 120	MK 620	MK 132	MK 632
• Resistance Range	30 ohms to 2 Megohms	2.1 Megohms to 40 Megohms	10 ohms to 5 Megohms	5.1 Megohms to 100 Megohms
• Resistance Tolerance	±1.0% is standard, to ±0.1% on special order, depending on value and model.			
• Wattage	0.5 Watt	—	0.75 Watt	—
• Voltage	200 V	200 V	400 V	400 V
• Temperature Coefficient	50 PPM/°C	80 PPM/°C	50 PPM/°C	80 PPM/°C
	Temp Range: -15°C to +105°C, ref. +25°C.			
• Package Size	.250" square, .100" thick		.300" square, .100" thick	

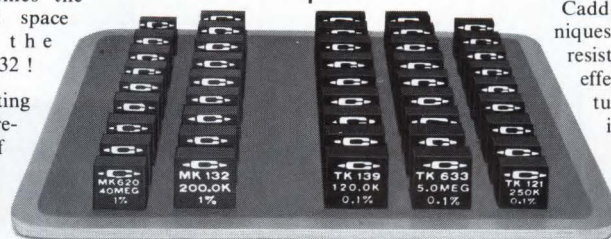


Either size of Type MK resistors can replace five sizes of "RN" axial-lead resistors.

These full-size photos comparing the Type MK resistors to "RN" style axial-lead resistors show that the largest Type MK, which is rated at 3/4 watt, requires less board space than the 1/20 watt "RN 50".

And within their voltage ratings, both sizes of Type MK resistors can replace five sizes of "RN" resistors, including the 1/2 watt "RN 70" which requires 10 times the board space of the MK 132!

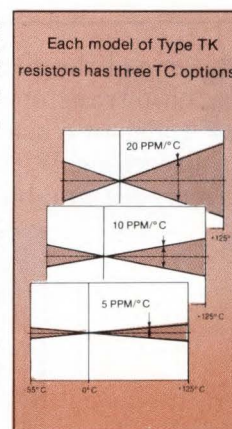
This combination of higher power rating and smaller size can also lower procurement costs by replacing many sizes of axial-lead resistors with Type MK resistors that have a 'standard' size and mounting dimensions.



Type TK Temp-Stable Precision Film Resistors with Caddock's Tetrinox® resistance films combine a choice of TCs of 5, 10 or 20 PPM/°C, a wide resistance range and tight tolerances.

Type TK Temp-Stable Precision Film Resistors provide a combination of performance advantages that are unique in a miniature resistive component:

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- **Resistance Range:** 1 Kohm to 10 Megohms.
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CIRCLE 115

Electronic Design • November 29, 1984 283

PAL circuit puts unused op codes to work as 8085 interrupts

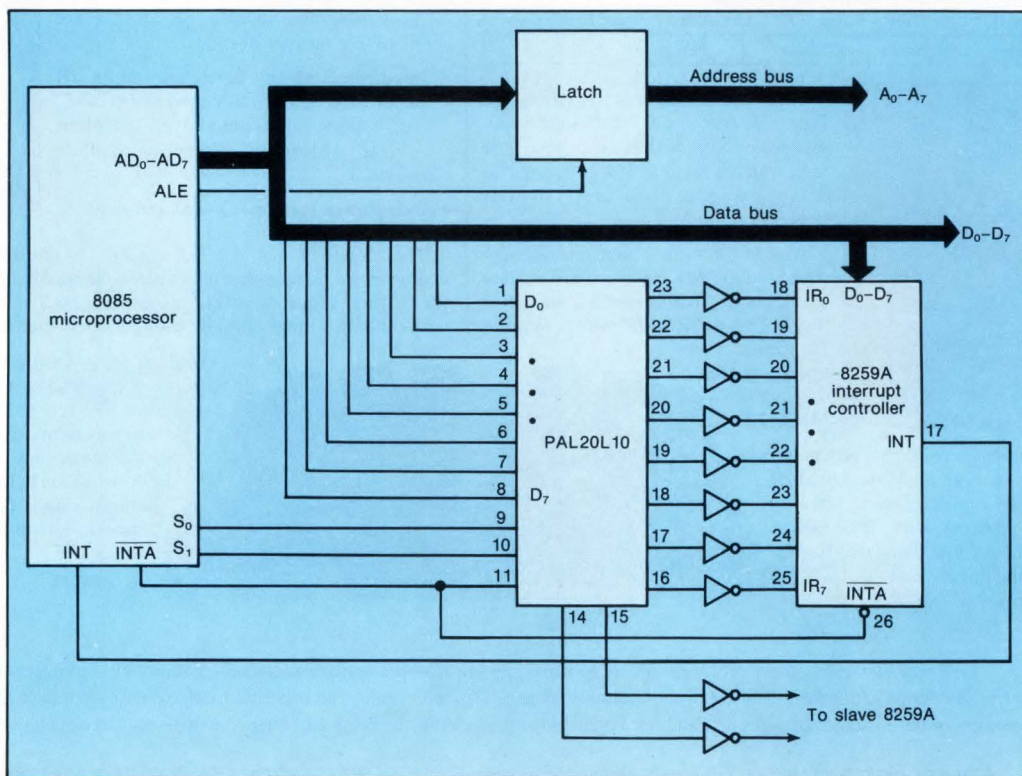
Vittal Rao
Engineer
ISRO Satellite Centre
Digital Systems Section
Airport Road, Vimanapura PO
Bangalore: 17
India

Some of the circuitry contained in a PAL chip transforms 10 otherwise invalid op codes into useful interrupts for an 8085 microprocessor. With a helping hand from the 8085's programmable interrupt controller, the

8259A, each of the op codes can be assigned to a unique vector in memory.

Of the 256 possible 8-bit op codes, 246 are recognized by the microprocessor. The remaining 10 elicit no response from the processor. They are (in hexadecimal notation): 08, 10, 18, 28, 38, CB, D9, DD, ED, and FD. The PAL device, however, decodes the data bus to detect any of the unrecognized op codes (see the figure).

When the processor fetches an op code from memory, its data bus status pins, S_0 and S_1 , plus the Interrupt Acknowledge ($\overline{INTA}$) line will be high. When $\overline{INTA}$ goes low, the invalid op code's



Op codes that would otherwise go unused are detected by a specially programmed PAL circuit. The chip drives a programmable interrupt controller, making 10 additional interrupts available to an 8085 microprocessor.

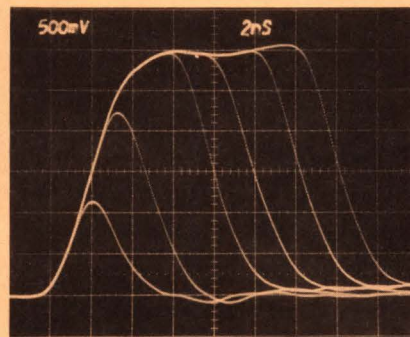
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DESIGN SOLUTIONS

vector is placed on the data bus by the interrupt controller and the microprocessor branches to that address. Thus interrupts can be generated under software control and then assigned a specific job or function within the system.

Programming equations for op-code detector built with a PAL chip

D0 D1 D2 D3 D4 D5 D6 D7 S0 S1 /INTA GND
NC /IR9 /IR8 /IR7 /IR6 /IR5 /IR4 /IR3 /IR2 /IR1 /IR0 VCC

/IR9 = D0•D1•D2•D3•D4•D5•D6•D7•S0•S1•/INTA.
/IR8 = D0•D1•D2•D3•D4•D5•D6•D7•S0•S1•/INTA.
/IR7 = D0•D1•D2•D3•D4•D5•D6•D7•S0•S1•/INTA.
/IR6 = D0•D1•D2•D3•D4•D5•D6•D7•S0•S1•/INTA.
/IR5 = D0•D1•D2•D3•D4•D5•D6•D7•S0•S1•/INTA.
/IR4 = D0•D1•D2•D3•D4•D5•D6•D7•S0•S1•/INTA.
/IR3 = D0•D1•D2•D3•D4•D5•D6•D7•S0•S1•/INTA.
/IR2 = D0•D1•D2•D3•D4•D5•D6•D7•S0•S1•/INTA.
/IR1 = D0•D1•D2•D3•D4•D5•D6•D7•S0•S1•/INTA.
/IR0 = D0•D1•D2•D3•D4•D5•D6•D7•S0•S1•/INTA.

A single 8259A is capable of handling eight interrupts. To handle the full complement of 10, a slave controller must be added. A set of logic programming equations tailors the PAL device to its task (see the listing).

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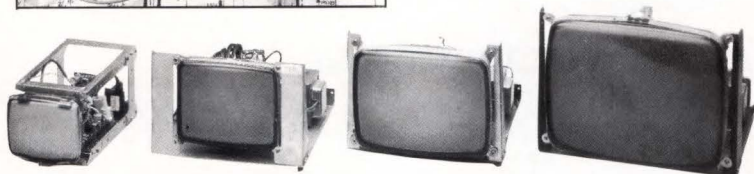
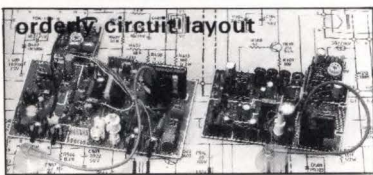
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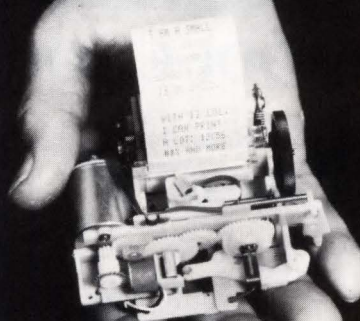
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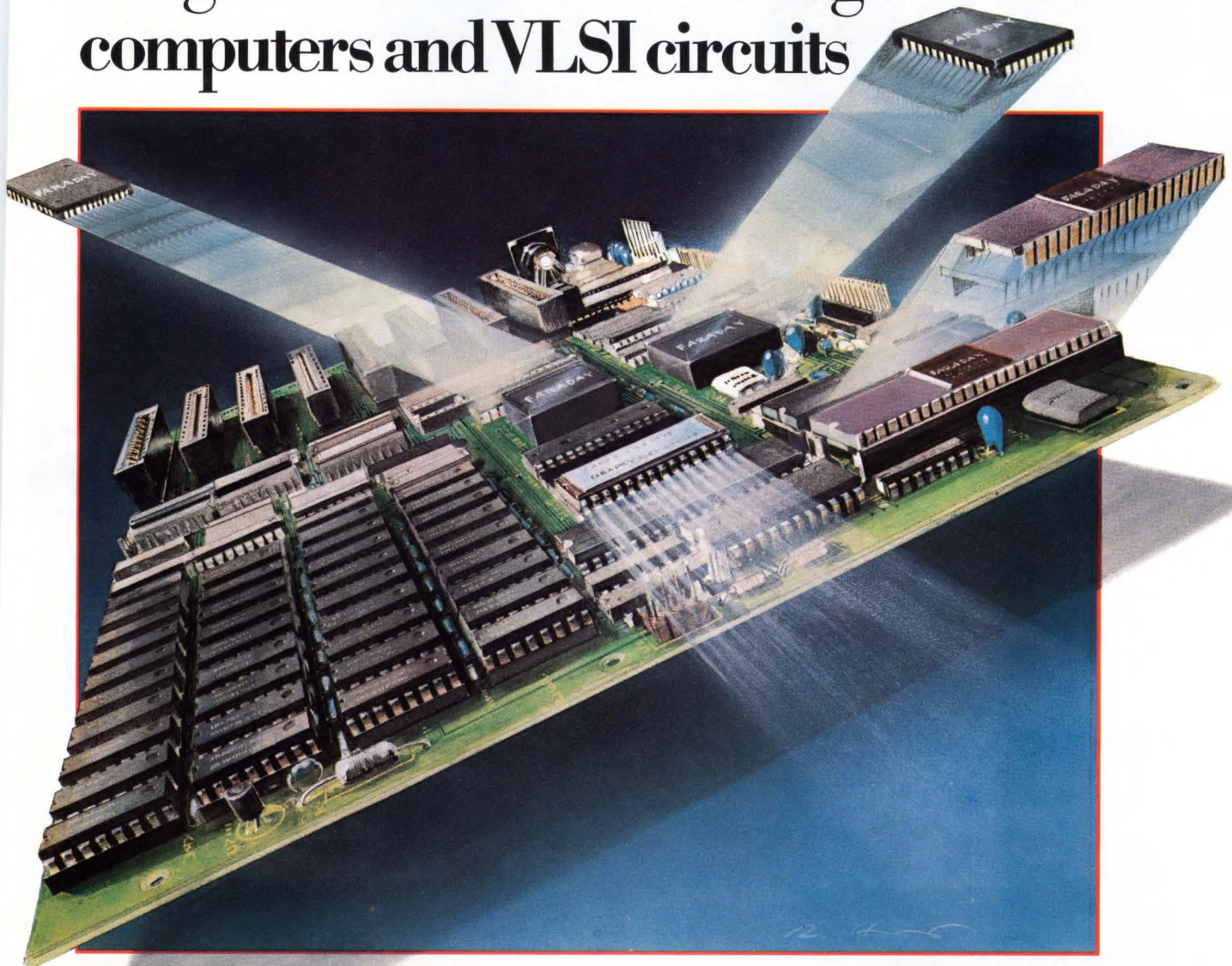
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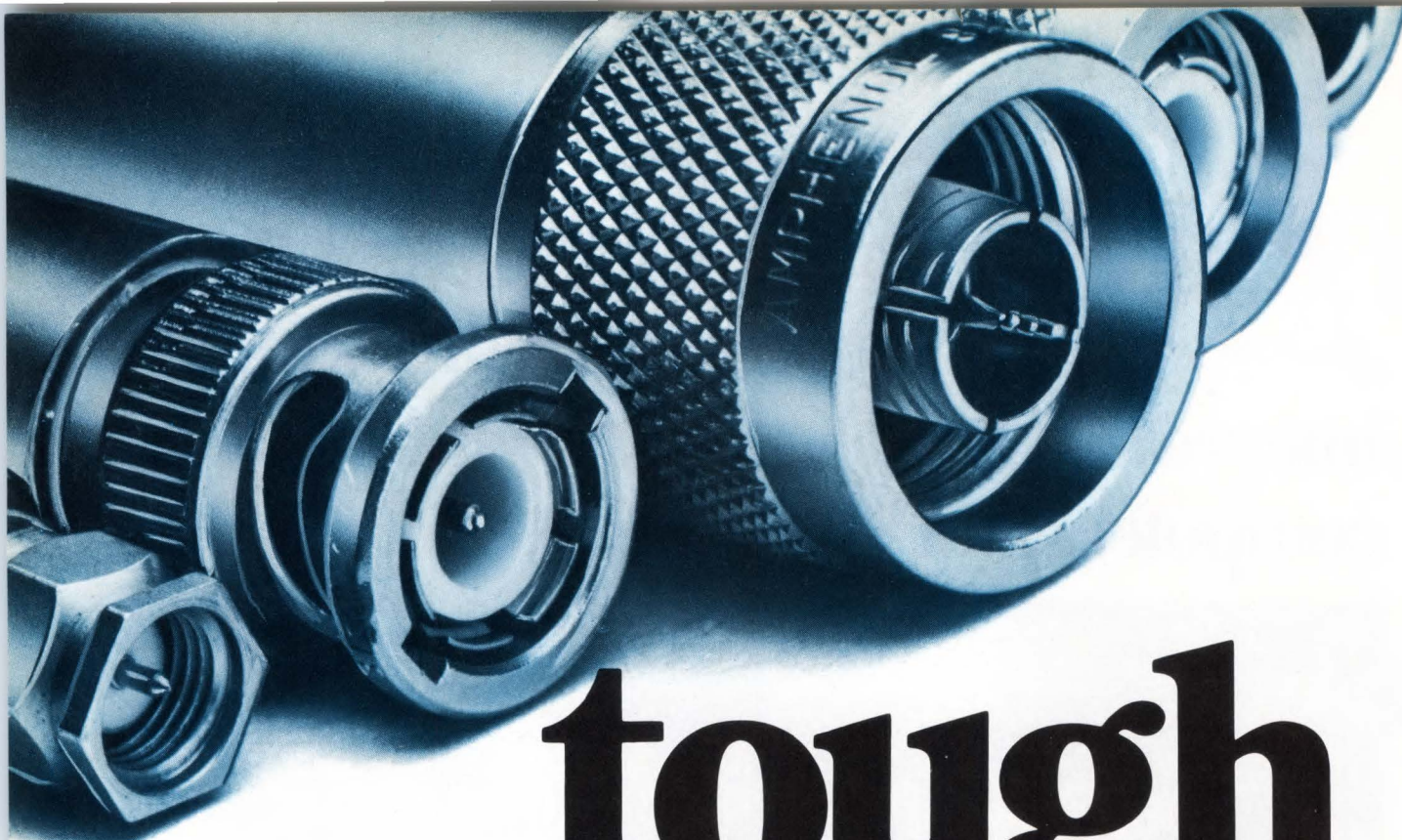
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3	●	■	●	●
4	●			
5	●			
6	●	■	●	●
7	●			
8	●			
9	●			
10	●	■	●	●
12	●			
15	●			
20	●	■	●	●
30	●	■	●	●
40	●	■	●	●

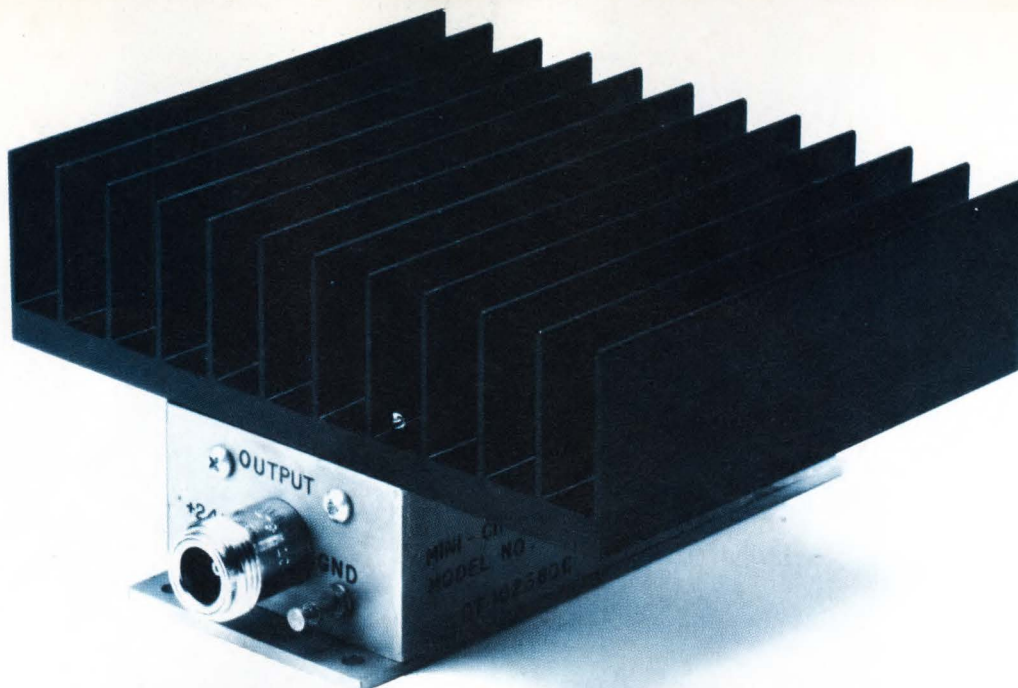
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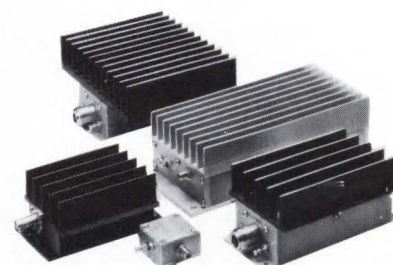
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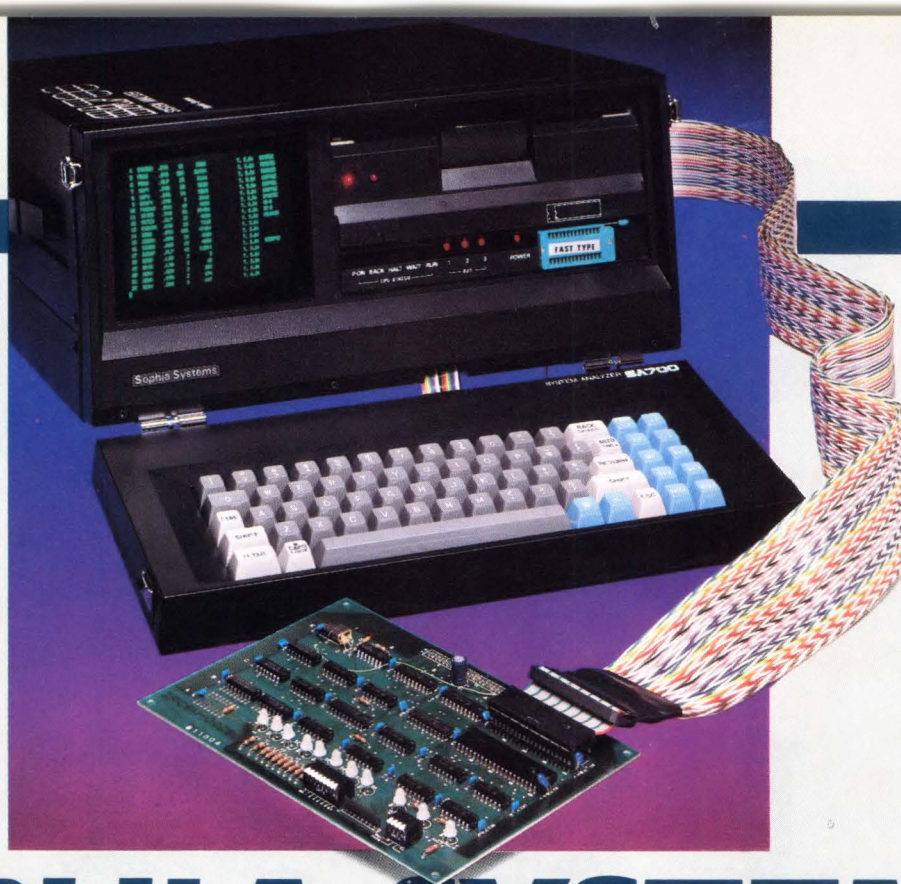


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PRODUCT REPORT

FOCUS ON ADVANCED LOGIC

Higher speeds and lower power requirements characterize the latest descendants of TTL. As is true elsewhere, CMOS looms large on the horizon.

Despite the march of integration, most systems still need some sort of glue logic to bind together their VLSI circuits. This glue—SSI and MSI components such as simple gates and registers—has kept pace with VLSI's move toward higher speed and lower power. Today's logic shows delay-power products that are anywhere from 7 to 25 times lower than that of the first transistor-transistor logic.

At present, the field is dominated by three mutually compatible logic families: advanced low-power Schottky (ALS), advanced Schottky (AS), and Fairchild advanced Schottky TTL (FAST). In addition to these descendants of Texas Instrument's original 54/74 TTL line, two CMOS logic types must be reckoned with as well. The HC family is a candidate to take over the territory traditionally dominated by bipolar technologies. HCT logic, on the other hand, is TTL-compatible and will probably serve as a bridge between the bipolar and CMOS eras.

For very high-speeds, ECL circuitry is available. Its high power consumption and poor noise immunity, however, restrict it to settings that simply cannot do without its blinding speed.

Of course, anytime speed is an issue, gallium arsenide must be considered. This is a very exciting technology, since it makes possible operating frequencies in excess of 1 GHz (Fig. 1), ensures radiation hardness and high-temperature operation, and holds out the potential for optical coupling. Despite its promise, the day of large families of standard GaAs logic has yet to dawn.

What does exist is a dynamic area in which manufacturers seem to be torn between standardization and differentiation. On one hand, they want to make the designer's job easier by guaranteeing compatibility. Alternatively, they want their own products to stand out. Indeed, although much of the technical material confuses the issue, the good news is that all the available TTL-based families are strongly

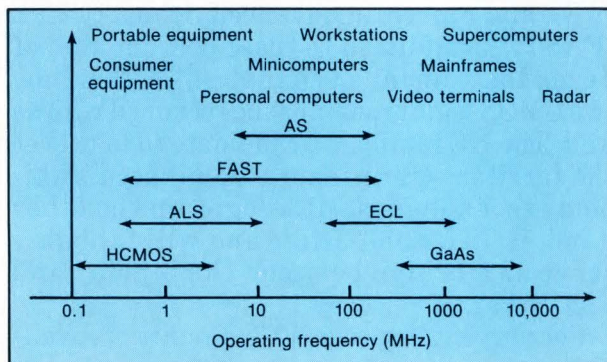
Heather Bryce

Focus on advanced logic

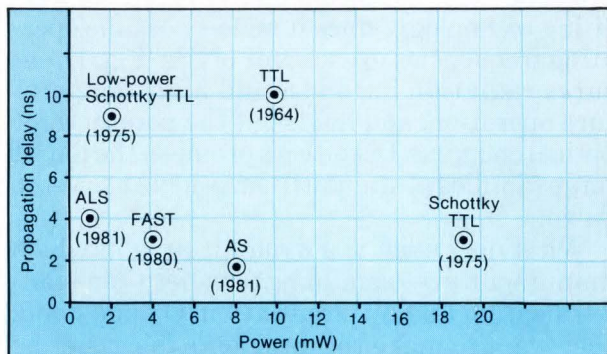
similar and can be mixed to build working circuits. What's more, the families keep growing. Error-correction circuits and bit-slice processors are about to join the flip-flops, counters, and multiplexers that are already familiar to designers.

Family feuds

The differences among ALS, AS, and FAST are their speeds and power dissipations (Fig. 2). AS is the fastest but dissipates the greatest amount of power. ALS, at the other extreme, consumes the least power but is also the slowest. FAST, for its part, stands roughly in the middle.



1. Speeds above 1 GHz demand gallium arsenide logic, which is not yet available in commercial families. At lower frequencies, a wide variety of technologies is on hand for applications ranging from portable equipment to supercomputers.



2. Just how much recently introduced logic surpasses its predecessors is illustrated by a delay-vs-power chart. The year of each family's introduction is also shown.

More specifically, AS has a propagation delay of about 1.7 ns and consumes 8 mW/gate. FAST cuts that consumption in half, while increasing delays to about 3 ns/gate. Finally, ALS dissipates only 1 mW and pushes delays to 4 ns, giving it the best delay-power product by far (see the table, opposite).

Perhaps predictably, yet somewhat amusingly, various manufacturers will advise certain combinations of technologies based on what they make. Since Fairchild employs only FAST, it recommends that technologies not be mixed. TI and National, in comparison, say that combining AS and ALS is the way to go. They recommend putting AS into the speed-critical paths and going with ALS elsewhere to keep a lid on power dissipation. Motorola ignores family relationships completely and suggests combining ALS and FAST, thereby attaining the fastest speed with the lowest power dissipation.

Designers quickly see that they may readily blend all three types of logic to suit their own purposes, whether they be highest speed, lowest power dissipation, or simply availability and inventory control. As similar as they are, though, each technology has particular advantages.

Direct descendant

Intended primarily to be an enhancement of the original 54S Schottky TTL, AS was originally intended to have one-half the 3-ns propagation delay of its progenitor and draw one-third of its 19 mW. Improvements were also looked for in line-driving capability, power-supply loading (reduced supply current spikes), and input characteristics—higher impedance, lower input current, and higher voltage thresholds. AS also was to eliminate malfunctions due to parasitic capacitance and to be protected against electrostatic discharges.

The technology is an oxide-isolated, walled-emitter bipolar process. Its emitter width is 2.5 μm . The design goals were almost completely met, the most impressive being speed. Even when driving a 100-pF load, AS has a propagation delay of less than 4 ns (Fig. 3).

Not far behind AS—in terms of speed—comes FAST. These circuits are pin-for-pin replacements for 74S family parts, yet they furnish one-third to one-fourth the power dissipa-

tion, as well as higher operating speeds. In fact, a designer can substitute FAST parts for their 74S equivalents and increase performance without making any other change beyond reducing the size of the power supply.

On different planes

FAST is based on an advanced isoplanar process, which means that components are isolated by a selectively grown thick oxide rather than by the p+ isolation region used in the planar approach. Since the oxide need not be separated from the base-collector regions, the chip size is reduced appreciably (Fig. 4). FAST's much smaller dimensions, in comparison with standard and low-power Schottky TTL, account for both its higher speed and its lower power.

When the process was introduced in 1978, it was intended to be the speediest technology out. Since its inception, both minimum and maximum ac propagation delays have been specified, eliminating the need to derate so-called typical specifications. The parts are specified using the conservative capacitive loading of 50 pF rather than the often used 15 pF. Lastly, the selection of devices has been well thought out: Only 100 functions are required to complete the family, as opposed to more than 300 for a combined AS and ALS family.

Further, in keeping with its original conception, FAST keeps growing steadily. Signetics recently introduced the 74F3040 and 74F3037 dual and quad two-input NAND gates, which feed a 30- Ω transmission-line driver. Fairchild itself just unveiled the FAST402 expandable serial-data polynomial generator-checker and is about to announce its first FAST LSI device—the 29F01, a 4-bit-slice processor. Basically, FAST LSI is a 50% reduction of conventional FAST. It is expected to come in with a gate delay of merely 1 ns and dissipate only 1 mW/gate. That would make it the most attractive logic family of all, except for its current shortage of members.

Low power indeed

Also making the scene at 1 mW/gate, ALS was designed to be an improvement over low-power Schottky—drawing one-half the power and delivering twice the speed. It also turns out to have a better noise margin, reduced input

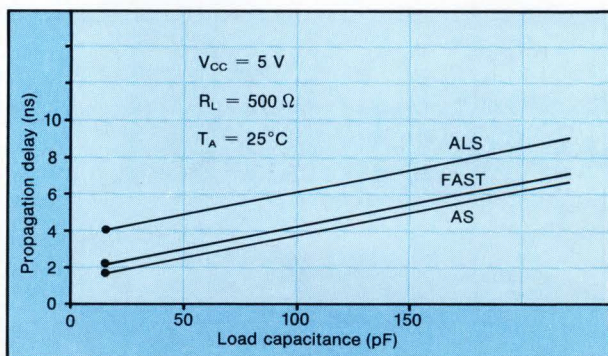
current, and superior line-driving characteristics. Of course, at 4 ns/gate, it is the slowest of the advanced logic families.

CMOS is cropping up in every area of the industry, and advanced logic is no exception. Although there are about half a dozen major players in high-speed CMOS (HCMOS), more than 20 companies are involved, and the number keeps growing. To decrease a designer's possible confusion, JEDEC standards are being defined for HCMOS. Thanks to this early effort, HCMOS will enjoy more standardization than did TTL. With so many manufacturers, this step is as necessary as it is welcome.

As noted, two classifications of HCMOS are available, dubbed HC and HCT. Both have the

Key characteristics of logic families			
Family	Propagation delay (ns)	Power consumption (mW)	Delay-power product (mW-ns)
AS	1.7	8	13.6
FAST	2.5-3.0*	4	10-12
ALS	4	1	4
Low-power Schottky TTL	9	2	18
Schottky TTL	3	19	57
TTL	10	10	100

* at 50 pF

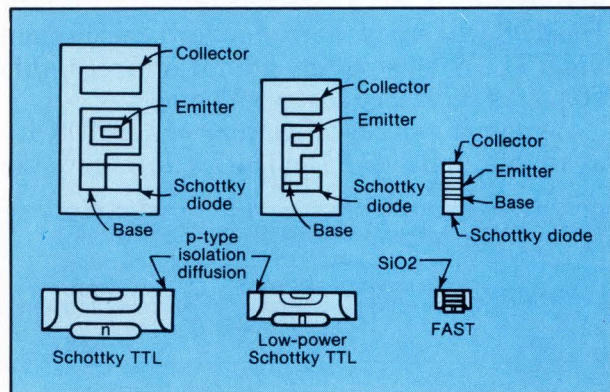


3. AS and FAST have comparable propagation delays, whereas ALS is somewhat slower. The last is thus best employed where speed is not critical but power consumption must be kept down.

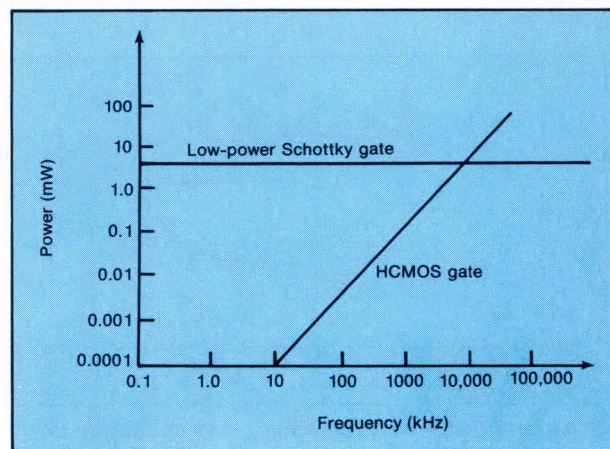
Focus on advanced logic

same functions and pin-outs as 74LS and CD4000. The difference lies in the fact that HC devices are true CMOS parts and HCT parts have TTL-compatible inputs. HCT will thus be used mainly to upgrade existing TTL designs. Designers will turn to it when they want to decrease the power consumption in a certain portion of their circuits, or when equivalent TTL parts are hard to come by.

A few companies offer almost an equal num-



4. Process and design enhancements have chipped away at device size over the years. FAST is appreciably smaller than either Schottky TTL or low-power Schottky, making it both faster and lower in power consumption.



5. The power dissipation of CMOS circuitry increases with frequency. Thus although CMOS logic draws practically no power at dc, there is a frequency above which it pulls more than bipolar. For low-power Schottky and HCMOS, the crossover frequency is around 7 to 10 MHz.

ber of HCT and HC parts. The vast majority, though, offer very few HCT devices compared to those fabricated with HC. The thinking behind this is that HCT is a temporary solution and will not be very important in the future. New designs will go completely to HC, they believe. Further, because of their TTL inputs, there is a slight degradation in HCT's performance in comparison with HC's.

It should be noted that a third type of HCMOS exists—HCU. It employs CMOS input switching levels but is unbuffered. At this time, there are only a handful of HCU parts.

Friend or foe?

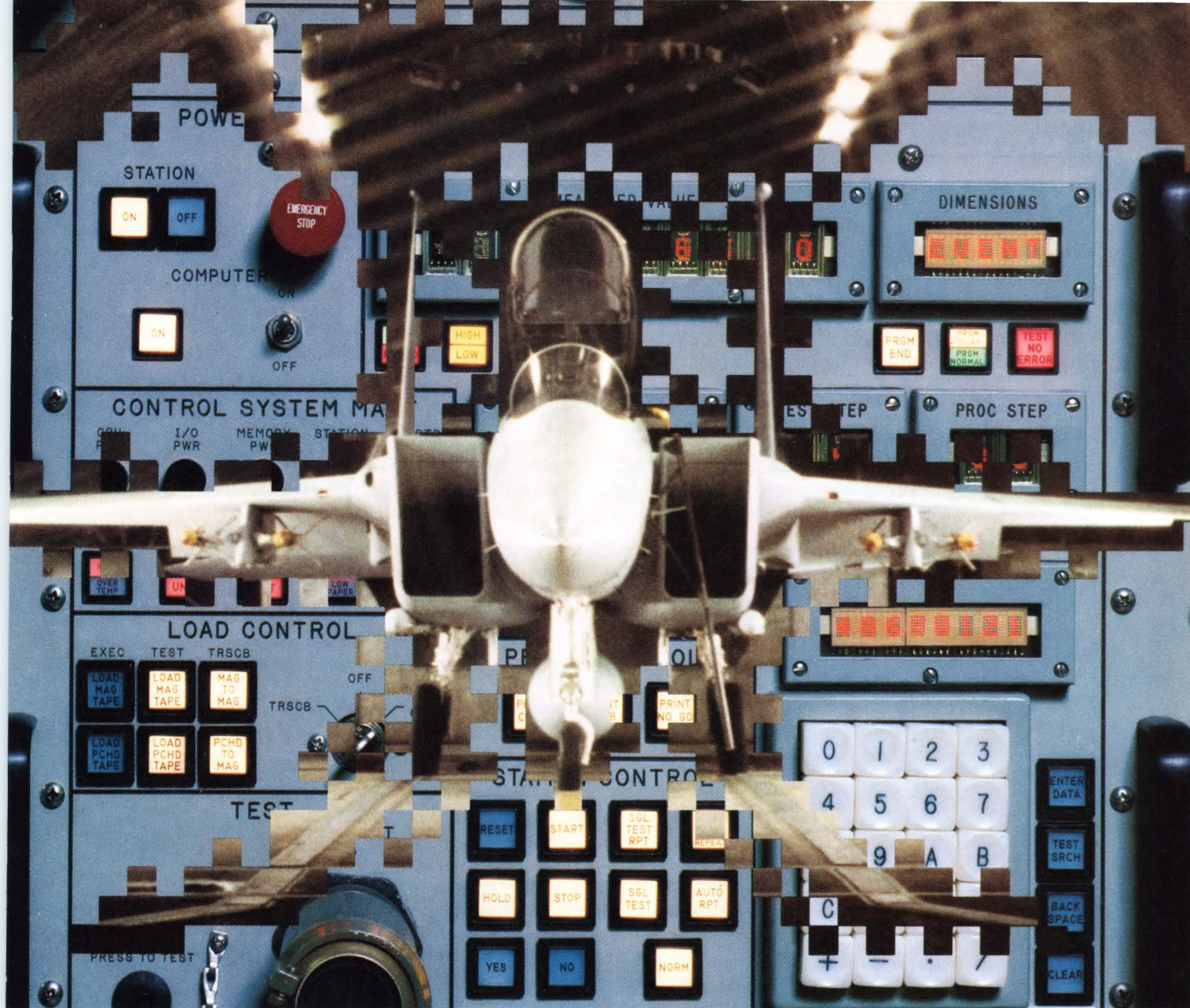
As with all CMOS, HCMOS's main attraction is its low power consumption. In this regard, however, it must be remembered that the power draw of the technology rises as frequency increases (Fig. 5). Advanced logic circuits are usually found where high speed is a prerequisite. These facts call into question CMOS's role as a competitor to bipolar logic.

The entire issue, it turns out, is a false alarm. In any system, relatively few devices will actually be operating at full speed at any given instant. Most will be in a static state, in which CMOS has a tremendous advantage. Manufacturers believe that overall power savings will be anywhere from 50% to 99.9% if CMOS replaces bipolar circuitry, even in high-speed applications.

Another important advantage of HCMOS is its intrinsically high noise immunity—30% to 45% of the supply voltage. That makes it two to three times better than TTL. A relaxed power-supply requirement is another of CMOS's strong suits. Whereas TTL requires $5\text{ V} \pm 10\%$, HCMOS can be driven with 2 to 6 V.

The main drawback of HCMOS is its speed, which is closer to that of low-power Schottky than to the other advanced logic families. Nevertheless, its low power consumption makes it very important.

The fastest logic available today is ECL, with its gate delays on the order of a few hundred picoseconds. Unfortunately, ECL has some problems. First, since it is a nonsaturating logic, it dissipates a large amount of power. Second, it uses a -5.2-V power supply with the high level at ground, so it is not compatible with



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PRODUCT REPORT

Focus on advanced logic

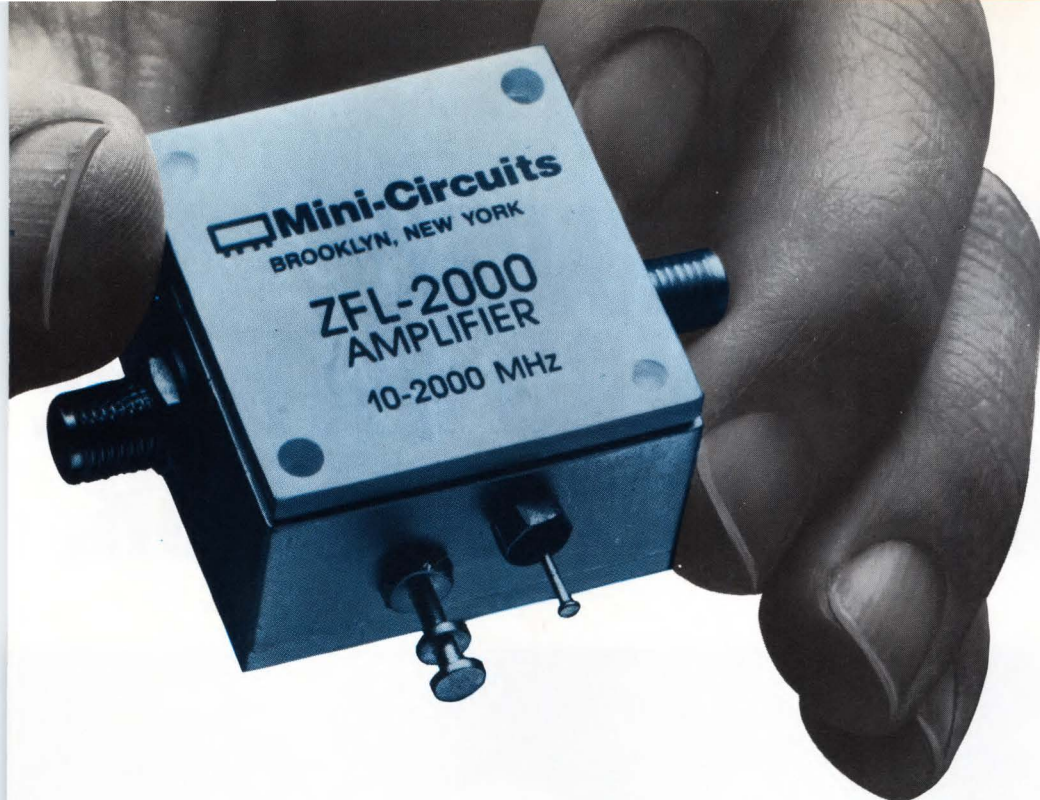
TTL. Thus mixing the technologies requires two power supplies. ECL's negative supply brings up another of its problems—its low noise immunity. The negative supply is an attempt to minimize that problem by operating the more susceptible positive rail at ground, where there is less noise.

Nevertheless, ECL is found in many applications—primarily mainframes and superfast computers. The important area for ECL is in semicustom cells. Motorola is now offering

macrocell arrays with anywhere from 600 to 2500 gates. These arrays contain different functions, such as flip-flops, latches, multiplexers, adders, and the like.

By allowing logic functions to reside on one chip rather than various SSI and MSI chips, the macrocell approach takes full advantage of ECL's speed. For this reason, it is possible that standard cells will be the shape of the future as far as advanced logic designs—at least in quantity—are concerned. □

Directory of advanced logic manufacturers											
	ALS	AS	FAST	HCMOS	Circle		ALS	AS	FAST	HCMOS	Circle
Fairchild Camera & Instrument Corp. South Portland, Maine (207) 775-8100			*		451	RCA Corp., Solid State Division Somerville, N.J. (800) 526-2177				*	465
Fujitsu America Inc. Santa Clara, Calif. (408) 727-4300				*	452	Sanyo Electric Trading Co. Ltd. Osaka, 570 Japan 06 992-1521			*		466
GTE Corp., Microcircuits Division Tempe, Ariz. (602) 968-4431				*	453	Semiconductor Process Inc. San Jose, Calif. (408) 945-1500				*	467
Hitachi America Ltd. San Jose, Calif. (408) 942-1500				*	454	SGS Semiconductor Corp. Phoenix, Ariz. (602) 867-6222				*	468
Integrated Device Technology Santa Clara, Calif. (408) 727-6116				*	455	Sharp Corp. Osaka, 545 Japan 06 621 1221				*	469
Matsushita Electric Industrial Co. Inc. Moriguchi, Osaka, Japan 06 909 1121				*	456	Signetics Corp. Sunnyvale, Calif. (408) 739-7700			*	*	470
Mitel Corp., Semiconductor Division Kanata, Ont., Canada (613) 592-5630				*	457	Solid State Scientific Inc. Montgomeryville, Pa. (215) 855-8400				*	471
Monolithic Memories Inc. Sunnyvale, Calif. (408) 970-9700				*	458	Supertex Inc. Sunnyvale, Calif. (408) 774-0100				*	472
Motorola Semiconductor Products Inc. Austin, Texas (512) 928-6000				*	459	Telmos Inc. Santa Clara, Calif. (408) 727-1501				*	473
Motorola Semiconductor Products Inc. Phoenix, Ariz. (602) 244-6900	*		*		460	Texas Instruments Inc. Dallas, Texas (214) 995-3333	*	*		*	474
National Semiconductor Corp. Santa Clara, Calif. (408) 721-5000	*	*		*	461	Toshiba America Inc. Tustin, Calif. (714) 730-5000				*	475
NEC Electronics USA Inc. Sunnyvale, Calif. (408) 745-6520				*	462	Universal Semiconductor Inc. San Jose, Calif. (408) 279-2830				*	476
Nitron Inc. Cupertino, Calif. (408) 255-7550				*	463	Vatic Systems Inc. Mesa, Ariz. (602) 962-8998				*	477
OKI Semiconductor Santa Clara Calif. (408) 720-1900				*	464	Zytrex Corp. Sunnyvale, Calif. (408) 733-3973				*	478



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- Extending the frequency range of signal generators when using a frequency doubler, filter and then amplifying.
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NOISE FIGURE	7.0 dB
INTERCEPT POINT (3rd order)	25 dBm
VSWR, 50 OHMS	2:1
DC POWER volt, current	+15 V, 100 mA
HEAT SINK	Internal
OPERATING TEMP	-55°C to $+100^{\circ}\text{C}$

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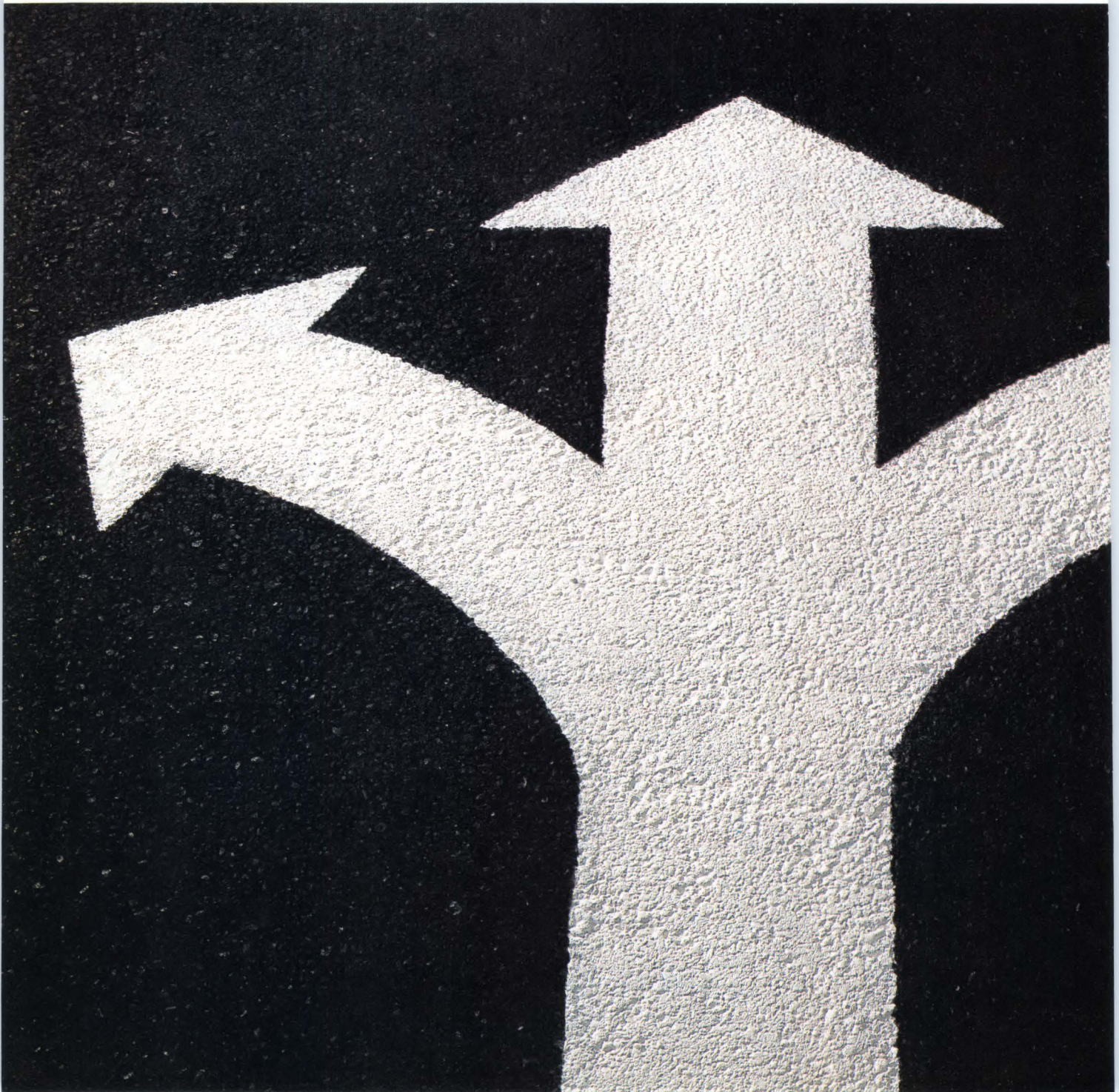
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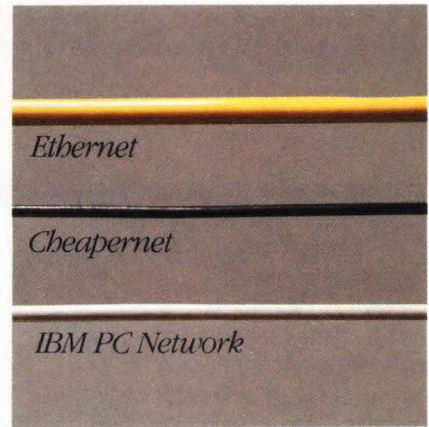
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Integrating ADC chip builds complete autoranging 3½-digit DMM

Manufacturers of hand-held digital multimeters can now use an integrating analog-to-digital converter to construct a complete 3½-digit autoranging instrument. The TSC805 converter chip, developed by Teledyne Semiconductor, does the same job as the industry-standard 7106 but without the dozen or so extra ICs that the latter needs. Moreover, the converter works over a wider range and performs more functions.

The automatic selection of ranges simplifies the mechanical design and construction of the multimeter and also makes it simpler to use. In addition, ranges can be selected manually merely by adding a single-pole momentary contact switch. Resolution is 1 part in 2000 for all automatic selections, 1 part in 3000 for manual selections.

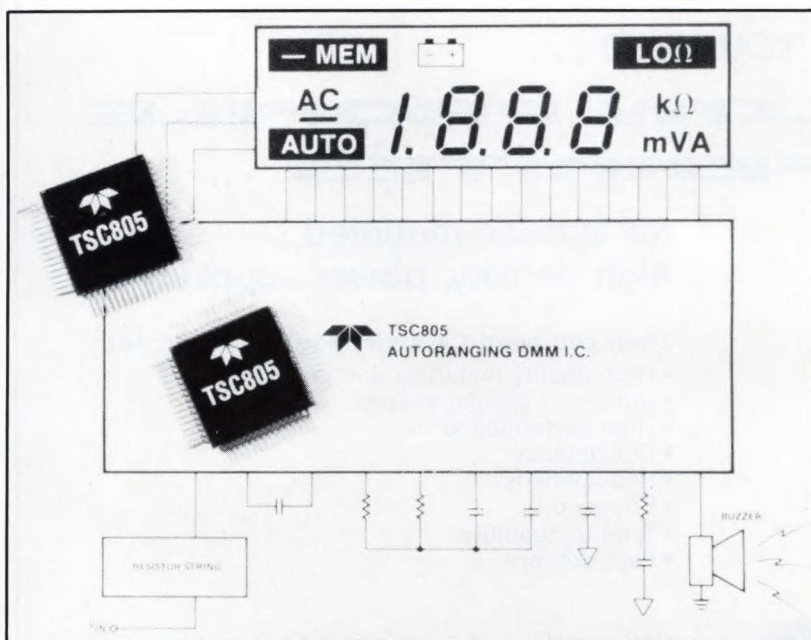
With the a-d converter, the instrument can select five dc voltages, ranging from 200 mV to 2000 V full scale. It also can measure resistances in five ranges, from 200 Ω to 2 M Ω . In addition, four low-power ranges—2 k Ω to 2 M Ω —

limit open-circuit voltage to 350 mV, so that resistances can be measured on pc boards without forward-biasing semiconductor junctions.

With the help of a few external diodes, resistors, and capacitors, the converter's on-chip op amp proves valuable in building precision rectifiers that can measure ac voltage from 2 to 1000 V full

scale. As an added benefit, the instrument can work with a pair of manually set current ranges: 20 and 200 mA full scale.

The display driver circuit directly drives the latest triplex-type LCD, which continuously informs the user about the operating mode, the full-scale range, and the position of the decimal point. For



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CIRCLE 136

NEW PRODUCTS

instance, the LCD flashes for overrange conditions and when it detects a low battery. For extra security, an on-chip audio oscillator, running at 4 kHz, activates a buzzer that announces those conditions, too. The buzzer also can be used for measuring continuity, sounding off when the reading drops below 1% of full scale.

A two-digit memory on the chip helps in making measurements and displaying them relative to a user-stored constant offset, which extend to $\pm 5\%$ of full scale. Typical applications include probe-resistance and tare-weight compensation.

Although designed primarily for digital multimeters, the converter can be incorporated in special-purpose instrument systems, where it can be used, for example, for sensor linearization or as a peak detector.

The chip's precision reference has a temperature coefficient of just 50 ppm/ $^{\circ}C$, and the entire chip needs a mere 10 mW from a 9-V battery.

The chip is housed in a 60-pin quad plastic package, with either formed or straight leads. It works over a temperature range of 0° to $+70^{\circ}C$ at a maximum operating voltage of 15 V.

The TSC805 sells for \$13.20 in quantities of 100, and small amounts are available from stock.

Teledyne Semiconductor Inc., 1300 Terra Bella Ave., PO Box 7267, Mountain View, Calif. 94039; Dave Gillooly, (415) 968-9241.

CIRCLE 305

Digitally programmable 8-pole active filters boast solid-state tuning

A family of digitally programmable eight-pole active low-pass filters is the first to rely on solid-state tuning in lieu of mechanical relays, thus offering all the advantages of the former. From Frequency Devices, the Model 848 filters use an 8-bit word to set their cut-off frequency at some value within a 256:1 range.

The family contains 10 members, 5 with a Bessel response and 5 with a Butterworth response. One model in each set covers one of these

frequency bands: 0.1 to 25.6 Hz, 1 to 256 Hz, 10 Hz to 2.56 kHz, 100 Hz to 25.6 kHz, and 200 Hz to 51.2 kHz.

The 8-bit word input is applied to 8-bit clocked CMOS latches that accept 15-V CMOS-compatible data and command inputs. The filters can be programmed to transfer data with a strobe, or the latches can be transparent.

Each filter contains high-gain op amps with resistor-capacitor tuning networks in their feedback loops. The solid-state switches driven by the latches form RC combinations that tune the filter to

the selected frequency. Within each range the highest tunable frequency is $f_{\max}$; the lowest is $f_{\max}/256$. Tuning stability is within $\pm 0.01\%/^{\circ}\text{C}$.

Inverting gain for all models is ± 0.5 dB at dc. At the -3 -dB corner frequency (f_c), both Bessel and Butterworth filters have a gain tolerance of ± 0.2 dB. When the filters roll off 70 dB, gain deviation from the theoretical is ± 2 dB for the Butterworth and ± 3 dB for the Bessel models.

Input impedance is 20 k Ω , and output impedance is 10 Ω . Each filter operates from ± 12 - to ± 18 -V supplies. Output noise is just 50 μV rms. Maximum dc offset voltage is 20 mV.

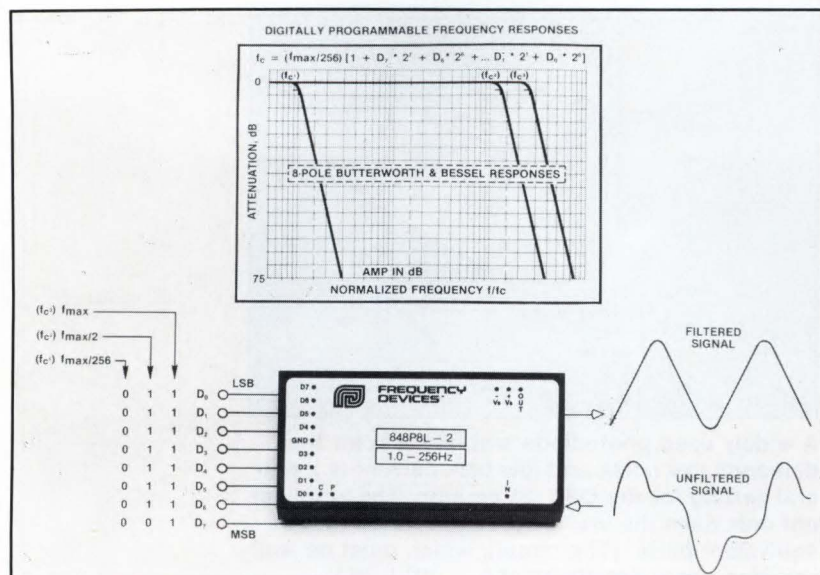
The filters are contained in 2-by-4-in. modules. The two lower-frequency units are just 0.7 in. high; the others, 1 in. high. All operate over 0° to 70°C .

Small quantities are available from stock. All family members sell for \$300 each for up to 9 units and \$200 in 100-unit lots.

Frequency Devices Inc., 25 Locust St., Haverhill, Mass. 01830; Warren Munroe, (617) 374-0761.

CIRCLE 309

Frank Goodenough



Inexpensive op amp features low noise and low bias current

Typically, working with low-cost monolithic op amps involved a series of tradeoffs: low noise could be had, say, but only at the price of high bias current. Burr-Brown's OPA121A puts an end to that problem, boasting a typical noise figure of $6 \text{ nV}/\sqrt{\text{Hz}}$ at 10 kHz and drawing a maximum current of 5 pA. What's more, it comes in at close to half the price of competitive devices.

These impressive specifications open up a range of applications long closed to inexpensive op amps, including optoelectronics (see the figure) and test and medical equipment. It also is a natural in settings where radiation resistance is a must, because of the dielectrically isolated process used to build it.

The OPA121 exhibits an offset of 2 mV maximum with a typical offset drift of $3 \mu\text{V}/^\circ\text{C}$. Some bipolar components, it is true, offer lower offset voltage drift—in the 250- μV range. Yet with a bias current that is several orders of magnitude lower, the 121 shows far better overall characteristics. Its open-loop gain

of 110 dB maximum and common-mode rejection ratio of no more than 86 dB further demonstrate its impressive credentials.

Critical to attaining such performance is the dielectrically isolated bipolar process employed to build the amplifier's FETs. The DIFETs, as they are called, are made by fabricating ion-implanted low-noise JFETs in dielectrically isolated tubs.

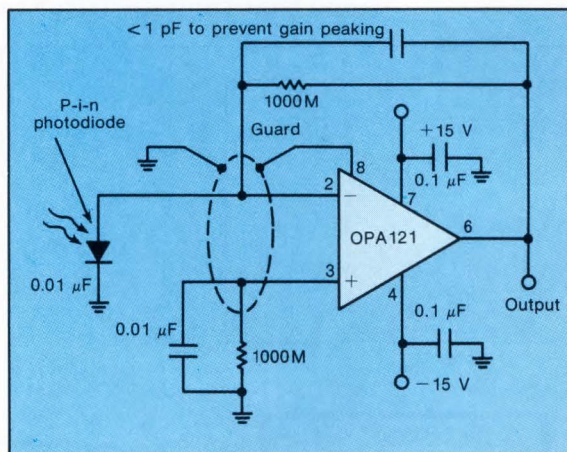
The dielectric isolation means that no special input protection is required, such as

the external current-limiting resistors found on conventional monolithic FET op amps. On-chip guard circuits further enhance the op amp's performance.

The OPA121KM, housed in a TO-99 metal can, and the OPA121KP, mounted in a plastic mini-DIP, are available from stock. In lots of 100 or more, they cost \$5.95 and \$5.40 each, respectively.

Burr-Brown Corp., PO Box 11400, Tucson, Ariz. 85734; Naresh Shah, (602) 746-1111.

CIRCLE 303



A widely used photodiode amplifier circuit that demands low noise and low bias current is a natural setting for the OPA121 op amp. The amplifier not only does the job, it costs about half that of equivalent parts. (The circuit, which must be well shielded has a sensitivity of $5 \times 10^8 \text{ V/W}$.)

Heather Bryce

ANALOG

A-d converter guarantees ± 1 LSB

CMOS design and process technology enable the AD7582 a-d converter to guarantee low error and no missing codes over its operating temperature ranges without sacrificing speed. The four-channel successive-approximation converter guarantees a maximum total unadjusted error—including gain, offset, and differential linearity errors—of ± 1 LSB. Furthermore, it has a maximum conversion time of 100 microseconds.

To achieve its rated accuracy, the AD7582 requires a +5-V external reference and several passive components. The device is available specified for the commercial, industrial, and military temperature ranges, with respective prices of \$32.50, \$37.50, and \$92.37 in lots of 100.

Analog Devices Inc., 804 Woburn St., Wilmington, Mass. 01887; (617) 935-5565.

CIRCLE 316

D-a chip supplies composite signals

The second in a series of 8-bit CMOS digital-to-analog converters for color graphics terminals, the TML1842 is a low-cost, space-efficient alternative for systems that do not require adjustable composite video signals. Housed in a 20-pin 0.3-in.-wide DIP, the converter has the same specifications as the earlier TML1840 except that its composite

video signals are not adjustable and signal invert is not supplied.

The TML1842, which has a nonlinearity of 1 LSB, can drive 75- or 37.5- Ω loads while operating at a conversion rate

of 25 MHz. It provides composite sync, composite blank, and 10% brightness signals.

Telmos Inc., 740 Kifer Road, Sunnyvale, Calif. 94086; (408) 732-4882.

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ANALOG

12-bit a-d chip sports four inputs

For the first time a monolithic analog-to-digital converter blends 12-bit resolution and accuracy with

four input channels. Analog Devices' AD7582 has a guaranteed total unadjusted error of ± 1 LSB over its operating

temperature range, a specification that ensures no missed codes. (Unadjusted error includes gain, offset, and non-linearity). Conversion time is 100 μ s.

The autozeroing comparator in the chip ensures an offset error of $\pm 1/4$ LSB and acts as a high-impedance buffer amplifier between the input multiplexer and the thin-film digital-to-analog converter. Unlike most successive-approximation devices, which pump current into the signal source (necessitating a fast op amp to drive it), the 7582 connects directly to impedances as great as 2000 Ω .

Like most CMOS converters, it requires a reference voltage, which must be 5 V $\pm 5\%$ to meet specifications, and operates from ± 5 -V supplies. The full-scale input also is 5 V.

The digital output is available in two bytes of 8 LSBs and 4 MSBs, and either byte can be first. A 2-bit word selects the channel, and standard signals (CS, RD, and WR) control the chip.

The converter, housed in a 28-pin DIP, is available in three grades: plastic commercial (KN), ceramic industrial (BD), and ceramic military (TD). The respective prices are \$32.50, \$37.50, and \$92.34, all in quantities of 100 units.

Analog Devices Inc., PO Box 280, Norwood, Mass. 02062; Dan Domanski, (617) 935-5565.

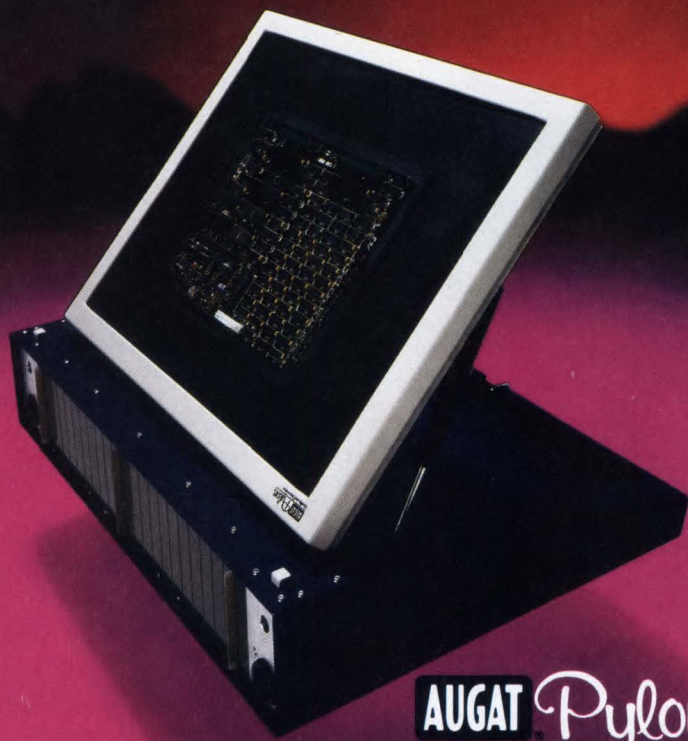
CIRCLE 311

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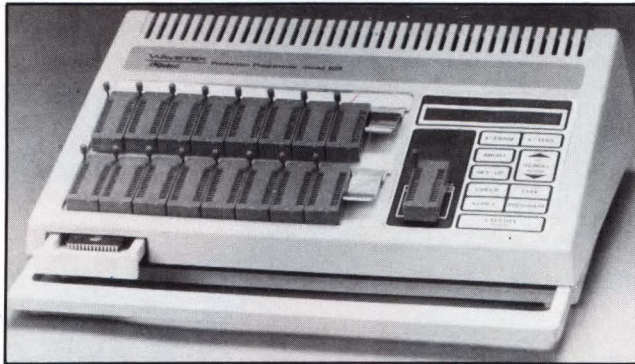


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Gang programmer updates with plug-in cartridges



As product designs increasingly rely on large amounts of firmware, a cost-effective production programmer that simultaneously handles up to 16 devices and can be updated quickly is good news for all. Capable of programming all available EPROMs and EEPROMs with capacities of up to 512 kbits, the Model 828 from Wavetek-Digelec features fast programming algorithms that shorten device programming time.

Moreover, since the unit is easily updated by means of plug-in software cartridges that contain programming algorithms for new devices, the user does not have to return it to the factory or service center for that purpose. Another advantage to having the device type accommodated by software is that the programmer requires no adapters or characterizers to accommodate different memory parts.

As an added convenience, the unit has a built-in eraser,

a feature not normally found in gang programmers.

A clearly marked keyboard and interactive software simplify programming of the unit by guiding the user in plain English. Device programming is initiated by a single keystroke that invokes an automatic test and programming sequence.

The sequence performs master EPROM check-sum testing, blank checking, device programming, programmed device check-sum verification, and check-sum error indication. What's more, the unit automatically detects conditions such as overloads and reversed or dislocated chips.

Easily transported, the unit is only 37 cm wide by 10 cm high by 25 cm deep and weighs just 14 lb.

The 828 is priced at \$2395 for a single unit. It will be available starting in December.

Wavetek-Digelec, 586 Weddel Drive, Suite 1, Sunnyvale, Calif. 94089; (408) 745-0722.

CIRCLE 314

Bob Milne

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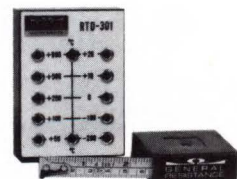
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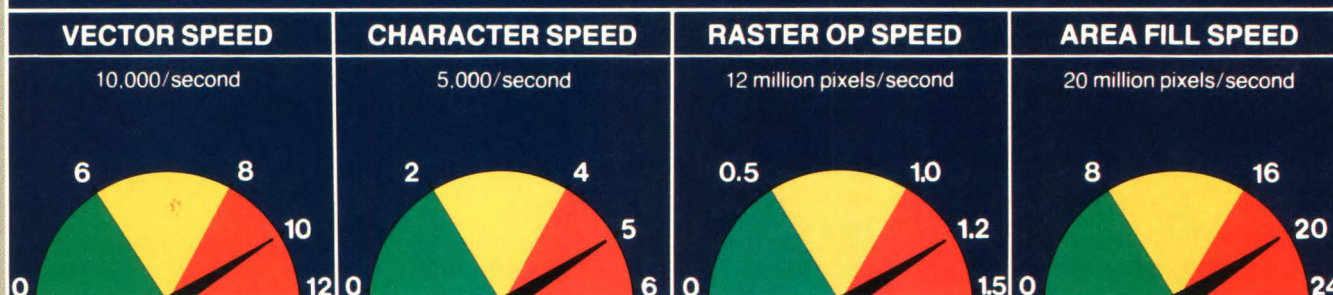
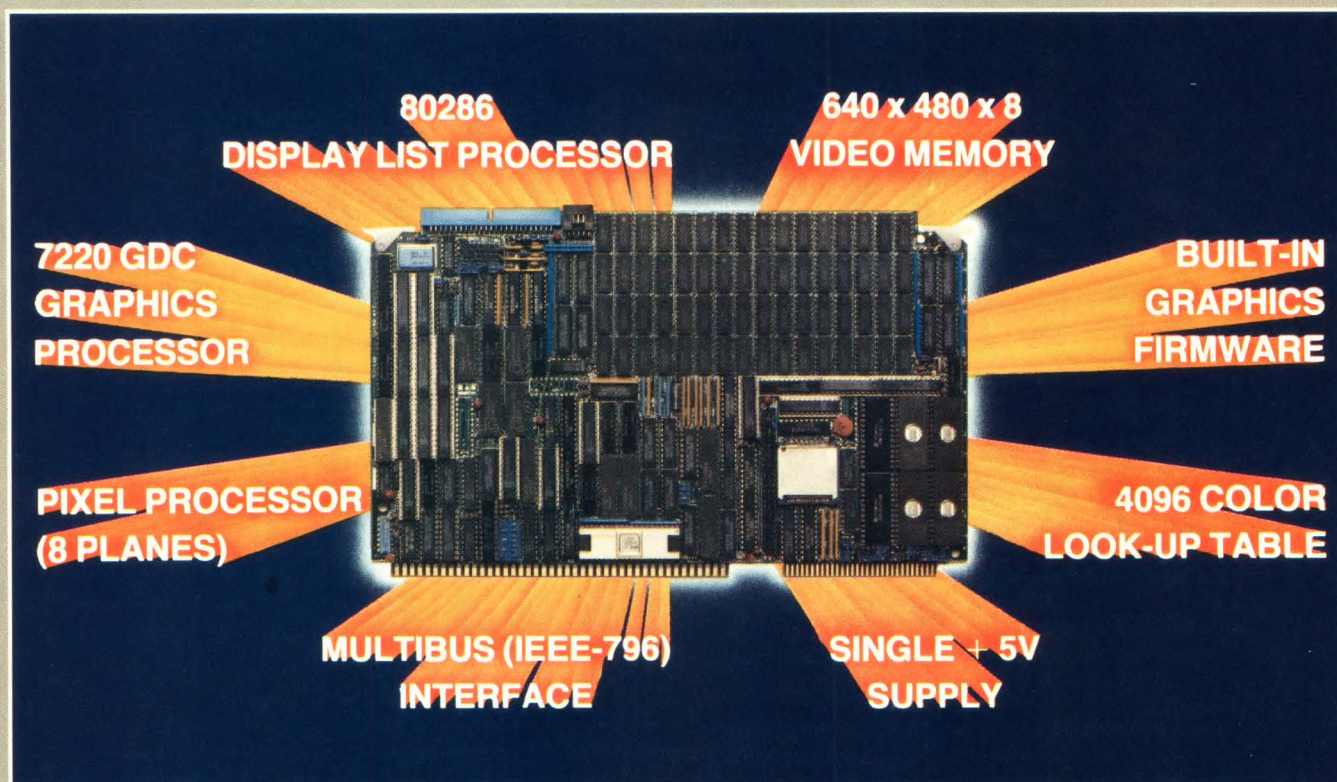
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- 7220 GDC graphics primitive processor
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The new Matrox SX-900 is a high performance color graphics display controller. It is the perfect solution for OEM manufacturers of process control and instrumentation equipment. The SX-900 is software compatible with the popular Matrox GXB-1000A high resolution display controllers, but occupies only a single Multibus card slot, and provides high speed drawing capability.

The hardware provides 640 x 480 pixel resolution, 4 or 8 bit planes, a 4096 color look-up table, and a 60Hz flicker free video refresh rate. The fast performance of the SX-900 results from a multi-processor pipelined architecture. A powerful 80286 CPU is used as the front end display list processor and is supported by a 7220 graphics primitive

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processor and a high speed pixel processor for simultaneous 8 plane drawing.

The SX-900 incorporates the proven on-board graphics firmware used by the GXB-1000. Over 256 high level display list commands are supported including line drawing, character drawing, circle and arc drawing, area fills, cursors and raster ops.

In addition to graphics boards, Matrox can also supply color monitors, cardcages, CPU cards, memory boards, and communications controllers for complete OEM display system requirements.

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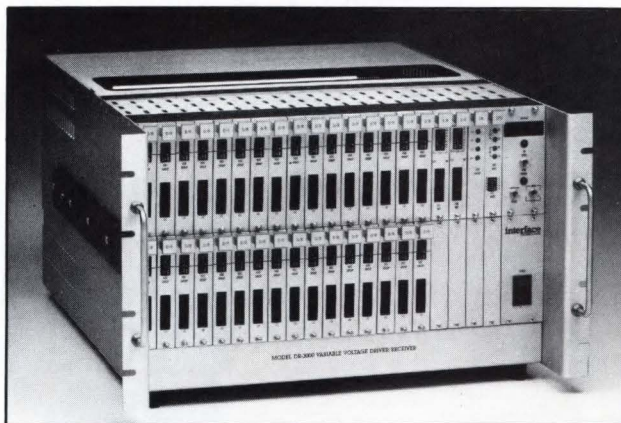
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NEW PRODUCTS

INSTRUMENTS

Logic-level converter handles 144 channels



A single piece of digital test equipment can drive up to 144 stimulus/response channels at different voltage levels using a programmable logic-level converter. The voltage levels can be set individually for each of 36 modules (cards) containing four drivers and receivers. The DR-3000 converter from Interface Technology also compares voltage levels and buffers its test connections.

Designed to augment standard digital test setups, the converter receives TTL-level signals from instruments such as a digital word generator or a pattern generator and translates them into programmed voltage levels that are passed on to the target unit. It accepts three-state TTL inputs and can be configured for bidirectional or unidirectional operation, delivering corresponding three-

state outputs. Levels can be set from -15 to $+15$ V, with logic swings of 15 V pk-pk at a resolution as fine as 10 mV.

The unit handles data rates of up to 10 MHz. Signals received from the target equipment can be converted and passed back to the tester.

The DR-3000 has an IEEE-488 interface. Output voltage levels and input thresholds are fully programmable. The front panel can be disabled remotely as well.

A self-test is run when the unit is powered up. All necessary power supplies are internal, and maximum power dissipation is 1100 W. The output signal rise and fall times are 15 ns at no load and 30 ns with a 100-pF load.

The DR-3000 is in stock for \$8000, and a driver-and-receiver module costs \$1550.

Interface Technology Inc., 150 East Arrow Highway, San Dimas, Calif. 91773; (714) 599-0848.

CIRCLE 313

Ray Weiss

INSTRUMENTS

1-GHz signal generator costs \$3950

A synthesized signal generator that spans a frequency range of 10 kHz to 1 GHz offers many

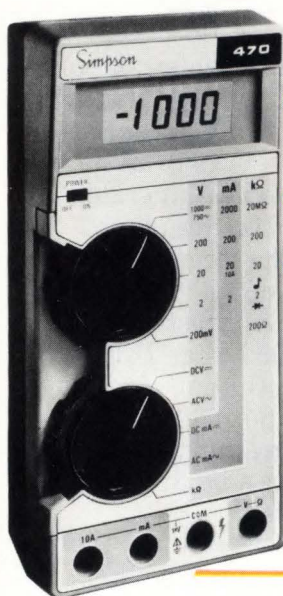
of the capabilities found in instruments that cost upwards of 25% more for only \$3950. The Model 2022, from Mar-

coni Instruments, packs its performance into a compact 6-by-10 $\frac{1}{4}$ -by-14 $\frac{1}{2}$ -in. package that weighs only 16.5 lb.

Frequency, phase, and amplitude modulation functions enable the Model 2022 to be used for testing practically all types of radio equipment. Accuracy is held to within ± 1 dB for outputs above -10 dBm

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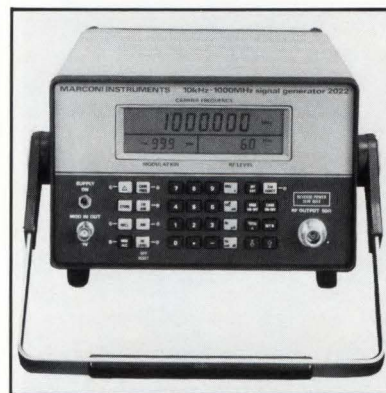
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CIRCLE 142



and to within ± 2 dB for outputs below -10 dBm.

The instrument's liquid-crystal display provides a simultaneous readout of carrier frequency, modulation, and rf level, and push-button entry simplifies operation. Up to 100 settings can be stored in the unit's nonvolatile memory to speed routine measurement tasks.

Although ideally suited for field service, the signal generator can also be used for benchtop and laboratory applications when fitted with an \$195 IEEE-488 interface.

Marconi Instruments, 3 Pearl Court, Allendale, N.J. 07401; Keith Elkins, (201) 934-9050.

CIRCLE 306

INSTRUMENTS

Function generator is phase-locked

Their ability to produce multiple waveforms makes function generators indispensable not only on the test bench but in systems too. The Model 23, from Wavetek, is of even greater value, as it is phase-locked to a crystal oscillator.

Operating from 100 μ Hz to 32 MHz, the unit sports a frequency accuracy of $\pm 0.005\%$, as well as a rotary encoder and an LCD for setting the desired frequency. It is programmable over optional RS-232 or IEEE-488 interfaces and features AM, FM, trigger,



and gate modes.

At frequencies of dc to 12 MHz, sine, square, or triangle waves can be generated, and ramp and haversine signals are available up to 1 KHz. The generator's synthesizer-based clock mode supplies TTL or ECL drivers for frequencies of up to 32 MHz.

Its built-in microprocessor

works the unit's 2-line-by-16-character interactive alphanumeric display. The processor also converts frequency and amplitude units and handles internal calibration. Further, its battery backup ensures that the unit retains its setup conditions.

The Model 23 costs less than \$2000. An optional RS-232 or IEEE-488 interface adds about \$300. The unit is available now.

Wavetek Corp., 9045 Balboa Ave., San Diego, Calif. 92123; (619) 279-2200.

CIRCLE 304

EPROM programmer handles 32-bit data

The E12 programmer eases the programming of EPROMs for 16- and 32-bit microprocessors. Whereas many programmers have a single socket for copying, the E12 has four. These can be configured as sets of two for data widths of 16 bits or as a single set for data widths of 32 bits. It can, of course, be used for programming four separate EPROMs intended for use with a single 8-bit processor. Additionally, the E12 can be used as a multiple EPROM copier, with the same data being applied to each of the four sockets.

Programming is accomplished either manually or via a computer linked to the instrument's standard RS-232-

C interface. The E12 accommodates all single-supply devices from 8 to 512 kbits.

Electronic System Products Inc., 1135-C San Antonio Road, Palo Alto, Calif. 94303; (415) 964-5338. \$2200.

CIRCLE 426

Plug-in board links IBM PC with 488 bus

A plug-in board that interfaces an IBM PC or PC-compatible computer with the IEEE-488 bus comes with ROM-based software that supports Tektronix standard codes and formats, most Hewlett-Packard control statements, and standard IEEE-488 command mnemonics. The interface board, designated the PC-488, provides 14 registers for direct

access to the data bus, the bus-management lines, and the DMA control lines. An optional cache RAM transmits and receives up to 64-kbyte arrays at 790 kbytes/s; rates greater than 400 kbytes/s can be achieved with standard system RAM.

All device functions, addresses, interrupt conditions, and serial/parallel poll responses are programmable to allow emulation of any device function at any address without moving jumpers. The PC-488 supports interpreted and compiled Basic, Microsoft Pascal, Microsoft C, Lattice C, CWARE C, and assembly language.

Capital Equipment Corp., 10 Evergreen Ave., Burlington, Mass. 01803; (617) 273-1818. \$395.

CIRCLE 427

INSTRUMENTS

HP-150 serves as instrument controller

With the HP-IB enhancement library, the HP 150 computer can be used as a powerful and flexible instru-

ment controller. The library contains assembly language subroutines that enable the HP 150 to utilize its built-in HP-IB interface to communicate with any device that adheres to the IEEE-488 pro-

tol. The subroutines are callable from most HP 150-supported languages, including MS Basic, MS Pascal, and MS Fortran.

The software comes on a 3½-in. disk and includes Basic programs that demonstrate the use of the library for touch-screen instrument control.

Optimatic Solutions, 7013 Owensmouth Ave., Suite 105, Canoga Park, Calif. 91303; (818) 716-4088. \$450.

CIRCLE 318

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For more information on components from the leader in telecom technology, call Teltone today: 1-800-227-3800, ext. 1130.

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Teltone Corporation, the telecommunications company, P.O. Box 657, Kirkland, WA 98033. In the east call: Teltone Corporation, (904) 262-6910. In Canada, contact: Teltone Ltd., 183 Amber Street, Markham, Ontario L3R 3B4, (416) 475-0837.

Low-cost synthesizer spans 0.4 to 1050 MHz

Demonstrating an excellent price/performance ratio is the 6060A 1-GHz synthesized signal generator, which meets or exceeds the performance of units costing over \$6000. The fully loaded package, including an optional IEEE-488 interface and reverse power protection, is only \$5000; just \$500 above the base price of \$4500.

The instrument covers a range of 400 kHz to 1050 MHz, which is selectable with 20-Hz resolution, and it has a typical switching speed of less than 100 ms. Harmonics are kept to less than -30 dBc across the entire frequency range, while spurious signal levels are less than -60 dBc. The generator provides output power from -137 to +13 dBm, accurate to within ± 1.5 dB with a resolution of 0.1 dB.

John Fluke Mfg. Co. Inc., PO Box C9090, Everett, Wash. 98206; (206) 342-6300.

CIRCLE 319

Encoder-decoder chip ties USARTs into low-cost LANs

A single-chip bipolar Manchester encoder-decoder links USARTs to coaxial or twisted-pair cable. Thus it can help build low-cost local-area networks that transfer data at 500 kbits/s to 3 Mbits/s.

The Am7960 encoder-decoder, from Advanced Micro Devices, performs tasks—including noise filtering, and high-impedance transformer interfacing—that previously required up to 15 discrete parts.

The chip has a serial transmission and reception line, in addition to modem control lines and a clock, that all simplify the connection to any USART. The chip can be set to work with a 32-bit preamble, so that it can neither send nor accept signals without it.

The transmission section of the chip accepts serial data and a clock from a USART. It combines them into a Manchester data stream, which flows into a transformer whose output directly drives the cable. An output driver generates a 2-V signal into a 37.5- Ω cable. An external pin controls the slew rate

of the data stream in order to minimize the associated rf emissions levels to conform with FCC regulations.

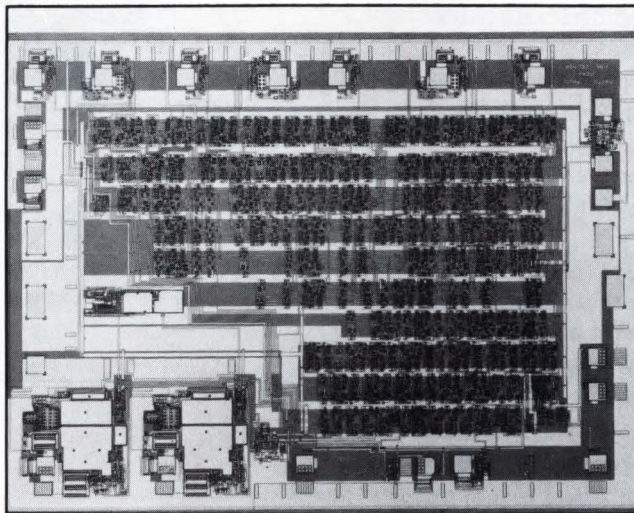
The receiving section has a built-in filter that ignores signals below 20 mV and only senses signal durations greater than 40 ns. It uses a phase-locked loop to convert the Manchester signal that gets through the filter into a clock and data stream that can be passed on to a USART. A major benefit of these features is noise immunity,

which makes the chip particularly well suited to industrial environments. It has a 32-dB dynamic range and can use signals as low as 35 mV.

The chip, which calls for a single 5-V power supply, is now being tested and will be available early next year. The price is \$18 in 100-piece quantities.

Advanced Micro Devices Inc., 901 Thompson Place, PO Box 3453, Sunnyvale, Calif. 91088; (408) 732-2400.

CIRCLE 307



Curtis Panasuk

Digital loop transceivers trim circuitry for a variety of links

A pair of master-slave digital loop transceiver chips replace transceiver boards, which require many random logic parts. The Motorola DLTs can be incorporated in voice and data PBXs, keypad systems, and limited-distance modems, and they operate over twisted-pair, coaxial, and fiber-optic cables.

Intended for short loop lengths (i.e., under 1 km in twisted-pair applications), the MC145418 master and the MC145419 slave run at 80 kbits/s in the half-duplex mode. They use a 256-kbit/s squared differential phase-shift-keying burst modulation technique for transmission, to eliminate the need for complex filters or echo-canceling circuits. In addition, the user can apply a variety of line driver interfaces, such as an inexpensive op amp, to suit twisted-pair systems.

Each DLT consists of a modulator, a demodulator, two intermediate data buffers, sequencing and control logic, and transmitter and receiver registers.

The master DLT, designed

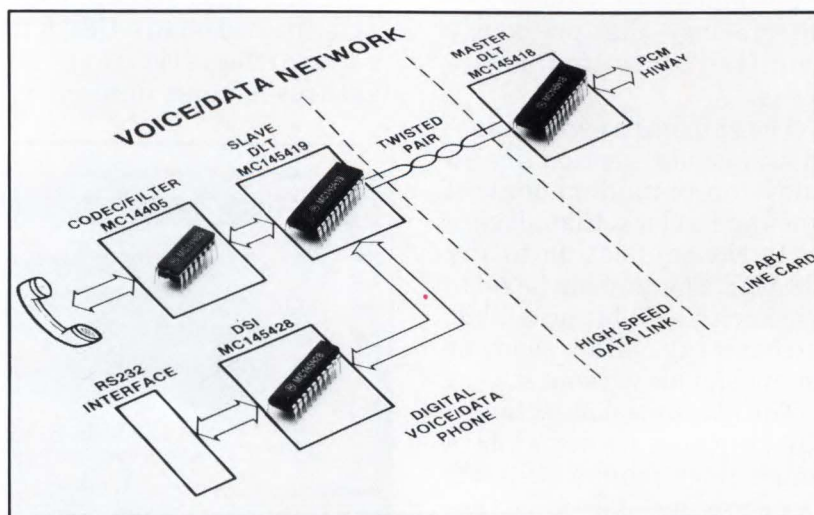
for use at the telephone line card, requires a standard 2.048-MHz clock. The slave DLT, designed for remote digital telephone set or data terminal, needs only an inexpensive 4.096-MHz crystal or external clock.

Each transceiver chip has a power-down input pin. (On the slave, the pin acts as a power-down output.) If no

bursts come from the master in 250 μ s, the slave powers down.

The chips operate over 5 to 8 V and dissipate a maximum of 80 mW. Both are available from stock in plastic packages. They cost \$9.89 apiece in production quantities.

Motorola Inc., 3501 Ed Bluestein Blvd., Austin, Texas 78721; (512) 928-6860.



Heather Bryce

COMMUNICATIONS

**Power amplifiers
conserve space**

Two power amplifiers—for use in the 40-to-450-MHz frequency range of the forward CATV branch—not only offer high voltage output ratings, but conserve space as well. Designated the BGD102 and BGD104, each device consists of two complete amplifier modules housed in a single SOT-115, the standard package that is currently used for individual amplifier module circuits.

At 450 MHz, the paralleled amplifiers have minimum voltage outputs of 65 dBmV with -60-dB intermodulation. Measured at 50 MHz, the power gain is 18.5 dB for the BGD102 and 20.0 dB for the BGD104.

Philips Elcoma, PO Box 523, 5600 AM Eindhoven, the Netherlands; (040) 757005; Telex: 51573.

Amperex Sales Corp., Providence Pike, Slatersville, RI 02876; (401) 762-9000.

CIRCLE 322

**Intelligent modem
secures data bases**

Compatible with Hayes 1200-, 300-, and 110-bit/s modems, the Cermetek security modem protects computer data bases against unauthorized remote access. The modem requires the caller to have a valid password and to be at a specified telephone number (stored in nonvolatile memory), which it automatically calls back before it allows access to the computer.

In addition to its password/call-back function, the modem employs a dial-out password to prevent unauthorized calls from the computer. It also generates an audit trail that lists both valid and invalid attempts to access the computer. To discourage tampering with the modem's circuitry, the case is sealed with special stickers.

Cermetek Microelectronics Inc., 1308 Borregas Ave., Sunnyvale, Calif. 94088; (408) 752-5000. \$695.

CIRCLE 323

**Unit links remote
peripherals to host**

The PE-2000 parallel interface extender offers a cost-effective way of locating computer peripherals, such as parallel printers, plotters, and terminals, in remote areas within local building structures without the use of costly modems. By installing one PE-2000 at the computer site and another at the remote site, equipment can be placed up to 2000 ft from the central computer. Parallel signals are converted into serial format at the local site and transmitted to the remote site at rates up to 40,000 char/s, where they are transformed back into parallel format. Optical couplers reduce electrical interference on the RS-422 differential transmission lines.

CBM Electronics Inc., 160 McCormick Ave., Costa Mesa, Calif. 92626; (714) 241-8194. \$195.

CIRCLE 324

**simulate
transducers**

± 4 to 20 mA, 10 to 50 mAdc

thermocouples± 0.1 μ V to 10.0 Vdc

Model CR-103J



For Quality Control Departments
Simulation and verification of Data Logging Systems and Process Control Systems in a production line environment.

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Accuracy: ± 0.003% of setting

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From ± 10 nanoamperes to ± 100 mAdc
Both ranges have 100 volts of compliance.
Accuracy: ± 0.005% of setting

NOTE: Specifications conservatively based on the Limit-of-Error ("worst case") method and are guaranteed for twelve months.

Price: Complete with certification traceable to N.B.S.: \$1995.
Option: Front panel protective cover: \$95.
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Prices and specifications subject to change.
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CIRCLE 144



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Tauber Electronics helped pioneer the Gates Value Distributor concept. From prototype to O.E.M. production, we deliver.

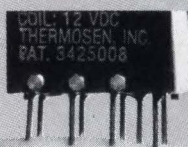


Energy Products

TAUBER ELECTRONICS INC.
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619/274-7242; No. CA 408/737-9408

CIRCLE 145

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Tiny package, tremendous performance: Low thermal EMF, low dynamic noise, low stable contact resistance, high speed, excellent isolation, high frequency characteristics and long life. The Thermosen Type D relay is the state-of-the-art for instrumentation and automatic test equipment.



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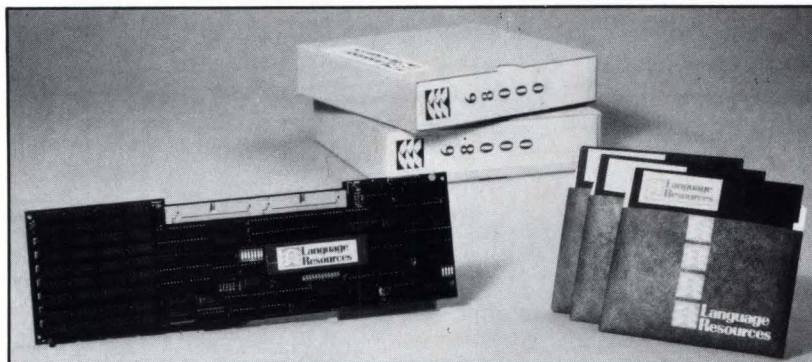
375 Fairfield Avenue, P.O. Box 1254
Stamford, CT 06904 (203) 324-6125

CIRCLE 146

NEW PRODUCTS

SOFTWARE

IBM PC XT, PC AT add-on develops 68000 code



Normally, an IBM PC XT or PC AT is not considered for developing 68000 software, but the picture changes with the addition of a cross-software development upgrade from Language Resources. The PC-68K consists of an IBM PC-compatible plug-in board, software on diskettes, and a user documentation package.

The board, which acts as an execution vehicle, contains a 68000 CPU, 256 kbytes of high-speed RAM, and a memory management subsystem. A full-length expansion slot in either the PC XT or PC AT is required to accommodate the board.

The software development tools consist of a 68000 macro-assembler, a linker, a locator, and a symbolic debugger. Pascal and C compilers are available, as are emulation and host communication utilities.

Both the Pascal and C compilers translate C, Pascal, and

macroassembler modules, allowing them to be easily interfaced. The Pascal compiler implements the ANSI and IEEE standard and also benefits from some useful extensions. The C compiler is the Mark Williams version.

With the emulator communication utility, several popular 68000 emulators may be connected to the PC XT or PC AT for hardware-software integration. The host communication utility allows binary and text files to be transferred between the PC XT or PC AT and an IBM VM-CMS or DEC VAX/VMS system running Language Resources' XDX-68 cross-software.

The basic PC-68K package is priced at \$2995. The C and Pascal compilers are \$895 each, and the host and emulation communication utilities are \$495 each. Delivery is in 30 days after receipt of order.

Language Resources Inc., 4885 Riverbend Road, Boulder, Colo. 80301; (303) 449-8087.

Bob Milne

CIRCLE 315

SOFTWARE

Chip design software is fully integrated, cuts turnaround time

The latest versions of the LDS logic design software provide one of the few fully integrated sets of routines that permit a designer to do as little as schematic capture or bring the design through simulation, and test pattern generation. The software, major upgrades of LSI Logic's LDS II package, offers designers a faster turnaround time thanks to the speed and integrated nature of the software.

LDS III consists of programs for schematic capture, logic verification, delay computation, logic simulation, test pattern generation, and detectable fault simulation. One key part, the simulator (LSIM), uses different models depending on the level of system used. It operates at twice the speed of the popular TEGAS routine.

An optional program called MSIM permits independently developed chip descriptions to be combined for multichip system simulations. (When it is added to LSIM, the package is called LDS IV.) The user can even specify the interchip loading capacitance and ex-

tract test data from the system simulation.

To speed simulations, there is an optional interface to Zycad's LE1002 hardware accelerator via a routine called ZSIM (with ZSIM added to LDS IV, the package becomes LDS V). The accelerator provides a hundredfold increase in speed over the use of LSIM.

Design verification routines perform full cell interconnection checks, provide design statistics (gate and I/O pad utilization), and construct functional files containing a description of the data flow on the chip. The test extraction portion pulls vectors from the simulation and automatically selects dc tests based on buffer types the user selected.

Fault grading is the last option. When added to the LDS

V grouping, the package becomes LDS VI.

The software accommodates all of the company's gate array families. Not all packages can run on the small systems, though (see the table). However, the software was designed to provide a simple migration path.

For a VAX-11/750 system, the LDS III package costs \$80,000 to \$100,000 and includes one cell library. Additional libraries can be added at a cost of \$30,000 to \$50,000. Enhancements can be added for \$40,000 to \$50,000 each. For an IBM 4341 mainframe, an all-inclusive package (LDS VI) would cost over \$250,000.

LSI Logic Corp., 1551 McCarthy Blvd., Milpitas, Calif. 95035; Keith Lobo, (408) 263-9494.

CIRCLE 305

System type	Schematic capture	Verification	Delay calculation	Simulation	Test generation	Detectable fault simulation	Fault grading
Personal computer	Yes	No	No	No	No	No	No
Workstation	Yes	Yes	Yes	Yes*	No	No	No
Single-user Unix system	Yes	Yes	Yes	Yes†	Yes	Yes	No
VAX-11/780	Yes	Yes	Yes	Yes†	Yes	Yes	Yes
IBM 3081	Yes	Yes	Yes	Yes‡	Yes	Yes	Yes

*Relatively simple logic model †Moderately complex logic model ‡Complex logic model

Dave Bursky

SOFTWARE

Multitasking, multi-user PDOS suits 68000

A multi-user, multitasking version of the PDOS real-time operating system consisting of a

kernel with file management, user monitor, and floating-point modules runs on 68000 family processors. The

2-kbyte kernel of Force Computers' SYS68K/PDOS synchronizes and controls real-time tasks with semaphores and events.

The system requires only 8 kbytes of memory, with an additional 4 kbytes for system buffers and stacks. Developed by Eyring Research (Provo, Utah) and widely adopted for VME systems, PDOS effectively accesses up to a 32-bit address space.

The operating system is written in assembly language and has a Basic interpreter with enhancements such as program debugging. Support utilities include virtual screen editors, a 68000 macro-assembler, and a linker.

The file management module runs files with sequential, random, and shared access using round-robin or priority scheduling. Program security is ensured by task memory-map control.

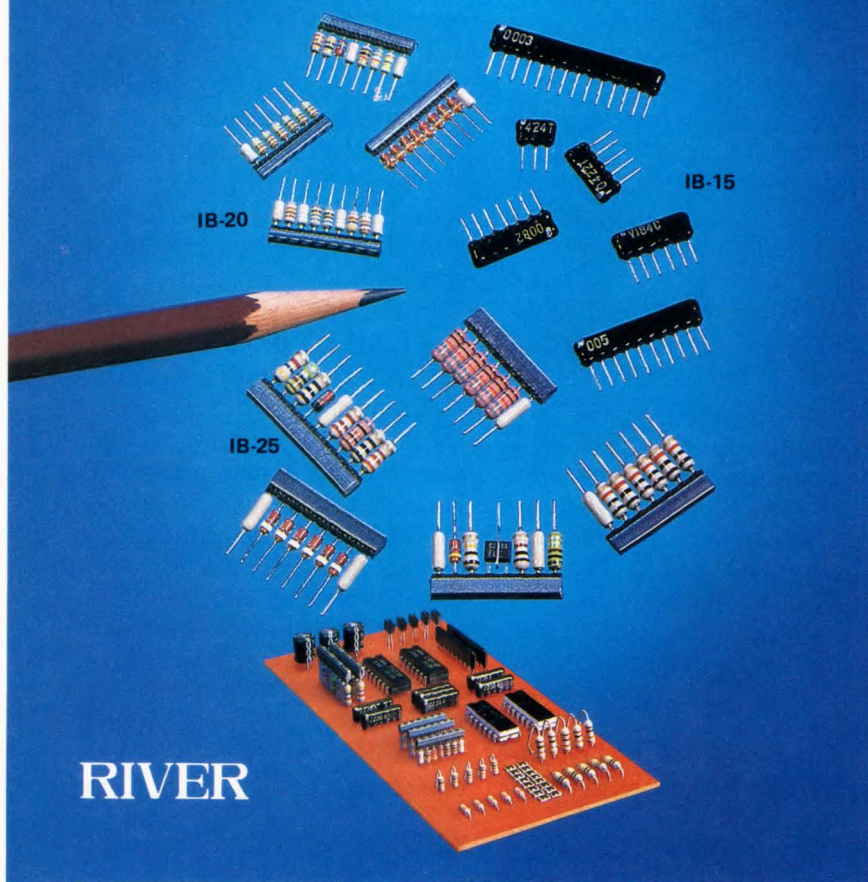
A Pascal compiler is available, and Fortran 77 and C compilers will be ready shortly. The operating system comes on a pair of 5¼-in. floppy disks, plus two bootstrap EPROMs. It costs \$1150; the Basic and Pascal options are \$350 and \$550, respectively.

Force Computers Inc. 2041 Mission College Blvd., Santa Clara, Calif. 95054; (408) 988-8686; Telex: 17265

Force Computers GmbH, Daimlerstrasse 9, 8012 Otto-brunn b. Munich, West Germany; (089) 6092033; Telex: 524 190 forc-d.

CIRCLE 301

SPACE SAVINGS OF 1/5 NEW APPROACH TO CIRCUIT BLOCK ASSEMBLY



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14-40, Nishi Shinjuku 4-chome, Shinjuku-ku, Tokyo, Japan
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SOFTWARE

Subroutines ease numerical analysis

The Fortran Scientific Subroutine Library, by Peerless Engineering Service, consists of 114 pretested and precompiled subroutines that save programming time, solve practical problems, and increase reliability of software design. The subroutines cover the common formulas for general statistics, regressions, matrices, polynomials, integrations, fast Fourier Transform, roots of biquadratic equations, cross tabulations, and more. The library comes complete with three diskettes containing the source code, the subroutine library, and the test programs, plus over 400 pages of instructions and reference materials.

John Wiley & Sons Inc., 605 3rd Ave., New York, N.Y. 10158; (212) 850-6000. \$175.

CIRCLE 325

Utility package links iRMX 86 and NDS-II

A software utility package acts as an interface between systems based on the iRMX 86 operating system and the NDS-II multi-user microprocessor development system to give users the benefits of a networked environment. Called the iRMX-NDS-II link, the product cuts development engineering costs by allowing individual iRMX target systems tied to the NDS-II network to share mass storage, line printers, and archival facilities. The iRMX-NDS-II link uses a

high-speed Ethernet coaxial cable to transfer data at 10 Mbits/s—compared with the 9.6-kbit/s rate typical of conventional serial links. The software license is priced at \$2500 for eight copies, plus

\$2000 for the Ethernet controller handset.

Intel Corp., Literature Department I-12, 3065 Bowers Ave., Santa Clara, Calif. 95051; (408) 496-9484.

CIRCLE 326

McCoy Reliability is out of this World

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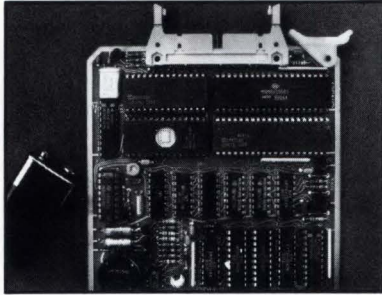
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COMPUTER BOARDS

Computer board slashes power to as little as 1 mW



An 80C88-based single-board computer draws only 1 mW when stopped and 3 mW when waiting, making it suitable for applications that combine intermittent duty cycles with a lack of ample power. This exceptionally low power consumption is achieved, in part, by halting the system's oscillator in either mode and also allowing the voltage to drop to 3 V while the computer is stopped.

Capable of operating as a CPU as well, the CPU-8088 from Onset Computer employs a phase-shift oscillator rather than the conventional crystal-controlled oscillator. As a result, restarting takes only one cycle and recovery from the stop mode requires about 10 ms, the time needed for the board to return to 5 V.

The board holds an 82C52 UART (universal asynchronous receiver-transmitter). That CMOS part is generally programmed to turn itself off while waiting; otherwise it would boost power consumption to approximately 20 mW.

The board leaves the waiting mode in response to a UART interrupt. Alternatively, it can be reactivated by an interrupt signal from an on-board real-time clock, from an external reset signal, or by asserting a wakeup line.

A built-in switching voltage regulator allows the board to use a wide range of supply voltages while keeping overall power consumption relatively constant. When fully operational and executing code, the board draws approximately 20 mA from a 12-V power supply.

As part of a larger system, the computer can access up to 512 kbytes of off-board memory without resorting to bank switching. On power-up, a 27C64 (64-kbit) EPROM at the top of the memory is addressed. (Larger EPROMs can be readily substituted when they become available.)

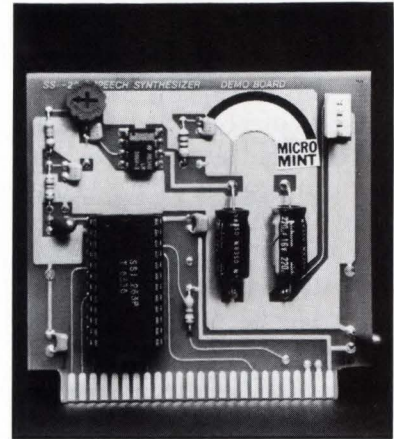
The 81C55 port chip provides 22 programmable I/O lines. The system's C-44 bus, especially well suited to low-power applications, allows for memory expansion up to 192 kbytes using currently available cards.

The CPU-8088 is priced at \$550 for a single unit. Delivery is within six weeks.

Onset Computer Corp., 199 Main St., PO Box 1016, North Falmouth, Mass. 02556; Lon Hocker, (617) 563-2267.

CIRCLE 310

Speech synthesis board plugs into Apple II



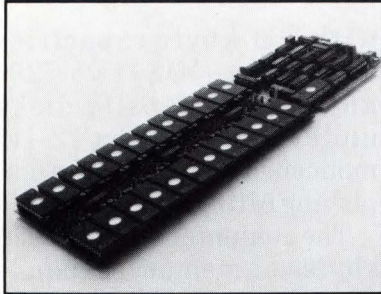
Sweet Talker II, a third-generation speech synthesizer for Apple II+ and IIe computers, is based on the SSI 263 speech synthesis chip from Silicon Systems Inc. At data rates of no more than 400 bits/s (and as low as 50 to 70 bits/s), the Sweet Talker II permits control of intonation, inflection, and filtration. It features 256 phoneme equivalents, 4096 pitch variations, and an on-board 1-W amplifier with volume control. Phoneme values are dynamically set on five 8-bit internal registers.

Sweet Talker II also offers 16 speed settings and amplitude levels, as well as 255 settings of the vocal-tract filter's frequency response. The board's analog output can be used to produce music, sound effects, and continuous speech of unlimited vocabulary. It operates from +5- and +12-V supplies and is a mere 3 by 3¼ in.

Micromint Inc., 561 Willow Ave., Cedarhurst, N.Y. 11516; (516) 374-6793. \$104.

CIRCLE 429

COMPUTER BOARDS

IBM PC board has nonvolatile memory

SoliDisk, a mass-storage system for the IBM PC, provides up to 384 kbytes of nonvolatile storage utilizing 64- and 128-kbyte EPROMs. Its on-board EPROM programmer can copy a double-sided diskette in less than 45 minutes. What's more, an optional UV-eraser allows the user to erase the entire board in less than one hour.

Once programmed, SoliDisk permits high-speed data access in 2 ms—compared with 360 ms for floppy disks, 160 ms for hard disks, and 100 ms for bubble memories. SoliDisk is available in single-, double-, and quad-density configurations, which cost \$650, \$1250, and \$2500, respectively.

Fastore, 200 Danbury Road, Wilton, Conn. 06897; (203) 834-1975.

CIRCLE 327

SMD disk controller works with VMEbus

One of the first SMD disk controllers to be manufactured in the U.S. for the European standard VMEbus supports both 32-bit data transfers and addressing. The single-board controller and

formatter, designated the V/SMD 3200, implements a virtual buffering architecture that controls 12 kbytes of buffer space. The design speeds up access and data transfer time and reduces actual disk activity under disk-intensive operating systems, such as Unix or RMX/86.

The 68000-based controller supports data rates of up to 24 Mbits/s and features on-board error correction with 32-bit ECC. A read operation of one track never takes more than one complete revolution of the disk, reducing by one-third the disk transfer time after the drive completes the seek.

Interphase Corp., 2925 Merrell Road, Dallas, Texas 75229; (214) 350-9000. \$2750.

CIRCLE 328

Hard-disk controller offers data encryption

The DC-6 series of hard-disk controllers for the IBM PC features a data encryption facility based on the National Bureau of Standards Data Encryption method. Totally encoded confidential files in shared-user or secure systems may be created through the board's encrypt and decrypt utilities. The controller also features configuration flexibility, provided through a proprietary self-adjusting technique that stores drive configuration parameters and media information on private disk sectors. Once formatted, the drive can be used with any operating system. It is compatible with

8- and 5-1/4-in. disk drives, storing from 5 to 150 Mbytes per drive. Multiple-burst error correction is implemented through hardware and microcode, enabling error-handling that is independent of the operating system.

Sigen Corp., 1800 Wyatt Drive, Suite 7, Santa Clara, Calif. 95054; (408) 988-2527. \$495 (with encryption option); stock to two weeks.

CIRCLE 329

Processor board extends IBM PC

Compatible with the IBM PC and most PC look-alikes, the PC-Slave/16 is a high-speed single-board processor. By plugging the board into the PC's bus, a dumb terminal can be added to create a two-user configuration. For installations supporting many users, the PC-Exbus expansion chassis can accommodate up to 12 PC-Slave/16s. Furthermore, the PC-Slave/16 enables users to be added at a cost of only \$1650/user, including the terminal.

The processor board contains an 8-MHz 8088 CPU, 256 kbytes of bank-selectable dynamic RAM, and two serial ports. The RTNX Executive software permits the PC-Slave/16 to run PC-DOS, MS-DOS, or CP/M. RTNX also provides file/record locking with controls for file access management.

Advanced Digital Corp., 5432 Production Drive, Huntington Beach, Calif. 92649; (714) 891-4004. \$1095.

CIRCLE 330

COMPUTER SYSTEMS

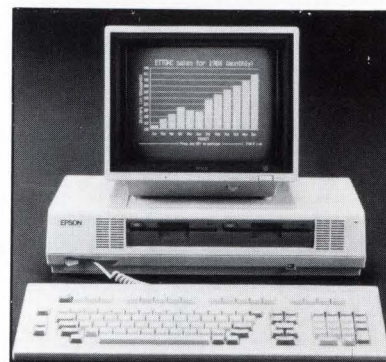
PC runs under MS-DOS and CP/M

The QX-16 personal computer from Epson America contains a 16-bit 8088 processor running

under MS-DOS and an 8-bit Z80 processor running under CP/M. It comes with two 5¼-in. dual-density floppy disks

with 360-kbyte capacities under MS-DOS, two 720-kbyte quad-density disks under CP/M, and a 12-in. monochromatic monitor displaying 610 by 100 pixels.

The computer contains 256 kbytes of memory, expand-



able to 512 kbytes. It also features three IBM PC-compatible expansion slots, an RS-232-C serial port, and a Centronics parallel printer interface. Its integrated software package, VALDOCS 2, includes a file manager and word-processing, spreadsheet, graphics, and electronic mail.

The keyboard is compatible with that of an IBM Selectric typewriter. Its functions may be redefined under software control.

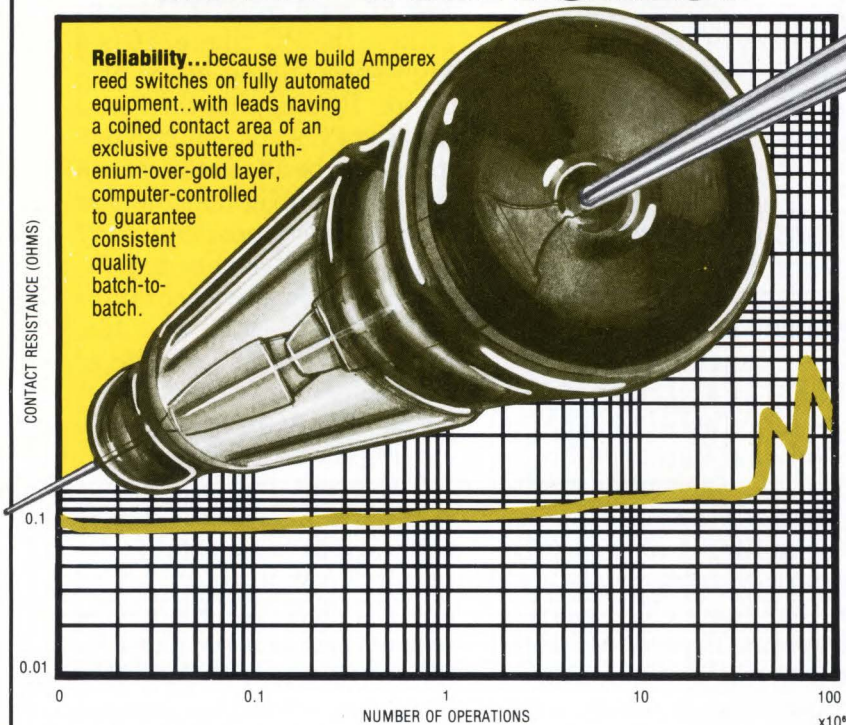
The unit comes with a one-year warranty. Priced at \$3000, it is available from stock. Future options will include a color monitor, 10- to 20-Mbyte hard disks, and a modem.

Epson America Inc., Computer Products Division, 2780 Lomita Blvd., Torrance, Calif. 90505; (213) 539-9140.

CIRCLE 312

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COMPUTER SYSTEMS**Micro offers 100% IBM PC-compatibility**

The Micromix 16, a true 16-bit PC-DOS microcomputer, is fully compatible with IBM PC peripherals, software, and I/O expansion boards. It is designed to upgrade nonintelligent business machines, such as display terminals and electronic typewriters, to provide them with advanced communications and local intelligence.

The basic Micromix system comprises an 8088-based CPU, 256 kbytes of RAM, a 360-kbyte 5¼-in. disk drive, a parallel printer port, an RS-232-C serial port, a universal terminal controller (UTC), and four I/O expansion slots. The UTC has a serial ASCII-terminal port and optional coax-terminal and network interfaces, all of which are switch-selectable.

Trios Micro Systems Inc., 147 Beacon St., San Francisco, Calif. 94080; (415) 583-7733. From \$2150; 30 days.

CIRCLE 331

PC-based workstation handles design tasks

A personal-computer based workstation provides 90% of the functions needed for computer-aided design at 20% of the cost of large-scale design systems. At \$15,400, the fully configured Electronic Design Micro Workstation includes an IBM PC-XT-compatible computer; software for schematic entry; documentation, project manage-

ment, and netlist extraction to several design software packages; a printer/plotter; a 10-Mbyte Winchester drive; a 360-kbyte floppy-disk drive; and a mouse.

The workstation offers multiple split-screen windows and a user-definable grid, which helps visualize the scale and space between components. Set commands facilitate the storing and editing of schematics, while automatic arc and circle generation improve the quality of the design. Further extending the workstation's usefulness is the SALT program (\$3500), which performs logic simulation, timing verification, and stability analyses.

Control Data Corp., Information Systems Design, 2500 Mission College Blvd., Santa Clara, Calif. 95054; (800) 253-4004 or (612) 921-4400.

CIRCLE 332

Fault-tolerant system is cost-effective

A fault-tolerant process-control system has fewer components than comparable systems, resulting in reduced costs, as well as faster processing speeds. The base price of the CS330 control system is approximately \$40,000—about \$30,000 less than the base price of the earlier CS300.

The system comprises a motherboard, three control computer boards, a four-port serial I/O board, up to 14 process I/O boards, and a triple power supply unit. The three computers perform all con-

trol functions simultaneously. All inputs, computations, and control outputs are "voted" on by the three systems before being sent to the process. Even transient errors are detected and corrected by the two-out-of-three voting process.

August Systems Inc., 18277 SW Boones Ferry Road, Tigard, Ore. 97223; (503) 684-3550.

CIRCLE 333

Graphics workstations tout 32-bit processing

The 6000 family of NS32000-based graphics workstations can be configured for a variety of applications, ranging from a satellite unit for instrument and process control to a powerful CAE workstation that supports multiple CPUs and users. Comprised of two distinct but software-compatible product groups—the 6100 and 6200 series—the workstations feature 32-bit processing power.

The 6100 series supports a 15-in. monochrome display with a 640-by-480-pixel resolution or a 13-in. 16-color (from a palette of 64) display with the same resolution. The 6200 series offers a 19-in. monochrome display, as well as a 16- or 256-color (from a palette of 16 million) display. The resolution for either one of the 6200's displays is 1024 by 768 pixels.

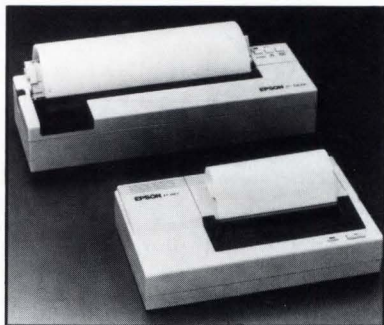
Tektronix Inc., PO Box 1700, Beaverton, Ore. 97075; (503) 644-0161.

CIRCLE 334

COMPUTER PERIPHERALS

Thermal miniprinter uses plain paper

A portable, battery-run thermal-transfer printer produces letter-quality copy on normal or thermal paper. Using a 24-pin print head and selling for just \$130 in OEM quantities, the P80 from Epson



America is only 297 by 107 by 62.2 mm and weighs 2.5 lb.

Powered by built-in AA-type nickel-cadmium batteries, it yields about 25,000 characters per battery charge and consumes an average of 3 W per print operation. The estimated head life is 20 million characters.

The printer produces 40 characters unidirectionally within an 80-column format using bit-addressable graphics at 180 by 180 dots/in. It is configured for the standard 96 ASCII characters and 31 international and 32 graphics characters. It has a standard RS-232-C serial interface that operates at 75 to 9600 bauds and terminates at a six-pin DIN connector. A 240-byte input buffer is included.

The unit can be customized to meet a variety of OEM requirements. The printer is

available without the case for \$30 off the OEM price and can also be purchased with a 6-V adapter. Units are in stock.

Epson America Inc., OEM Products Division, 23600 Telo Ave. Torrance, Calif. 90505; (213) 534-4500.

CIRCLE 302

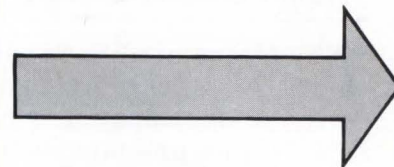
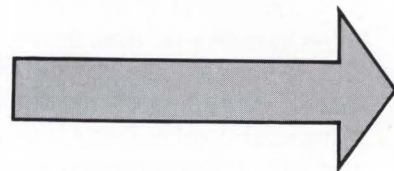
VAX-11/780 add-on
uses 64k RAM chips

Equivalent to DEC's MS780-E, a memory system utilizing 64k RAM devices can be used as a field replacement for the original 16k memory system (the MS780-C) or as an add-on upgrade for any VAX-11/780. When installed as an add-on, the memory is configured in a CPU expander cabinet, which can also house two slot assemblies for peripheral adapters.

The system consists of a 20-slot backplane, an interleaved memory control set, a minimum of 4 Mbytes of memory, a power supply, and related hardware. Using VX-2MB-780 memory cards, the 11/780 can be configured with up to 32 Mbytes of memory per backplane. The memory system installed in the CPU cabinet with 4 Mbytes of storage lists for less than \$27,000, 30% less than DEC's comparable upgrade.

EMC Corp., 12 Mercer Road, Natick, Mass. 01760; (800) 222-3622 or (617) 655-6600. Stock to two weeks.

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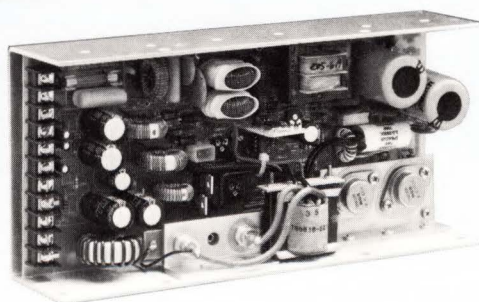
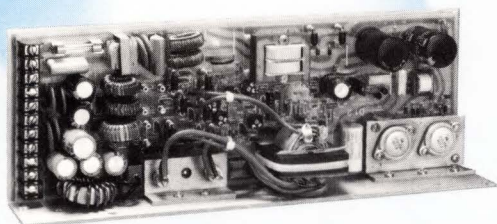
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Deltron Cool 1 & Cool 2 Series Voltage/Current Ratings

QUAD OUTPUT COOL 1 SERIES

Output	#1	#2	#3	#4	Max.	Output
Current	15A	3A	2A	2A	Watts	Current
Q130AXX	+5V	+12V	-12V	- 5V	130W	F501AX
Q130BXX	+5V	+12V	-12V	+24V		F501BX
Q130CXX	+5V	+15V	-15V	- 5V		Output
Q130DXX	+5V	+15V	-15V	+24V		Current
Q130EXX	+5V	+12V	-12V	+12V		F502AX
Current	20A	3A	2A	2A	Max.	F502BX
Q150AXX	+5V	+12V	-12V	- 5V	Watts	Output
Q150BXX	+5V	+12V	-12V	+24V	150W	Current
Q150CXX	+5V	+15V	-15V	- 5V		F503BX
Q150DXX	+5V	+15V	-15V	+24V		Output
Q150EXX	+5V	+12V	-12V	+12V		Current
Current	20A	4A	4A	4A		Max.
Q170AXX	+5V	+12V	-12V	- 5V	Watts	F1000B
Q170BXX	+5V	+12V	-12V	+24V	170W	F1000C
Q170CXX	+5V	+15V	-15V	- 5V		F1000D
Q170DXX	+5V	+15V	-15V	+24V		F1000E
Q170EXX	+5V	+12V	-12V	+12V		Output
Current	25A	4A	4A	4A		Max.
Q200AXX	+5V	+12V	-12V	- 5V	Watts	F1001A
Q200BXX	+5V	+12V	-12V	+24V	200W	F1001B
Q200CXX	+5V	+15V	-15V	- 5V		Output
Q200DXX	+5V	+15V	-15V	+24V		Current
Q200EXX	+5V	+12V	-12V	+12V		F1002A
Current	30A	4A	4A	4A		Max.
Q250AXX	+5V	+12V	-12V	- 5V	Watts	Output
Q250BXX	+5V	+12V	-12V	+24V	250W	Current
Q250CXX	+5V	+15V	-15V	- 5V		F1003A
Q250DXX	+5V	+15V	-15V	+24V		
Q250EXX	+5V	+12V	-12V	+12V		
Current	40A	6A	6A	6A		Max.
Q400AXX	+5V	+12V	-12V	- 5V	Watts	
Q400BXX	+5V	+12V	-12V	+24V	400W	
Q400CXX	+5V	+15V	-15V	- 5V		
Q400DXX	+5V	+15V	-15V	+24V		
Q400EXX	+5V	+12V	-12V	+12V		
Output	#1	#2	#3	#4	#4	Max.
Voltage	+5V	+12V	-12V	- 5V	+24V	Watts
E200A	25A/35 pk.	4A/8 pk.	2A	2A		200W
E200B	25A/35 pk.	3A	2A		2A/4 pk.	

Note: E Series units are standard with two post regulators and FCC/VDE EMI filter. No other options are applicable. Outputs #2 through #4, without peak ratings are post regulated.

SINGLE OUTPUT COOL 1 SERIES

Model	Volts	Amps	Nom. Watts
Q120A	5V	25A	120W
Q120B	12V	10A	
Q120C	15V	8A	
Q120D	24V	5A	
Q180A	5V	36A	180W
Q180B	12V	15A	
Q180C	15V	12A	
Q180D	24V	7.5A	
Q270A	5V	54A	270W
Q270B	12V	22A	
Q270C	15V	18A	
Q270D	24V	11A	
Q360A	5V	72A	360W
Q360B	12V	30A	
Q360C	15V	24A	
Q360D	24V	15A	

4 TO 7 OUTPUT COOL 2 SERIES

Output	#1	#2	#3	#4	Max. Watts
Current	50A	6A	6A	6A	
F500AXX	+5V	+12V	-12V	- 5V	500W
F500BXX	+5V	+12V	-12V	+24V	
F500CXX	+5V	+15V	-15V	- 5V	
F500DXX	+5V	+15V	-15V	+24V	
F500EXX	+5V	+12V	-12V	+12V	

COOL 2 SERIES CONTINUED

Output	#1	#2	#3	#4	#5	Max.		
Current	50A	6A	6A	3A	3A	Watts		
F501AXX	+5V	+12V	-12V	- 5V	+24V	500W		
F501BXX	+5V	+15V	-15V	- 5V	+24V			
Output	#1	#2	#3	#4	#5	#6	Max.	
Current	50A	3A	3A	3A	3A	6A	Watts	
F502AXX	+5V	+12V	-12V	+15V	-15V	- 5V	500W	
F502BXX	+5V	+12V	-12V	+15V	-15V	+24V		
Output	#1	#2	#3	#4	#5	#6	#7	Max.
Current	50A	3A	3A	3A	3A	3A	3A	Watts
F503BXX	+5V	+12V	-12V	+15V	-15V	- 5V	+24V	500W
Output	#1	#2	#3	#4	Max.			
Current	100A	12A	12A	12A	Watts			
F1000AXX	+5V	+12V	-12V	- 5V	1000W			
F1000BXX	+5V	+12V	-12V	+24V				
F1000CXX	+5V	+15V	-15V	- 5V				
F1000DXX	+5V	+15V	-15V	+24V				
F1000EXX	+5V	+12V	-12V	+12V				
Output	#1	#2	#3	#4	#5	Max.		
Current	100A	12A	12A	6A	6A	Watts		
F1001AXX	+5V	+12V	-12V	- 5V	+24V	1000W		
F1001BXX	+5V	+15V	-15V	- 5V	+24V			
Output	#1	#2	#3	#4	#5	#6	Max.	
Current	100A	6A	6A	6A	6A	12A	Watts	
F1002AXX	+5V	+12V	-12V	+15V	-15V	- 5V	1000W	
F1002BXX	+5V	+12V	-12V	+15V	-15V	+24V		
Output	#1	#2	#3	#4	#5	#6	#7	Max.
Current	100A	6A	6A	6A	6A	6A	6A	Watts
F1003AXX	+5V	+12V	-12V	+15V	-15V	- 5V	+24V	1000W

Cool 1 & Cool 2 Series Options

Differential Mode Filters

Optional Filters to meet FCC 20780 Class A and VDE 0871 Class A & C conducted EMI specs.

Power Fail

Optional precision line monitor provides a TTL compatible logic low output if line voltage drops below rated value.

Temperature Protector

Optional thermal shutdown. Circuit cuts off supply in case of excess local temperature and automatically resets if excess temperature abates.

Cover

Optional cover for mechanical security and to meet FCC 20780 and VDE 0871 radiated EMI specs.

Outputs 2 & 3 Post Regulated, Output 4 Autobleed

Post regulators supplied on outputs #2 & #3 with specifications as detailed above, autobleed on output #4 keeps voltage rise at no load to less than 10%.

Outputs 2, 3 & 4 Post Regulated

All auxiliary outputs post regulated with specifications as detailed above.

Custom Options

1. Additional outputs either regulated or quasi regulated.
2. Custom form factors.

See next page for Option Code, notes.

Deltron Cool 1 & Cool 2 Series Specifications

Outputs:

See table of models for Cool 1 and Cool 2 units.

Input:

90-132 or 180-264 VAC, 47-440 Hz. Limit to 63 Hz. for Cool 2 units.

Input Surge:

17A peak from cold start. 34A for Series 250, 270, 360 and 400. Less than 4 times the steady state peak current from cold start for Cool 2 units.

Line Regulation:

±0.2% max. for input change from nominal to min. and max. rated values, when operated at 100% rated power with at least 20% max. rated load on all outputs. ±0.05% for post regulated auxiliaries.

Load Regulation:

+ 5V Main	±0.2%	±0.2% for
- 5V aux	±4%	post regulated
±12V aux	±2%	auxiliaries and
±15V aux	±2%	single output units.
+24V aux	±1.5%	

Test output set at 60% of rated load with a change of ±40% of rated load. Main +5V output requires a minimum load of 10% of rated value. All other outputs set at 20% max. rated load. Autobleed option removes need for 20% min. load on auxiliaries and keeps no load voltage rise to less than 10%.

Centering:

±5% with all outputs at 50% rated load and main +5V output set at 5.0V.
Not applicable to post regulated auxiliaries or single output units.

Cross Regulation:

Effect on Auxiliaries of Change in Main Output

130, 170, 500 WATT MODELS	150, 200, 250, 400, 1000 WATT MODELS
-5V aux	±2.5% ±0.1% for
±12V aux	±2.5% post regulated
±15V aux	±2.5% auxiliaries.
+24V aux	±2.5%

Measured output set at 20% rated load and main +5V output set at 75% of rated load with a change of ±25% of rated load. All other outputs set at 20% of max. rated load. With option 08, cross regulation is reduced to 1/5 the tabulated values on 500 and 1000 watt models. Not applicable to single output units.

Effect on Auxiliaries of Other Auxiliaries

All auxiliary outputs - ±0.5%

Measured output set at 20% rated load and other auxiliary outputs set at 75% of rated load with a change of ±25% of rated load.

Not Applicable to post regulated auxiliaries or single output units.

Ripple & Noise:

2% pk-pk
40 mv rms

Holdup Time:

20 milliseconds after loss of nominal AC power.

Efficiency:

75% min. (units with quasi-regulated auxiliaries or single output.)

Adjustability:

±10% trim. Auxiliaries track main output.
±3% trim on post regulated auxiliaries.

OVP:

Standard on main output.

Operating Temperature:

0°C-70°C. Full rated to 50°C. Derate linearly to 50% at 70°C. Cool 1 Series can be rated at 100% at 70°C with 85 CFM directly over unit.

Overload:

All outputs short circuit protected by current foldback with automatic recovery after removal of fault current. Post regulated auxiliaries have individual current foldback protection.

Reverse Voltage Protection:

All outputs are protected up to load ratings.

Temperature Coefficient:

Main +5V - ±0.02%/°C typ.
All auxiliary outputs - ±0.05%/°C. typ.
Post regulated auxiliaries - ±0.02%/°C typ.

Input Filtering:

Common mode standard. Differential mode optional. With differential mode option units meet FCC 20780 Class A and VDE 0871 Class A & C.

Safety:

Units designed to meet VDE 0804 and VDE 0806 Class 1 leakage and isolation, UL 478, CSA 22.2, IEC 435 and IEC 380 Class 1.

AC Undervoltage:

Units internally protected against damage for AC undervoltage operation.

Soft Start:

Units have soft start feature to protect critical semiconductors.

Inhibit:

TTL compatible field selectable logic high or logic low inhibit input.

Dynamic Response:

Peak transient less than ±2% or 200 mv for a step change of ±25% of rated load from a set point of 75% of rated load.

Recovery Time:

Less than 400 microsec on main output for recovery to within 0.5% of final value. Less than 50 microsec on post regulated auxiliaries.

Option Code

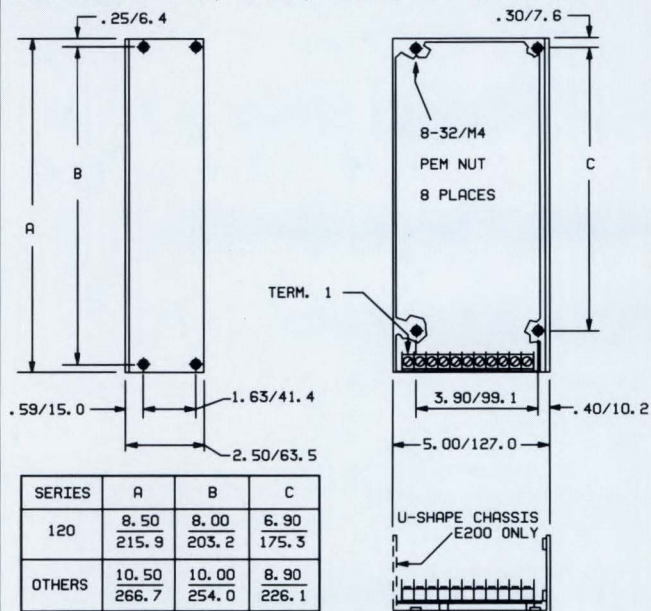
00	None
01	FCC/VDE EMI Filter
02	Line Monitor
04	Thermal Shutdown
08	Cover - Cool 1's /Cross Reg. Minimizer - Cool 2's
16	Last Auxiliary Autobleed. Others Post Reg.
32	All Auxiliaries Post Reg.

Notes:

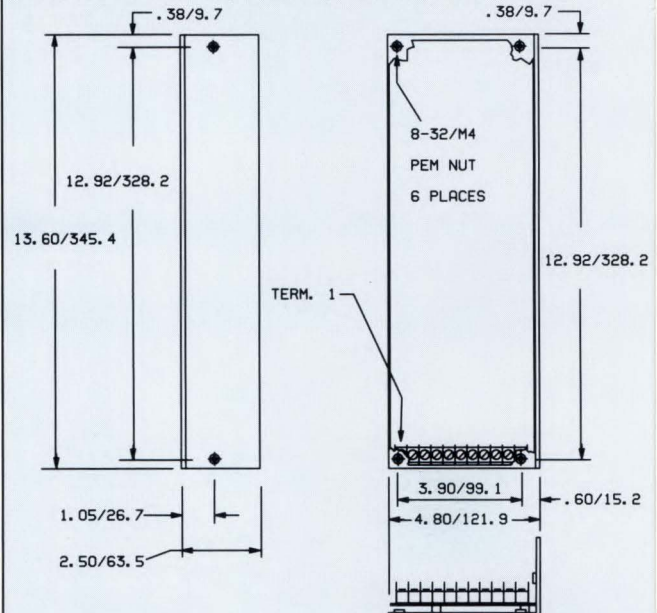
- XX in model numbers are for option codes. Insert sum of desired option codes, e.g. 07 is for Thermal Shutdown, Line Monitor and FCC/VDE EMI filter.
- Option 32 not available for models F1000BXX, F1000DXX, F1002BXX.
- Any polarities can be reversed except the main +5V output on custom order.
- Derate max. power rating by 12% when option 16 or 32 is specified.
- Cool 2 units are furnished for 90-132 VAC input. For 180-264 VAC input add suffix W to model number.
- Watts are maximum allowable total power ratings. On some models current ratings limit before power rating.

Cool 1 & Cool 2 Series Dimensions (inches/mm)

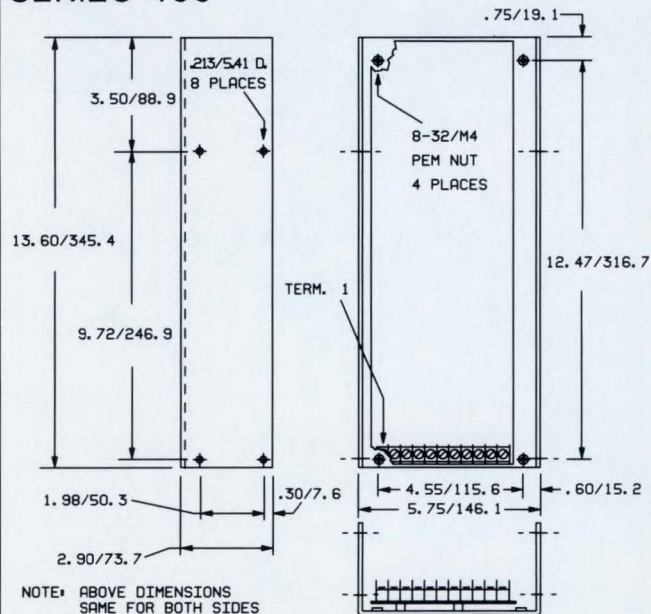
SERIES 120, 130, 150, 180, E200



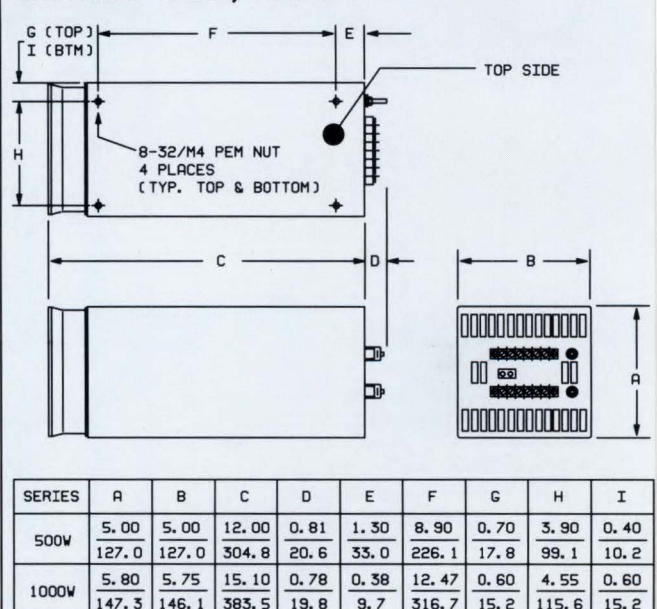
SERIES 170, 200, 250, 270, 360



SERIES 400



SERIES 500, 1000



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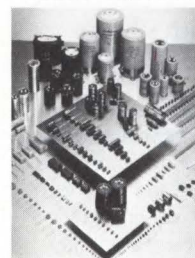
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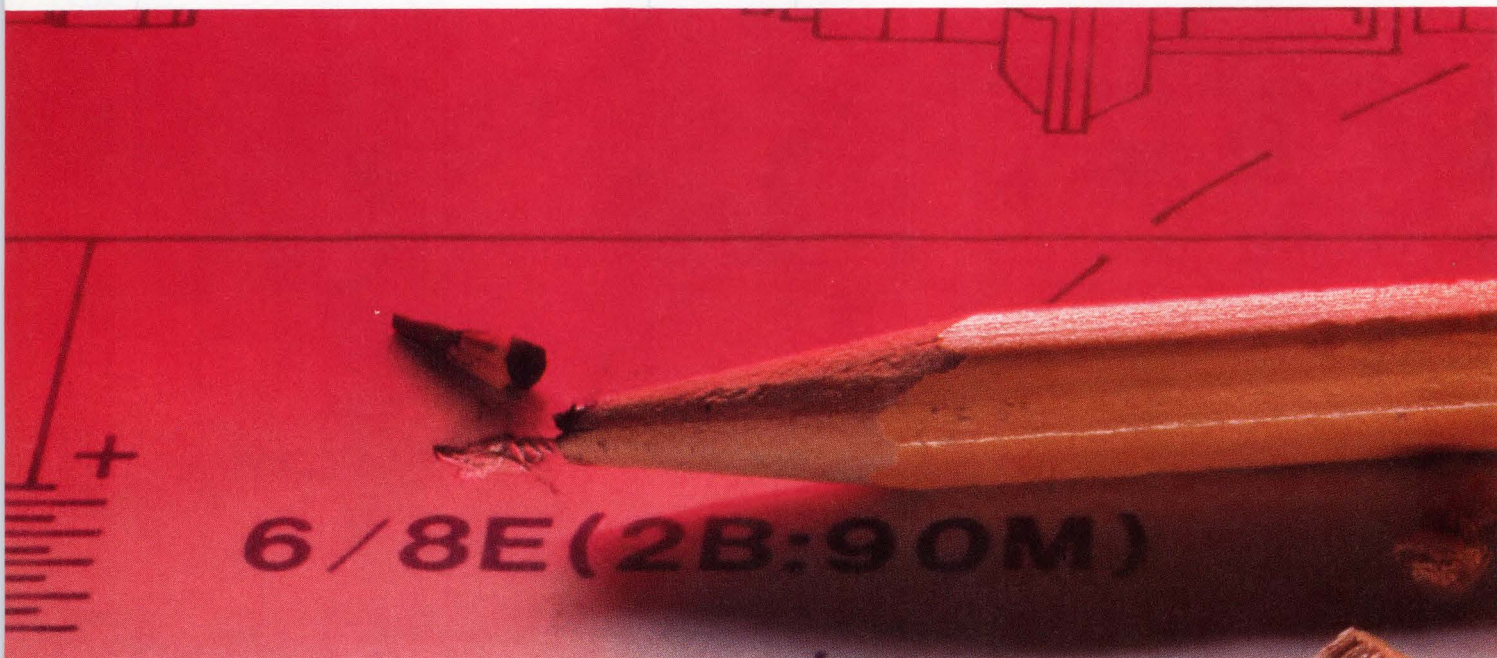
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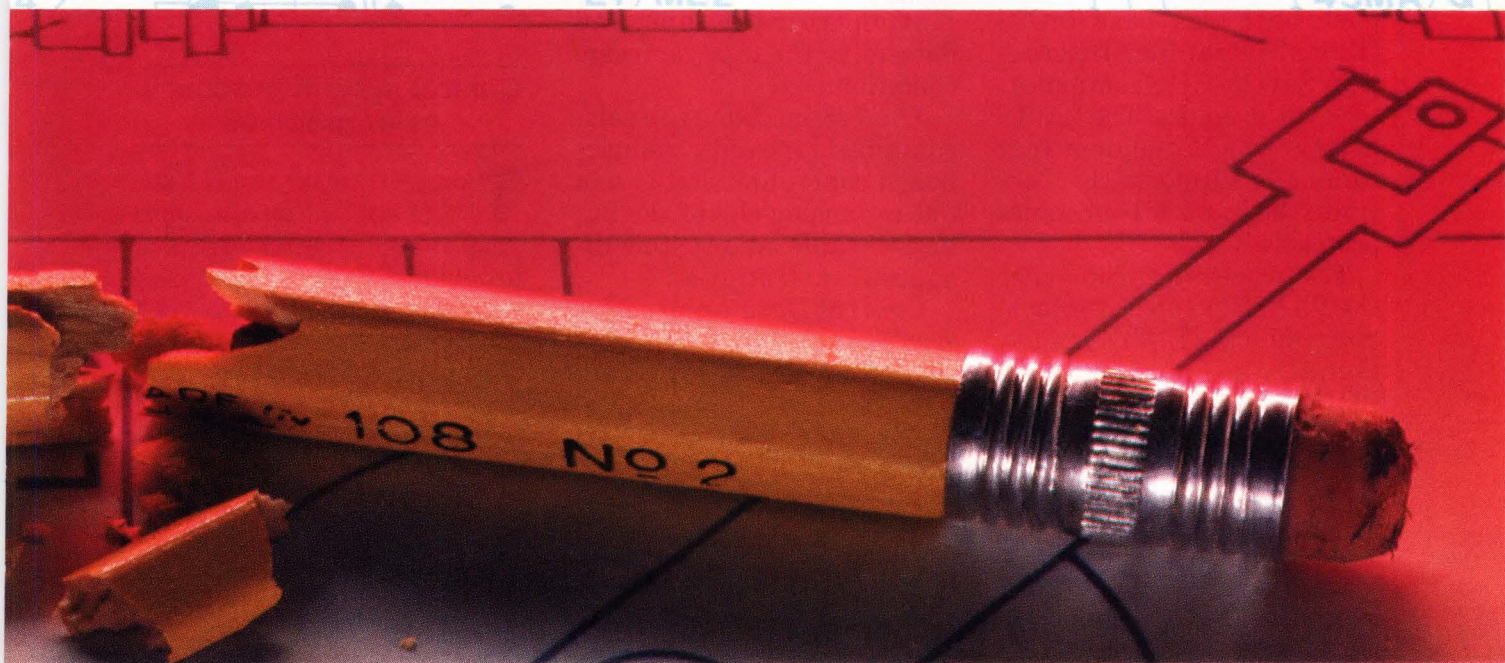
These modules can be incorporated into a VMEmodule system chassis or the VME/10 OEM microcomputer to meet a variety of demanding industrial applications and increase your flexibility.

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MOTOROLA

COMPUTER PERIPHERALS

Printers produce graphics, variable fonts

Targeted at a broad spectrum of users, the latest members of the LN01 family of laser printers provide graphics output and variable-font text on the same page. The LN01B features 16 resident labeling fonts and supports both DEC base ReGIS (Remote Graphics Instruction Set) and Calcomp plotter-type graphics. The LN01S printer has 12 resident text fonts and supports the Tektronix 4010 and 4014 graphics protocols.

The two printers run under the VAX/VMS operating system, while the LN01S is additionally supported by all PDP-11 operating systems. Housed in floor-standing cabinets, the LN01B and the LN01S are priced at \$22,520 and \$29,995, respectively.

Digital Equipment Corp., 146 Main St., Maynard, Mass. 01754; (617) 897-5111.

CIRCLE 335

45-Mbyte streamer works with IBM PC

Astreaming tape system that stores up to 45 million bytes of information on industry-standard DC300XL or equivalent 1/4-in. tape cartridges is compatible with the IBM Personal Computer.

Data is transferred by the StorageMaster 745 at a rate of 90,000 bytes/second using a streaming speed of 90 ips.

Three new software commands simplify the use of the tape system under IBM's DOS 2.X operating system. The DOS-like commands provide a means to backup and restore files, read directory information from the tape, and determine the tape cartridge condition.

The 745 includes the self-contained tape unit, a single-board controller that fits in one expansion slot of the PC, an I/O cable, and system diagnostics and utilities.

Control Data Corp., 2200 Berkshire Lane N., Plymouth, Minn. 55441; (800) 232-6789 or (612) 853-3276. \$2495.

CIRCLE 336

Floppy-disk subsystem stores 1600 kbytes

Providing data storage for a wide variety of system designs and application requirements is a floppy-disk subsystem that features high-level data file management and a 1600-kbyte storage capacity. On-board firmware utilizes CP/M-structured commands, operations, and formats.

The stand-alone Series 2000 master module contains two 5 1/4-in. 400-kbyte disk drives, a disk controller, a power supply, and an RS-232-C interface. A slave unit, the Series 2200, offers two additional drives and a power supply in an identical en-

closure. Combining the master and slave modules into an integrated system is the Series 2240.

Da-Tech Corp., 92 Steam-whistle Drive, Ivyland, Pa. 18974; (215) 322-9410. \$3300, \$2600, and \$5500 for the 2000, 2200, and 2240, respectively; 30 days.

CIRCLE 337

Control system produces color graphics

Targeted for use in CAD/CAM applications, a color graphics controller offers a programmable display resolution of 1024 by 781 pixels and Tektronix 4100 code-compatibility. The system comprises one or two graphics modules, a 68000-based CPU module, and a detachable keyboard. Available in either a desktop or rack-mounted version, the CG2100 interfaces with the computer and a high-resolution color monitor.

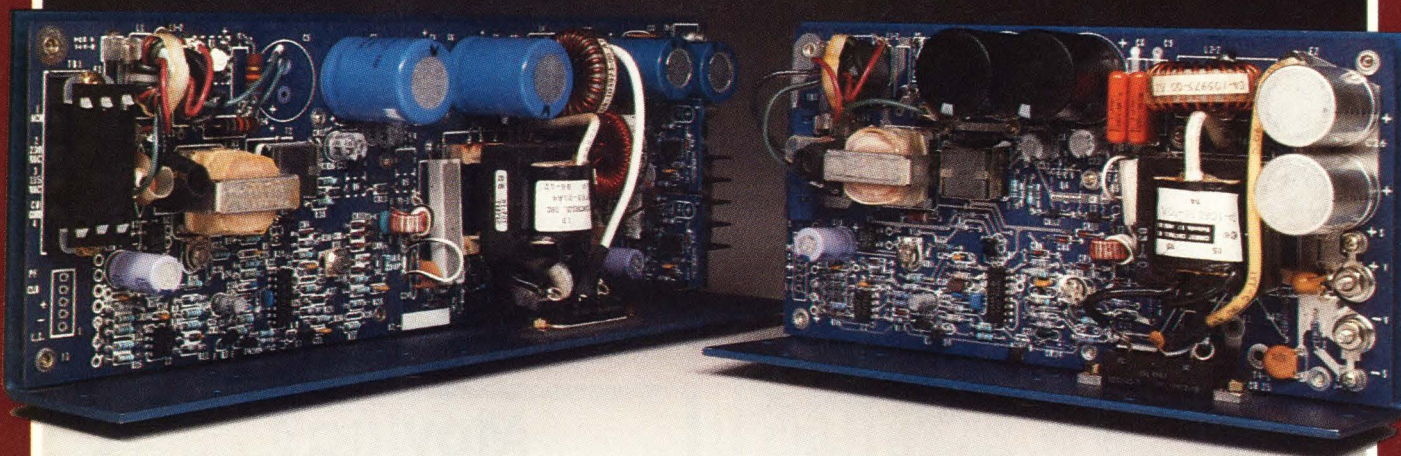
The VMEbus-compatible graphics module has four planes and is capable of producing 16 colors, chosen from a palette of 4096. In a dual configuration, each graphics surface has independent zoom and pan. The CPU board has an SCSI port for interfacing with a hard-disk drive, along with two RS-232-C serial ports and two parallel ports.

Cybernex Ltd., 1257 Algoma Road, Ottawa, Ont. K1G 3T8, Canada; (613) 741-1540. \$3995 and \$5595 (versions with one and two graphics modules, respectively).

CIRCLE 338

Computers, Peripherals, Instrumentation, Communications, Medical Electronics . . .

Our switchers are as good as gold
in all these applications and markets.



SWS Series



But it doesn't end there. For many years, Standard Power has designed and manufactured switching power supplies. In fact, our SWS Series of regulated switchers represents a third-generation power system—a design using a minimum number of components, with 100 percent burn-in, which means reliability. And that's critical to **your system's reliability.**

That's why Standard Power switchers keep showing up

in applications like process controllers, test equipment, telephone switching systems, such computer peripherals as drives, terminals, tapes and printers, document sorting equipment and machine tools.

The SWS Series includes 25 models—single, triple and quadruple outputs—in a power range from 150 to 250 watts. Each unit features line and load regulation at .2 percent each, built-in overvoltage protection and remote voltage sense on the main output, 20 millisecond holdup time and

UL recognition.

In addition, we were the first manufacturer to sell power supplies through electronic distribution. Today, more than 120 distributor locations stock our power supplies for off-the-shelf delivery. So go ahead and specify Standard Power . . . the quality switcher that's available.

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Santa Ana, California 92705

Telephone (714) 558-8512 • TWX: (910) 595-1760

CIRCLE 182

FACTORY AUTOMATION

Controller features simple programming

The SLC 100 programmable controller, a cost-effective replacement for electromechanical relays, timers, and hard-wired logic, is programmed using a simple ladder diagram language. The processor unit, including the CPU, the power supply, 16 I/O ports (10 input/6 output), and 855 words of user memory, requires only 37 in.² of panel space. Up to three I/O expansion units can be added to the processor unit for applications requiring up to 64 I/O ports (40 input/24 output).

The SLC 100 is designed to operate over a wide range of

ac and dc supply voltages. Users may select optically isolated input voltage ranges of 10 to 30 V ac/dc, 85 to 132 V ac, and 170 to 265 V ac.

Allen-Bradley Co., 1201 S. Second St., Milwaukee, Wis. 53204; (414) 671-2000.

CIRCLE 339

Basic chip set aims at industrial control

Designed specifically for ROM-based industrial control systems, C4 Basic includes a variety of standard Basic commands, plus a selection of additional commands for I/O interfacing and control applications. To expedite

development of C4 Basic programs, the companion NO-VOS nonvolatile operating system software enables programs to be created and tested directly on the target hardware. The ROM set is for use with the Z80 Smart Card, an STD bus processor board.

Unlike disk-based languages, C4 Basic requires a minimum of system RAM and ROM space. It features program execution directly in PROM for increased reliability, as well as automatic program execution at power-up.

VersaLogic Corp., 87070 Dukhobar Road, Eugene, Ore. 97402; (503) 485-8575. \$150 each or \$280 for the set.

CIRCLE 340

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3 Bit Planes direct (no D-A required)
- 100MHz Composite/Linear Video
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CIRCLE 183

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If mailing label is not available print your old Company name and address in this box

Please allow
6 weeks for
change to
take effect

2. Print your NEW business address here

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COMPANY _____

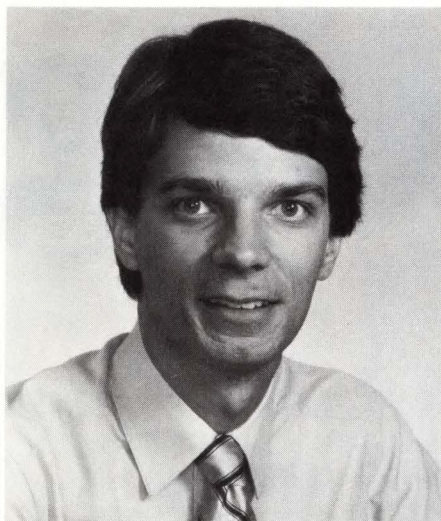
ADDRESS _____

CITY _____ STATE _____ ZIP _____

3. Mail to:

Electronic Design
P. O. Box 1418
Riverton, N.J. 08077 USA

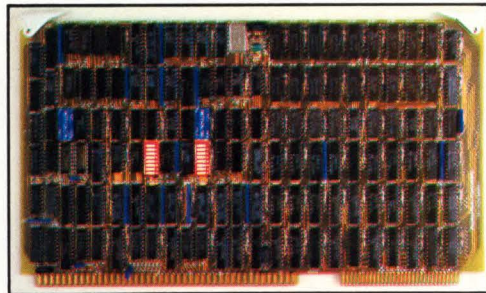
Central Data is High Performance Multibus* Speed



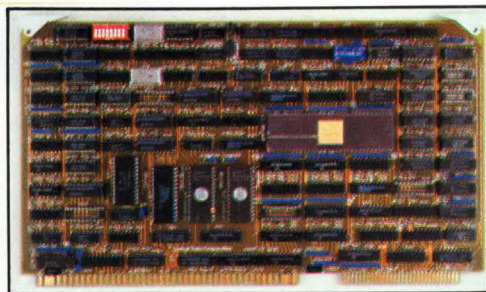
Jeff Roloff, President

"Central Data is committed to helping you get the maximum performance from your Multibus system. Our iLBX Cache Memory Board and 12.5 MHz 68000 CPU can do just that."

The new **Multibus iLBX* Cache Memory Board** delivers processor independent, high speed memory through the iLBX interface on the Multibus. The board's unique cache memory images the entire Multibus memory using a two-set LRU caching algorithm and stores 4K bytes of the most recently used memory. Access time is under 100ns, much faster than any dynamic RAM board. This new board also features write through operation, extensive error checking, and automatic and invisible deselection on error with interrupt. Its forced miss mapping allows use with dual-port memory on the Multibus. The **B1041** is available in 100 up pricing at \$1145.



The new **Multibus 12.5 MHz 68000 CPU** also takes advantage of the iLBX architecture by allowing connection to the Cache Memory Board or to dual port iLBX memory. The board's central processor is the powerful 68000 or optional 68010 and features paged SUN memory management. It supports 8 Multibus interrupt levels in either the bus-vector or non-bus-vector mode. The board has three programmable timers and two EPROM sockets for monitor or bootstrap programs. Its full multi-master capabilities allow the use of several processor boards and DMA devices on the bus at one time. The **B1045** is available in 100 up pricing at \$975.



Central Data

Central Data Corporation
1602 Newton Drive
Champaign, IL 61821-1098
217) 359-8010
TWX 910-245-0787
(800) 482-0315 Outside Illinois

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Complete
Multibus
Source

We've taken out operating

We've already done it for 200 American giants.

Companies who could well afford to develop their own real-time software. But instead called us.

Hunter & Ready.

Another software company, you ask?

No. But that brings us to the reason they called.

Simply put, Hunter & Ready components take the hard part out of real-time software.

Our software components handle the trickier parts of real-time. Functions like interrupts, I/O and task management. Which have nothing to do with making your application unique, but nonetheless take 60% of your software development time. Not to mention years of debugging and testing.

And if at this point you're wondering why components, the reason is simple.

Due to their standard nature, Hunter & Ready components provide the reliability strived for—but seldom attained—in real-time software. The kind that comes from 10 years of continual testing.

The same goes for any of our software components. The notable VRTX® real-time kernel. The multi-stream IOX component for character and disk I/O. The high-speed FMX component for file I/O. The TRACER component for real-time debugging.

Every one tried and proven. But that's not to leave you out of the picture.

Because it's up to you what you make of any one Hunter & Ready component. Whether it's a robot, PBX system or medical instrument. It merely acts as a real-time extension for any of today's popular microprocessors.

If all this sounds too good to be

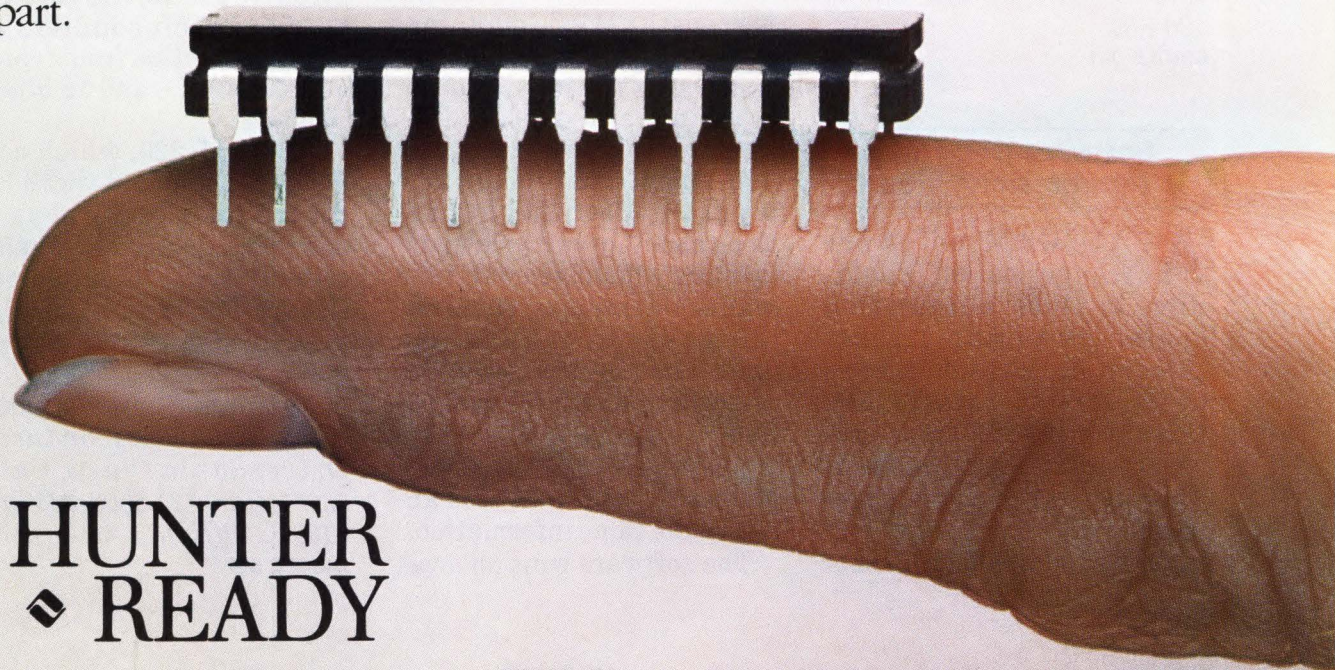
the hard part of systems.

true, we thought that it might. That's why we've prepared a packet with more details and some actual case histories.

We'd be glad to send it to you.

Just write Hunter & Ready,
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CA 94306. Or call (415) 326-2950.

If you can do that, we can do the
hard part.



HUNTER
◆ **READY**

FACTORY AUTOMATION

Fast control language suits robotics

Robasic is a high-level control language whose speed and ease of modification make it well suited for industrial control, robotics, and data acquisition. Although it is programmed in the same manner as Microsoft Basic, it runs an average of 30 times faster—eliminating the need for machine-code programming in 90% of all applications. Robasic achieves its speed through advances in both language architecture and syntax. For writing programs, Robasic incorporates a complete set of software development tools, including a text editor that allows programs to be written, tested, and stored on the single-board computer that they will be run on. Initially, the language will be offered on Octagon's 8088-based single-board computer.

Octagon Systems Corp., 6501 W. 91st Ave., Westminster, Colo. 80030; (303) 426-8540.

CIRCLE 341

Software performs robotic simulation

ACAD/CAM software package, called Robot-Sim, enables automation engineers to put a robot through its paces on a computer screen, rather than through trial-and-error procedures on the factory floor. The robotics package can also boost productivity by reducing the time needed for robot

work-cell implementation. Users can design a factory work cell, simulate a robot's movements and performance in the cell, and then modify both the robot's movements and the surrounding machinery to achieve optimum efficiency—all without employing a single piece of robotic hardware.

The robot library in Robot-Sim presently contains simulations for 20 popular industrial robots, which account for approximately 70% of all manufactured robots. The software product will be integrated into Calma's CAD/CAM system based on the Design, Drafting, and Manufacturing (DMM) core software.

Calma Co., 2901 Tasman Drive, Santa Clara, Calif. 95050; (408) 748-9600. From \$30,000; first quarter of 1985.

CIRCLE 342

Program optimizes manufacturing process

Prodstar MRP (manufacturing resources planning) aids in the planning, tracking, and overall efficiency of each step in the manufacturing process. The program offers such functions as bill of materials and inventory management, time management, master scheduling, cost accounting, and materials requirement planning. Prodstar MRP creates its own data base so that every department involved with the production process accesses the same information.

The software runs on a va-

riety of mini and microcomputers, such as VAX, HP 3000, and TI 990 series machines, as well as the IBM PC XT, HP 150, and Rainbow Plus computers. Prices for the mini and micro versions are \$35,000 and \$9900, respectively.

Satcom Inc., 11 Diamond Court, Glen Rock, N.J. 07452; (201) 447-5379.

CIRCLE 343

Board calculates signal frequency

Suitable for a variety of industrial applications, a frequency/period measurement board interfaces directly with most tachometers and voltage-to-frequency converters. Its four independent input channels can calculate the frequency or the period of each signal.

The totally digital CMOS board, designated the CIM-220, replaces expensive a-d converter boards in many applications. Moreover, the board's 16-bit counters increase resolution from typical a-d values of 8 and 12 bits to 16 bits.

The CIM-220, which conforms to the single-width Eurocard form factor, has an operating temperature range of -40° to $+85^{\circ}\text{C}$. A commercial version, the CIM-220C, is available for 0° to 70°C operation.

National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, Calif. 95051; (408) 721-5000. \$250 and \$180 (C suffix).

CIRCLE 344

**YOU OWE IT TO YOURSELF
TO CHOOSE FROM THE BEST.**

Choosing the right logic analyzer can be tough. But one thing is clear—you want all the advantages you know you can count on from the performance leaders.

**EVEN AMONG THE LEADERS,
THE DIFFERENCES CAN BE
SIGNIFICANT.**

For example, not all the top logic analyzers give you 200 MHz timing. Or highly sophisticated linkage and interactive analysis. Or 1000-word deep data collection and auxiliary memories. Or an easy-to-use ASCII keyboard. Or floppy disk data storage. *Only Nicolet's 800*

series gives you all these advantages. In the end, though, it's Nicolet's unmatched price/performance ratio that's the most important difference.

**SOME LOGIC ANALYSIS SYSTEMS
GROW WITH YOUR NEEDS.
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Only Nicolet makes it easy and inexpensive to enhance *performance*—not just add channels—any time you need it. And the NPC-800 Series gives you *five* instruments to choose from starting at \$7950, and more options than anyone else in the industry: Waveform Recorder, Performance Analysis, CT/SA, Computer/IEEE-488 Controller, Printer Software, Non-Volatile Memory, Dot Matrix Printer, and Second Disk Drive.

PUT THE LEADERS TO THE TEST.

When you really think about it, the only way to be sure is to let the best logic analyzers prove what they can do—for *you*. When it comes to capability, versatility, and performance, there's really only one choice. For a Logic Analyzer Comparison Chart, call: (800) NICOLET or (415) 490-8300 (inside CA). Nicolet Paratronics Corporation, 201 Fourier Ave., Fremont, CA 94539.

Think of us!

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CIRCLE 186

THE WORLD'S THREE GREAT LOGIC ANALYZERS.

HP 1630

NPC 800 SERIES

TEK 1240

FACTORY AUTOMATION

Module accepts 8 analog set points

Designed for G.E.'s Series 1 programmable controller, a dual-channel module installs in any I/O slot of the controller to provide eight independent analog set points. Using multiple input modules, the 14-slot Series 1 has the potential for monitoring up to 112 set points.

Three versions of the analog set-point module are available, covering input ranges of 0 to 5 V dc, 0 to 15 V dc, and 4 to 20 mA. The unit requires no special programming, and its plug-in design eases installation and maintenance. Available options in-

clude remotely mounted potentiometers and the ability to de-energize all inputs when no voltage signal is present.

Horner Electric Inc., 1521 E. Washington St., Indianapolis, Ind. 46201; (317) 639-4261.

CIRCLE 345

Industrial modem suits noisy environments

An industrial-grade short-haul modem board has a polarity-insensitive transformer coupling that eliminates dc continuity requirements and removes virtually all restrictions for receiving and transmitting data over

22 AWG wire in noisy, high common-mode-voltage areas. Error rates as low as one in a billion are possible using RS62A/U cable over distances of up to 7000 ft.

The standard 5.5-by-6.5-in. modem board, which handles asynchronous transmissions at 120 kbits/s, operates from ± 12 - and ± 5 -V dc supplies and accepts TTL-level bit-serial inputs. Built-in networking provisions support star, multidrop, and daisy-chain configurations or combinations thereof.

Controlonics Corp., Non-wire Division, 4 Kidder Road, Chelmsford, Mass. 01824; (617) 256-1918. \$350 (100 units); six weeks.

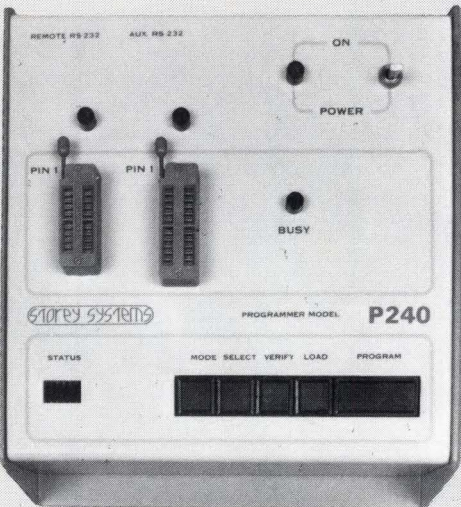
CIRCLE 346

Compact unit performs rectifier burn-in

For small-lot testing of axial-leaded rectifiers, the Model 1010-3-12 offers five forward-current settings and five reverse-voltage settings. The burn-in system tests up to five different lots simultaneously, ranging from 5 to 20 devices. The forward-current range of 0.1 to 3 A and a reverse-voltage rating of 0 to 1200 V peak provide adequate coverage for most rectifier testing. Moreover, a conduction angle of at least 175° is constant over the full current range. The system, which has dimensions of 44 by 24 by 26 in., is transportable.

Micro Instruments Co., 2250 Micro Place, Escondido, Calif. 92025; (619) 746-2010.

CIRCLE 347



Our
PAL
Programmers
Cost
LESS



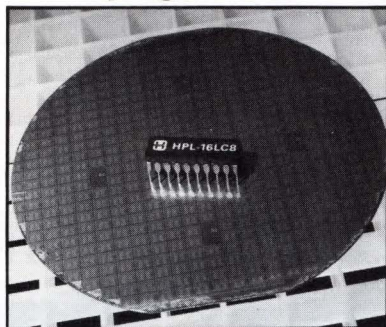
- Four Models to choose from
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CIRCLE 187

DIGITAL ICs

**CMOS logic circuit
is programmable**

Replacing discrete CMOS logic with a single package that saves both space and power is the HPL-16LC8 programmable logic circuit. The CMOS circuit is functionally equivalent to and pin-compatible with the industry-standard bipolar 16L8, but it consumes 95% less power.

The HPL-16LC8 has a maximum standby current of 150 mA, guaranteed over the commercial, industrial, and military temperature ranges. Operating current is guaranteed to be less than 5 mA/MHz; average operating power is less than 50 mW.

Harris Corp., Semiconductor Sector, PO Box 883, Melbourne, Fla. 32901; (305) 724-7800. From \$12.99 to \$36.07 (100 units).

CIRCLE 348

**Data-comm chip has 8
asynchronous lines**

To meet the demands for more asynchronous data lines when connecting terminals, printers, and other serial devices to 16- and 32-bit microcomputers, terminal concentrators, and multiplexers, a communica-

tions chip combines eight asynchronous serial lines in a single device. Called OCTART, the hybrid MOS chip is packaged in a 68-pin surface-mounted carrier and is functionally equivalent to eight UARTs. It features independent baud-rate generators for each line that support data rates from 50 to 19,200 bits/s.

The OCTART performs most of the character transmission- and reception-monitoring presently handled by higher-cost bit-slice control logic or additional board-level hardware. Its data/address multiplexed bus and timing signals are compatible with many 8-, 16-, and 32-bit microprocessors.

Digital Equipment Corp., 146 Main St., Maynard, Mass. 01754; (617) 897-5111.

CIRCLE 349

**Surface-mount RAMs
come in three versions**

Three single-in-line packages combine the density and cost advantages of advanced dynamic RAMs with surface-mounted technology. Designated the MI64X4, the MI64X8, and the MI64X9, they house four, eight, and nine 64k dynamic RAMs, respectively, in a package that is 3 in. long, less than $\frac{3}{4}$ in. wide, and less than $\frac{1}{4}$ in. deep.

The MI64X4 is aimed at systems with 4-bit-wide microcontrollers or systems that require full error-correcting. The MI64X8 is a candidate for a number of byte-wide systems, such as

personal computers. One bit wider than the MI64X8, the MI64X9 can be used in systems that require the ninth bit for parity checking. All three of the devices are available with 120- and 150-ns access times.

Micro Industries, 691 Greencrest Drive, Westerville, Ohio 43081; (614) 895-0404. From \$44.51 to \$89.04 (150-ns versions; 100 units).

CIRCLE 350

**16-bit registers
conserve board space**

Two 16-bit CMOS pipeline registers, which operate as fast or faster than comparable bipolar circuit combinations, can each replace eight octal registers or two 8-bit pipeline registers. Designated the LPR520 and LPR521, the devices are functionally compatible with AMD's AM29520 and AM29521 8-bit registers.

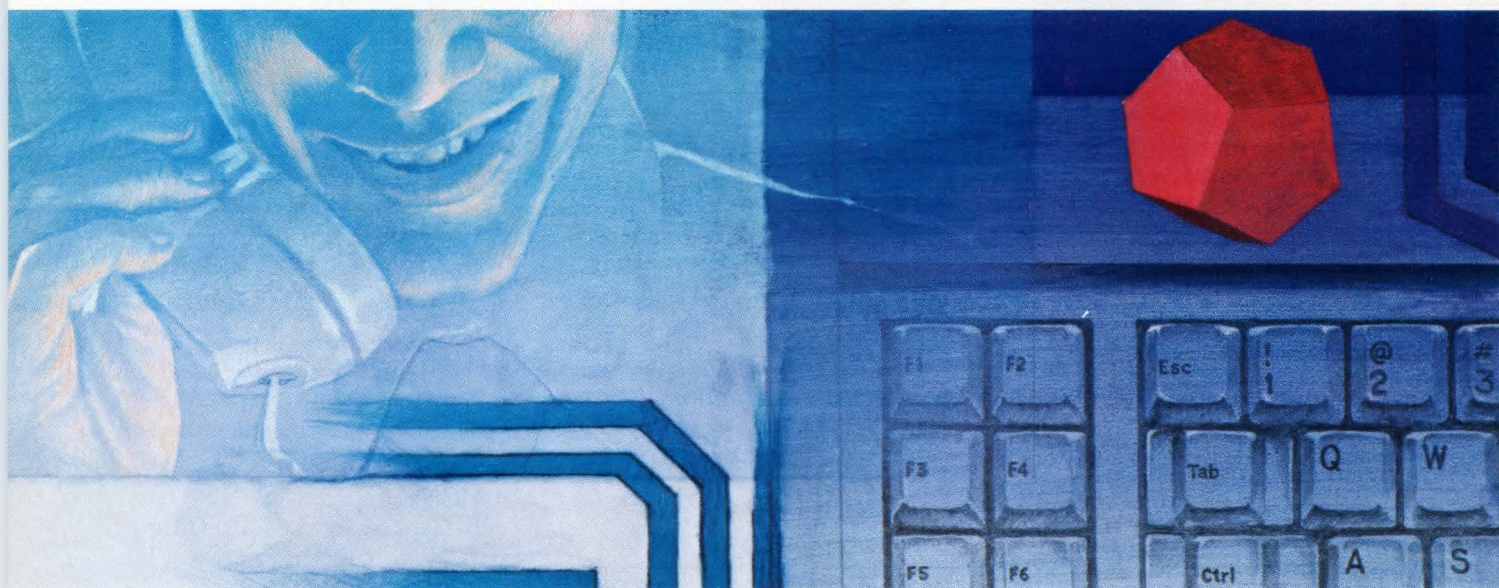
Each chip contains four 16-bit registers that can be configured as two independent two-level pipelines or as one four-level pipeline. The manner in which data is handled and preserved between registers on a load instruction is the only difference between the LPR520 and LPR521. Both of the registers are available in plastic or ceramic 40-pin DIPs.

Logic Devices Inc., 628 E. Evelyn Ave., Sunnyvale, Calif. 94086; (408) 720-8630. \$20 and \$64 for the plastic and ceramic versions, respectively (100 units).

CIRCLE 351

1-800-5

Cut your time at the voice/data drawing



As a communication systems designer, you have a difficult time keeping up with voice and data switching technologies. The recent trend toward combining telecommunication and computer products has made the voice/data market increasingly complex.

You can often get stuck right at the drawing board with new product designs.

Call us now, toll free, and we'll show you how state-of-the-art semiconductor technologies and over 150 innovative products can simplify challenging design-in tasks yet meet the complex market requirements of low cost, high performance and extreme versatility in the rapidly changing voice/data world.

Slash system cabling costs.

When the key requirement is cost, Motorola has the high technology answer. Take, for example, our Universal Digital Loop Transceiver (UDLT). This specialized integrated circuit system meets your customer's desire to avoid added data cable costs by allowing simultaneous high-speed data and voice to be transferred over common twisted-pair telephone wiring.

By integrating a PBX with the UDLT, the user can achieve a voice/data phone at every desk with the existing telephone wire in sprawling single-site commercial facilities. The resulting total network provides the optimum in performance for cost.

The UDLT is the first of its kind on the market; far ahead of any competitor.

Over 150 specialized devices for voice/data.

In addition to the added features and cost saving advantages of the UDLT, Motorola provides the broadest line of discrete semiconductors and bipolar and MOS LSI integrated circuits for voice/data applications.

For advanced telephone designs, put all the basic telephone functions on a single IC, including DTMF dialer, tone ringer, speech network and line voltage regulator.

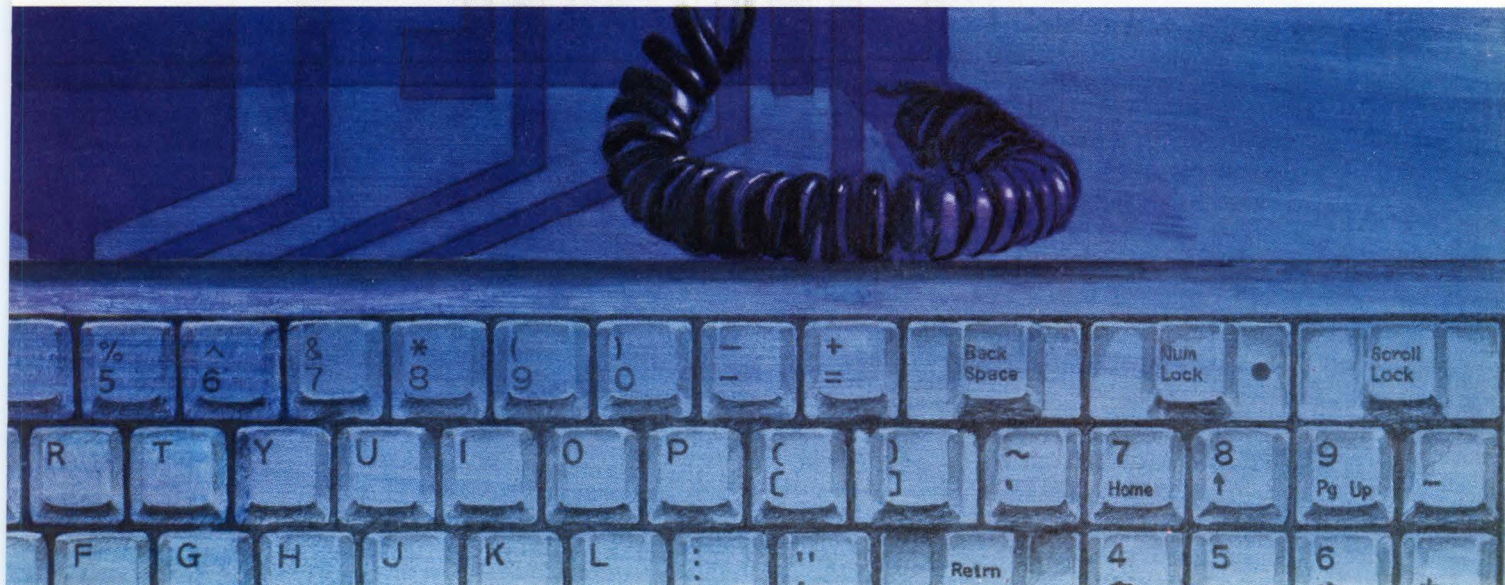
One-chip telephones. At the edge of technology.

To support your conventional modem needs, Motorola has a line of integrated modem ICs to simplify your design and manufacturing requirements. Single-supply operation and standard clock frequencies keep it simple. And inexpensive.

In sensitive data communication applications, Motorola provides fiber optic coupling devices with exceptional isolation, high current transfer ratios and industry standard packaging that outperform and cost considerably less than traditional electrical, coaxial or hard-wired transmission systems. Fiber optics. Light years ahead.

21-6274.

board. Call now for design-in support.



At the forefront for a reason.

Competition is intense to put integrated voice/data applications together while still meeting the demands of the user to be cost effective. With these stakes you cannot afford to trust an odd assortment of suppliers with yesterday's products. A total systems company geared to the future can keep your user's capital investment from becoming obsolete.

Motorola has built a complete system of integrated voice/data chips. We've targeted technologies to your market needs and applied design expertise to improve yield and reduce costs. And most importantly, we've maintained a fierce commitment to new products.

It all starts with design support from our massive staff of field application engineers. One's near you. An application engineer who can match new semiconductor technologies and products to your communication applica-

tion requirements so that, with your unique designs, you can perhaps leapfrog your competition. Fast.

1-800-521-6274

Talk engineer to engineer.

Motorola has tripled the number of application engineers it has throughout the U.S. and Canada.

Each has the expertise in emerging semiconductor technologies that can electrify your new voice/data ideas. Call 1-800-521-6274 and discuss your applications. Any time between 9 A.M. East Coast and 5 P.M. West Coast time. Toll free. Talk to our specialists. They'll discuss your applications and get you in touch with a field application engineer who'll, in person, describe in depth how Motorola voice/data products can cut your design time and keep you from going back to where it all starts. The old drawing board.

Wait'll you hear what we have in store for your new design. Be it in voice/data communication, office or

factory automation, entertainment equipment or any electronics-driven product, we'll work with you at any level of chip, board or box integration through the industry's premier technical field organization.

A Motorola semiconductor field application engineer is in the right location with the right expertise to help you.

Call us on it. One call. One source. For all your semiconductor needs.

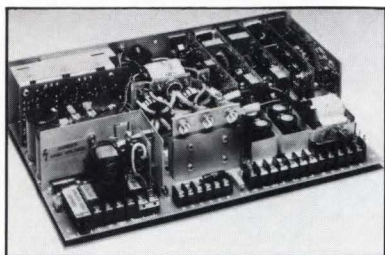
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**We're
on your
design-in
team.**



MOTOROLA

POWER

350-W switcher offers choice of outputs

The Powerflex series of 350-W switching power supplies has a main output of 5 V at 50 A and slots to accept up to four plug-in auxiliary output cards. The cards, which supply 12 to 15 V at 5 A, -12 to -15 V at 5 A, 24 V at 5 A (8 A peak), and -5 V at 2 A, may be used in any combination up to the maximum rating.

The open-frame supply offers a typical efficiency of greater than 70% with the main output fully loaded. Ripple and noise on the 5-V output are held to less than 70 mV over a bandwidth of 20 MHz. Worst-case regulation on stabilized outputs is 0.5%.

Advance Power Supplies Inc., 32111 Aurora Road, Solon, Ohio 44139; (216) 349-0755. \$470; four weeks.

CIRCLE 352

High-power regulators boast low dropout

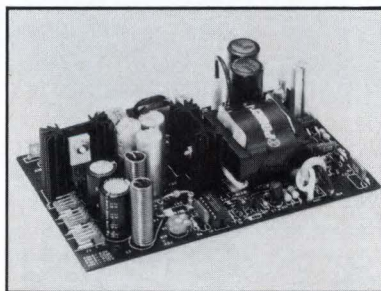
For applications requiring minimum input-output voltage differential, a line of linear regulator assemblies delivers 5 to 24 V with a dropout of less than 1 V. The PM-1 family of 3-, 6-, 12-, and 18-A

three-terminal regulators also offers low noise characteristics. Total peak-to-peak noise at maximum current is under 25 mV.

The entire PM-1 is housed in a modular assembly that is less than 2 in.³ and contains all of the associated control and linear regulator circuitry. Its mechanical design includes a radiator plate, which provides cooling that is adequate up to 5 A. For larger currents, the radiator plate can be bolted to a heat sink.

Silicon General Inc., Power Products Division, 940 Detroit Ave., Concord, Calif. 94518; (415) 686-6660. From \$15 (100 units); 90 days.

CIRCLE 353

150-W switcher aims at microcomputer users

A triple-output switching power supply provides the three most commonly required dc outputs (+5, +12, and -12 V) for powering desktop and personal computers, disk-based systems, CRT displays, and various peripherals. The SPL50-3200, which conforms to the industry-standard 40-W switcher case size, is capable of delivering a power output of up to 50 W. The +12-V output handles 2

A continuous and up to 4 A peak, making it well suited for pulsed-load applications. The switcher has an overall operating efficiency of 70%.

Power-One Inc., Switching Products Division, 833 Flynn Road, Camarillo, Calif. 93010; (805) 482-0757.

CIRCLE 354

Dc-dc converter suits portable printers

The second in a series of dual-output dc-dc converters that accommodate a nominal 12-V dc input, the DCM 102 is designed specifically to withstand the shock and vibration levels common to mobile, battery-powered printer applications.

The converter accepts a wide range of inputs—from 11 to 16.5 V dc—and is transient-protected up to ± 600 V. Outputs are +5 Vdc at 1 A and +24 V dc at 2 A, with a 15-A peak capability to withstand the surge produced when the printer is powered on. Line and load regulation are $\pm 1\%$ and $\pm 5\%$, respectively. The unit has a package size of less than 38 in.³.

Intronics Inc., 57 Chapel St., Newton, Mass. 02158; (617) 964-4000. \$175 (500 units); four to six weeks.

CIRCLE 355

COMPONENTS

2-in. plasma display eases viewing

Large 2-in.-high characters make the Model SP-461 plasma-gas discharge display particularly applicable in environments where the display must be viewed at long distances. The 14-segment alphanumeric display has a minimum viewing angle of 130° and can be read at distances of up to 90 ft. Working in temperatures from 0 to 55°C, the display is refreshed in 8 ms and requires a minimum of 170 V dc.

The actual size of the four-character package is 3.42 by 9.91 in., with a depth of only 0.769 in. Since the SP-461 stacks horizontally, users are not limited to the four-character display and can configure virtually any number of characters.

Beckman Industrial Corp., 2500 Harbor Blvd., Fullerton, Calif. 92634; (714) 773-8850.

CIRCLE 356

Midget timer conserves space

Occupying one-third the space of conventional time-delay relays, a plug-in midget timer combines solid-state circuitry with SPDT relay switching for full input-output isolation. The low-cost module, designated the type TGS, is 1 3/8 in. square and stands 2 in. high.

The timer is available with 5- or 10-A contacts and with timing ranges of 30 or 60 seconds, which can be either fixed or adjustable. It may be

specified for operation from supplies of 24 to 110 V dc and 24 to 115 V ac. Power consumption is less than 1 W for the dc units; 1 1/2 VA for the ac versions. The device's plastic enclosure has an 8-pin octal base.

Typical pricing for a 5-A unit with a 30-s adjustable timing range and a supply voltage of 115 V ac is less than \$10 in quantities of 1000.

Vanguard Relay Corp., 225 Cortland St., Lindenhurst, N.Y. 11757; (516) 226-5000. Stock to four weeks.

CIRCLE 357

Photoelectric amp mounts on pc board

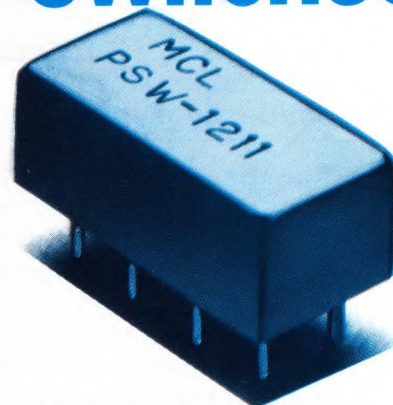
The ability to mount directly on a pc board allows the MPC3 photoelectric amplifier to be used in applications where conventional photoelectrics are not practical or cost-effective. The CMOS integrated circuit can be incorporated into products ranging from office copiers to robotic sensors.

The MPC3 includes the necessary circuitry to modulate nearly any LED and to amplify and demodulate a signal from almost any phototransistor. It can power opposed, diffused, or convergent sensors for either light or dark operation. The amplifier comes with a built-in alignment system that indicates both alignment and signal strength.

Banner Engineering Corp., PO Box 9414, Minneapolis, Minn. 55440; (612) 544-3164.

CIRCLE 358

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1000-2000 MHz	25 dB min.
2000-2500 MHz	22 dB min.
SWR	1.5 max. ("on" state)
SWITCHING SPEED	1 μ sec. (max.)
MAXIMUM RF INPUT	+20 dBm
CONTROL	+5 V (5 mA max.)
OPERATING TEMPERATURE	-54°C to +100°C
STORAGE TEMPERATURE	-54°C to +100°C
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CIRCLE 188

C102-3 REV. ORIG.

COMPONENTS

MIL connector has antidecoupling device

The MIL-C-38999 Series III cylindrical connector features an antidecoupling mechanism that maximizes shock and vibration resistance. The thicker wall sections and greater coupling surface of the series provide sine vibration resistance of up to 60 G for a duration of 36 hours at 175°C. Full peripheral metal-to-metal RFI-shielding fingers and 100% metal-to-metal bottoming provide EMI protection between 100 MHz and 10 GHz, with a minimum 50-dB effectiveness at 10 GHz. Positive full mating occurs with a 360° rotation of the coupling nut for quick connecting and disconnecting, with both tactile and visual positive-mating indicators. Thirty-three contact layouts are available in shell sizes ranging from 9 to 25.

Deutsch Co., Municipal Airport, Banning, Calif. 92220; (714) 849-7822.

CIRCLE 359

SIP resistors meet MIL low-profile specs

The TaNFilm 4900 series exceeds the performance standards for the latest mechanical specifications of MIL-R-83401 for low-profile 6-, 8-, and 10-pin SIP resistor network configurations. The devices are designed for precision instrumentation and military applications requiring long-term reliability and stability in a small amount of

space. They are particularly suited to applications where surface mounting is either not feasible or too costly.

Temperature characteristics are uniform among all of the resistors within each network, with temperature coefficients of resistance to within ± 25 ppm/°C and standard tracking of 5 ppm/°C. Resistance tolerances of $\pm 0.1\%$, $\pm 0.25\%$, $\pm 0.5\%$, $\pm 1\%$, and $\pm 2\%$ are available, along with resistance ranges of 20 Ω to 100 k Ω . The networks, which have an operating temperature range of -55° to $+150^\circ\text{C}$, have an on-board height of 0.187 in. (± 0.010) and a width of 0.074 in. (± 0.024).

TRW Electronic Components Group, Resistive Products Division, 4222 S. Staples St., Corpus Christi, Texas 78411; (512) 992-7900. \$1.40 to \$3.30 (1000 units); 8 to 10 weeks.

CIRCLE 360

Heavy-duty relay is mini sized

With dimensions of 9.8 by 24 by 25 mm, the heavy-duty VG series relay meets the high-density packaging requirements of industrial control applications. The relay is available in 1-, 3-, and 5-A versions, with a choice of either SPST or SPDT contact arrangements. It has a life expectancy of 10 million mechanical operations and 100,000 electrical operations at rated load.

Available coils include

heavy duty (TV-5) and standard types, which consume 0.38 W at 20°C, and a high-sensitivity type, which consumes 0.22 W at 20°C. The VG series also accommodates a wide variation of temperatures. Standard 3-A relays operate in temperatures ranging from -40° to $+75^\circ\text{C}$; more sensitive types can withstand temperatures to $+85^\circ\text{C}$.

ITT Components, 1201 E. McFadden Ave., Santa Ana, Calif. 92705; (714) 836-0351. From \$1.40 (1000 units); 10 to 12 weeks.

CIRCLE 361

Oscillator drives high-speed ECL devices

The ECL-compatible K1149-AM crystal clock oscillator drives devices with extremely high speeds, such as the MECL 10K and 10KH logic families. The oscillator has a frequency range of 60 to 90 MHz, with a stability of ± 100 ppm. Rise and fall times are rated at 1.0 ns typical, 2.0 ns maximum. Operating from a supply voltage of -5 V dc $\pm 5\%$, the K1149AM has a typical supply current (I_{ee}) of 30 mA.

The all-metal hermetically sealed package, which can be soldered or plugged into a standard DIP socket, requires only 0.820 by 0.520 in. of pc board space and has a seated height of 0.270 in.

Motorola Inc., Components Division, 2553 N. Edgington St., Franklin Park, Ill. 60131; (312) 451-1000.

CIRCLE 362

COMPONENTS

2-in. LED display uses just 13 diodes

Useful for a variety of applications requiring a 2-in. numeric readout, a multidigit display uses only 13 diodes per digit and includes a counter and support circuits. Each numeral is formed by a numeric character module, which costs less than 1½-in. ASCII alphanumeric types. The modules are 1.75 in. wide by 3 in. high and 2 in. deep (somewhat smaller than a pack of cigarettes). They are offered as packaged displays with any number of digits.

The two printed circuit boards that fit together to form the module are held together by flat cable connectors. Counters can be arranged to advance the tally in steps of any size.

Bayside Timers Inc., 43-69 162nd St., Flushing, N.Y. 11358; (212) 463-8935.

CIRCLE 363

Rf transformers are subminiatures

Transfer molded as small as 0.185 in. square and 0.065 in. high, surface-mounted rf wideband transformers operate in the frequency range of 500 kHz to 500 MHz. Insertion loss for the subminiature transformers is typically 0.5 dB. The series is rated for 100 mW and features dc isolated or nonisolated primary and secondary windings at impedances of 50 to 800 Ω. Additionally, the secondary

winding is either balanced (center-tapped) or unbalanced (no tap). The devices are designed to exceed the requirements of MIL-T-55631. The transformer's flat gold-plated terminations are

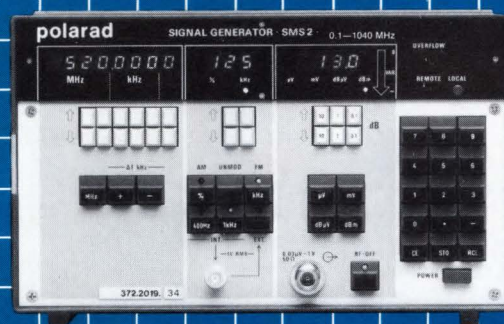
suitable for gold bonding in hybrid enclosures or for conventional pc board mounting.

Vanguard Electronics, 1480 W. 178th St., Gardena, Calif. 90248; (213) 323-4100.

CIRCLE 364

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IEEE-488

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PACKAGING & MATERIALS

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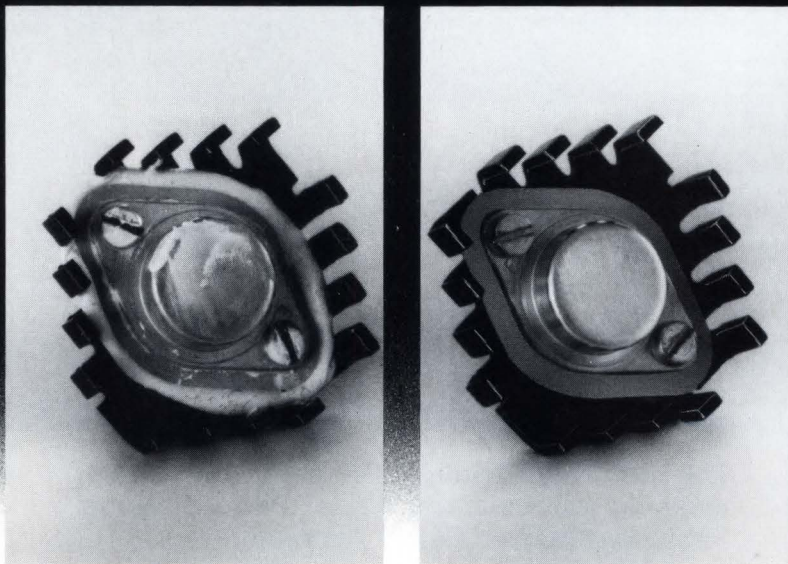
VDE approvals and is available in the popular sizes of 5, 4.7, and 3.15 in. square. The fans can be specified at voltages from 24 to 380 V and with airflows from 20 to 145 cfm (cubic feet/min). Constructed

to provide reliable operation at the lowest acoustical noise levels, the fans have an outer die-cast aluminum frame, a plastic impeller that meets the UL 94VO flammability rating, and ball bearings. The ball bearings permit operation at elevated temperatures (up to 70°C) and allow installation in any orientation.

Inmark Corp., 147 W. Cedar St., Norwalk, Conn. 06854; (203) 866-8474. \$13.81 (5-in. model, 500 units).

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CIRCLE 190

Receptacle and key speed firmware changes

For use with any 24- or 28-pin EPROM, Chipkey is a unique package that enables firmware changes to be made quickly and easily. The EPROM is mounted on a "key" and inserted through the equipment panel into the Chipkey receptacle. All of the memory device's connections are transferred via ribbon cable from the Chipkey receptacle to the EPROM socket, without circuit board modifications. Once installed, a bezel door closes over the key slot and the key is removed.

An evaluation kit is available for \$98 and contains everything needed to implement the Chipkey in any microprocessor-based product in which the ROMs and EPROMs are socketed.

ABC Systems Inc., 511 11th Ave. S., Suite 208, Minneapolis, Minn. 55415; (612) 333-0004.

CIRCLE 366

PACKAGING & MATERIALS

Evaluation kits
test GaAs ICs

Two design evaluation kits provide the necessary hardware and pc board interconnections for testing high-speed gallium arsenide ICs. The kits are designed for 50- Ω impedance system operation, which is required for most GaAs IC testing.

The HMK-11MSI-1 is designed to be used with 32-pin MSI products, such as the HMD-11141-1 four-bit universal shift register and the HMD-11016-1 divide-by-two/four/eight binary counter. The second kit, the HMK-11SSI-2, is for use with 16-pin SSI products, including the master-slave D flip-flop, the divide-by-two prescaler, and the five-input NOR/OR gate.

Harris Microwave Semiconductor Inc., 1530 McCarthy Blvd., Milpitas, Calif. 95035; (408) 262-2222. \$375 and \$350 (32- and 16-pin versions, respectively); four to six weeks.

CIRCLE 367

Six-slot chassis
extends IBM PC's power

For applications requiring more card slots than are available on the IBM PC, PC XT, or PC-compatible computers, the B106 expansion chassis offers six additional card slots. By using two expansion cards (one in the computer and the other in the expansion chassis) and a pair of ribbon cables, the remaining five card slots become a parallel extension of the PC's bus.

The chassis, which includes a self-enclosed 65-W power supply and a cooling fan, provides standard 1-in. card spacing on a low-noise backplane. The B106 costs \$795; the B120 interface kit (includ-

ing two expansion cards and cables) is priced at \$195. Delivery is four to six weeks.

Action Instruments Inc., 8601 Aero Drive, San Diego, Calif. 92123; (619) 279-5726.

CIRCLE 368

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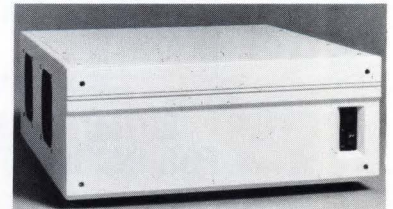
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PACKAGING & MATERIALS

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surface-mounted devices**

The Soldermaster SMD is a miniature soldering iron designed specifically for surface-mounted devices. Its

short reach permits precise positioning of components on fine-line circuitry and is suitable for soldering and desoldering under a microscope. A wide selection of miniature tips is available for dual-in-

line leads and leadless packages, including slotted spade tips for use with chip resistors and capacitors.

The standard Model SMD 10 has an idle temperature of 700°F. All Soldermaster SMD irons incorporate the posi-ground feature, which ensures less than 2 mV of leakage to comply with military specifications.

Hexacon Electric Co., PO Box 36, 161 W. Clay Ave., Roselle Park, N.J. 07204; (201) 245-6200.

CIRCLE 369

**Adhesives bond
various substrates**

Two lines of structural adhesives—designated the Scotch-Weld brand and the Pronto brand—are designed for high-strength bonding of metals, rigid plastics, wood, and many other materials for electronic and product-assembly applications. Scotch-Weld film adhesives provide a metal-to-metal shear strength of 2000 psi at 75°F. Epoxy adhesives in the series have overlapping shear strengths from 1200 to 3000 and 2000 to 4500 psi, while a urethane adhesive spans 2400 to 3100 psi.

The Pronto series of one-part instant adhesives cures in seconds and requires only contact pressure to form strong bonds with a variety of substrates.

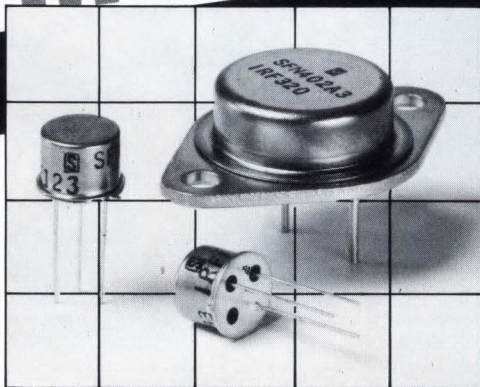
3M, Adhesives, Coatings, and Sealers Division, 223-1N, 3M Center, St. Paul, Minn. 55144; (612) 733-1110.

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PRODUCT NEWS

Program links Data General, DEC systems

Two previously incompatible systems—Data General's CEO office system and Digital Equipment's All-in-One series—can now communicate with one another via transNET, an IBM mainframe-based communications software tool from **Network Applications Inc. (Austin, Texas)**. When installed on an IBM or look-alike mainframe, transNET permits the two manufacturers' systems to exchange text documents, which can be edited by either system irregardless of whether they are sending or receiving. Additionally, the software enables the systems to be linked to a Xerox 2700 laser printer. The Network Applications' product is a compatible enhancement of IBM's DISOSS, the medium through which IBM's incompatible office systems communicate using the host mainframe.

CIRCLE 371

Graphics terminals gain IBM-compatibility

Tektronix Inc. (Beaverton, Ore.) has broadened the compatibility of its 4100 series of computer display terminals by making them plug-compatible with the IBM 3270. Designated the CX4100 series, the new models provide direct coaxial connection to IBM 3274 cluster controllers, as well as alphanumeric-emulation of the 3278/3279 machines. The CX series also enables the user to employ Tektronix' Plot 10 graphics command set, which carries out a greater portion of the graphics task at the terminal than does IBM's symbol-cell graphics.

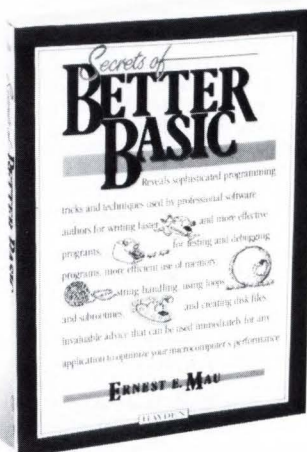
CIRCLE 372

Kit simplifies fiber-optic terminating

To ease the termination process, a kit includes everything needed to effortlessly strip, crimp, epoxy, polish, and/or inspect any fiber-optic communication cable that uses SMA connectors. Dubbed "The Terminator" by its maker—**Optical Fiber Technologies Inc. (Nutting Lake, Mass.)**—the kit includes for the first time buffer- and cable-stripping tools, a 100× microscope, a polishing plate, and scribing tools. These are in addition to the heat gun, crimp tools, epoxy packets, blades, polishing tools, scissors, and other products that make up the kit. With each Terminator kit is a free 50-page manual entitled *Optical Cable Terminating Procedures and Techniques*.

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NEW PRODUCTS

PRODUCT NEWS

Robotic handler loads hybrid substrates

To eliminate operator loading and unloading of hybrid circuit substrates, **Teradyne Inc. (Boston, Mass.)** designed a robotic handler that delivers the substrates to the company's W419 passive laser-trimming system. The handler is available in two configurations. A complete, self-contained model comprises an X-Z Cartesian-coordinate positioner arm (equipped with either a vacuum pickup hand or a gripper), a preloading station, and a shuttle arm, which transports the substrates from the preloading station to the W419's trim chuck. The price of this configuration is expected to begin at under \$50,000. For users who already have robots or other automation equipment, the handler's shuttle arm is available by itself, starting at about \$20,000. This partial configuration integrates easily with existing production environments, including those with conveyor systems.

CIRCLE 374

Software aids acquisition and control

Compatible only with the 2452 measurement and control system, ProGen application software—from **John Fluke Manufacturing Co. Inc. (Everett, Wash.)**—allows users to program up to 500 I/O channels for a wide range of applications, including batch processing, process control, and automated testing. The English language, menu-prompted software uses Fluke's touch-sensitive display as the user-interface. The programmer defines functions, alarm limits, procedures, and process parameters. A separate operator disk is then automatically created to protect against inadvertent changes to the program.

CIRCLE 375

New source for Gould switching supplies

The sales and servicing of switching power supplies formerly offered by Gould Inc. are now handled in the U.S. and Canada by **Advance Power Supplies Inc. (Solon, Ohio)**. The change in source and service for the product line results from the buy-back of the Gould power supply operation by the original equipment developer and manufacturer, Advance Power Supplies Ltd. of Bishop's Stortford, England. The U.K. plant will continue to manufacture and market the supplies in Europe and Asia. The full range of Advance switching power supplies includes open-frame, miniature, enclosed, and modular units for use in a variety of business, industrial, consumer, and military applications.

CIRCLE 376

PRODUCT NEWS

Logic analyzer gets 300-MHz trigger

A 300-MHz trigger for the 64300S logic analyzer, from **Dolch Logic Instruments Inc. (San Jose, Calif.)**, gives the user a high-speed (3.3-ns) instrument for locating hard-to-find timing problems that are common in newly developed logic circuits. In one mode of operation, the trigger can enable (arm) the standard recording channels to search for its trigger sequence. The second mode allows the standard recording-channel trigger to enable the independent 300-MHz trigger.

CIRCLE 377

Ultrafast 15-ns PALs go into production

Previously available in sample quantities only, **National Semiconductor Corp. (Santa Clara, Calif.)** has put its ultrafast PAL family into full production. Boasting a maximum access time of 15 ns over the commercial temperature range (0° to 85°C), the family is one of the fastest in the industry. The devices are also available for the military temperature range of -55° to +125°C, with access times of 20 ns. The new members include the PAL1618B, with active low outputs, and the -16R8B, -16R6B, and -16R4B, with registered outputs. Typical power dissipation for all of the devices is 600 mW.

CIRCLE 378

Round switches fit square cut-outs

A new adapter from **EAO Switch Corp. (Milford, Conn.)** allows the company's push buttons, keylocks, and other 5/8-in.-round hole-mounted controls to be inserted into square or rectangular panel cut-outs. Adapters are available for 0.75 in. square and 0.75-by-1.14-in. rectangular holes (19 mm square and 19 by 29 mm, respectively). The square adapter (31-948) and the rectangular adapter (31-949) have a suggested list price of \$0.60 each.

CIRCLE 379

Headers reformulated for surface mounting

Enabling them to withstand the high temperatures of surface-mounting procedures, the Series 235, 295, and 318 headers from **Aptronics Corp. (Mentor, Ohio)** are now made of 30% glass-filled polyester that meets the UL 94 V-0 flammability rating. The male headers withstand temperatures as high as 125°C over extended periods of time and up to 219°C for one minute.

CIRCLE 380

ElectronicDesign

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ANNUAL REPORTS

Annual and interim reports provide more than financial information. They often include the first public disclosure of new products, new techniques, and new directions of a company. Reports often contain superb analyses of the industry that a company serves.

Selected companies with recent reports are listed here with their main electronic products or services. Circle the indicated number for a copy.

AVX Corp. Multilayer ceramic capacitors in a wide variety of configurations.

CIRCLE 382

Advanced Micro Devices Inc. Microprocessor, peripheral, memory, analog, and logic products for electronic systems manufacturers.

CIRCLE 383

Ashton-Tate. Microcomputer software and computer-related books and periodicals.

CIRCLE 384

Avant-Garde Computing Inc. Products for data-communication network management.

CIRCLE 385

Bell Industries Inc. Uncoated aluminum memory disks and other computer and electronic components.

CIRCLE 386

Burndy Corp. A broad line of electrical and electronic connectors and related products.

CIRCLE 387

C3 Inc. Turnkey mini- and microcomputer systems for the Department of Defense and non-defense agencies of the U.S. government.

CIRCLE 388

Compaq Computer Corp. Personal computers for business and professional use.

CIRCLE 389

Computer Memories Inc. High-capacity 5 $\frac{1}{4}$ -in. Winchester disk drives.

CIRCLE 390

Ferro Corp. Specialty coatings, colors, chemicals, ceramics, and thermoplastics.

CIRCLE 391

Fujitsu Ltd. Computers ranging from single chips to large-scale systems; semiconductors and other advanced electronic components.

CIRCLE 396

GTE Telenet Communications Corp. Dedicated networks and electronic messaging systems.

CIRCLE 392

General Instrument Corp. Communications equipment, real-time data systems, semiconductor products, keyboards, and switching power supplies.

CIRCLE 393

Gerber Scientific Inc. Factory automation systems and CAD/CAM products.

CIRCLE 394

Gull Inc. Instrumentation systems, special-purpose computers, and equipment for military, commercial, and general aviation aircraft.

CIRCLE 395

Integrated Logic Systems Inc. Semicustom VLSI logic array products.

CIRCLE 397

Method Electronics Inc. Electronic components that connect, convey, and control electronic energy and pulse.

CIRCLE 398

Micom Systems Inc. Microcomputer-based data communications products.

CIRCLE 399

Micro Mask Inc. Photomasks and hard-surface photoplates for semiconductors and ICs; transformers, chokes, filters, coils, and reactors.

CIRCLE 400

Mitel Corp. Telecommunications products, multi-functional workstations, semiconductors, and thick-film hybrid circuits.

CIRCLE 401

Molex Inc. Connectors, conductor cable, terminals, and interconnection systems.

CIRCLE 402

Nuclear Data Inc. Double-sided and multilayer printed circuit boards; computer-based products for nuclear physics and the nuclear power industry.

CIRCLE 403

Pantasote Inc. Polymer- and elastomer-based specialty products, such as PVC film and sheeting.

CIRCLE 406

Park Electrochemical Corp. Multilayer circuitry materials for the military, aerospace, computer, and electronic instrument markets.

CIRCLE 404

Plessey Co. Telecommunications and aerospace products, microelectronics, and components.

CIRCLE 405

Questronics Inc. Equipment that monitors the performance of data communications networks.

CIRCLE 407

Raytheon Co. Electronic countermeasures, radar systems, communications equipment, microwave components, and semiconductor devices.

CIRCLE 408

Tandem Computers Inc. Computer systems for on-line transaction processing.

CIRCLE 412

Tektronix Inc. Electronic measurement, display, and control instruments and systems.

CIRCLE 409

Timeplex Inc. Multiplexers, network management equipment, modems, and other data communications products.

CIRCLE 410

Toshiba Corp. Semiconductors and other electronic components, office automation equipment, and telecommunications products.

CIRCLE 411

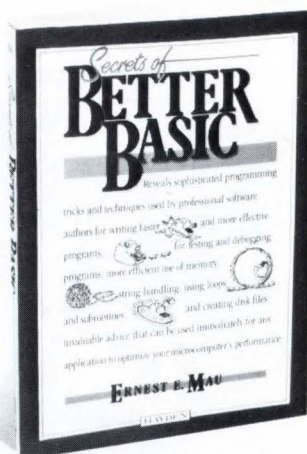
Tylan Corp. Proprietary components, subsystems, and systems for use in semiconductor processing.

CIRCLE 413

Verdix Corp. Hardware, software, and system-level products for computer security.

CIRCLE 414

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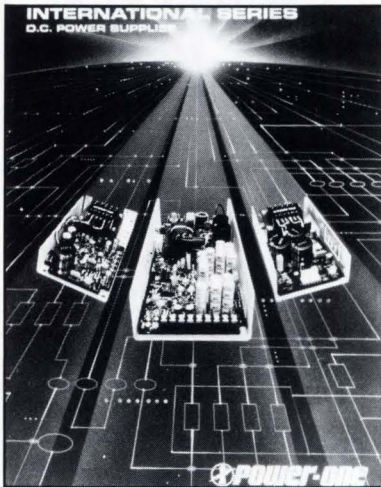
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NEW LITERATURE

Linear and switching dc power supplies



Including photos and mechanical drawings, this 28-page color catalog gives complete specifications and prices for more than 200 off-the-shelf linear and switching dc power supplies. A special applications section explains safety requirements for domestic and international marketing.

Power-One Inc., Power One Drive, Camarillo, Calif. 93010; (805) 987-8741.

CIRCLE 415

I/O controllers for Data General minis

Outlining an entire line of peripheral interfaces and controllers for Data General's Nova, Eclipse, and MV minicomputers is a six-page brochure. It includes SMD-interfaced disk controllers, magnetic tape couplers, and direct-memory-access line printer and terminal controllers. The brochure also high-

lights Zetaco's line of Slot Savers, multifunction boards that control general-purpose I/O peripherals.

Custom Systems Inc., Zetaco Division, 6850 Shady Oak Road, Eden Prairie, Minn. 55344; (612) 941-9480.

CIRCLE 416

RS-232-C molded cable assemblies

A bulletin (No. C-103) introduces a line of 25-position molded cable assemblies that conform to the EIA Standard RS-232-C. The parts-numbering system allows designers to quickly design and specify thousands of feature variations from catalog data. Also included in the literature are extension cables and gender changers.

Cablelink Inc., 311 Childers St., Kings Mountain, N.C. 28086; (704) 739-7473.

CIRCLE 417

IEEE-488 interface cards

Boards for interfacing with the IEEE-488 bus are featured in a 20-page pamphlet, along with the operating system and language support products available for each. Information about bus extenders, bus controllers, and bus testers is also included.

National Instruments, 12109 Technology Blvd., Austin, Texas 78727; (512) 250-9119.

CIRCLE 418

Computer systems engineering reference

The *Kierulff Designer's Guide* is a single-source reference of technical information for computer system designers. The 350-page volume provides detailed information on computer hardware, software, peripherals, data communications equipment, and accessories from more than 25 leading manufacturers. As a technology review, it aids in the selection of products that best suit the application. The prepublication price of \$37.50 will be in effect until December 15, 1984, after which the guide will be \$75.

Kierulff Electronics Inc., 2585 Commerce Way, Los Angeles, Calif. 90040; (800) 338-8811 or (213) 725-0325.

CIRCLE 419

MIL-C-83421/1 capacitors

An 11-page brochure presents a line of metalized polycarbonate film capacitors manufactured to meet MIL-C-83421/1 specifications. The document provides complete specifications and discusses the design and construction, failure rate, dielectric strength, dissipation factor, insulation resistance, and operating temperature ranges of the devices.

West-Cap Arizona, SFE Technologies, 2201 E. Elvira Road, Tucson, Ariz. 85706; (602) 294-2646.

CIRCLE 420

Solderforms line of solder preforms

Presenting the Solderforms line of solder preforms is a 12-page pamphlet that discusses both the advantages and possible disadvantages of using preforms. It lists the specifications of Solderforms made from foil and wire solders and solder spheres. A chart lists alloy compositions, their melting ranges, specific gravities, and tensile strengths.

Kester Solder, 4201 Wrightwood Ave., Chicago, Ill. 60639; (312) 235-1600.

CIRCLE 421

Bipolar analog integrated circuits

A short-form catalog presents both standard and custom bipolar analog ICs. It contains representative IC layouts, cross sections of various components, and product descriptions.

Solitron Devices Inc., 1177 Blue Heron Blvd., Riviera Beach, Fla. 33404; (305) 848-4311.

CIRCLE 422

Fairchild Advanced Schottky TTL family

The Fairchild Advanced Schottky TTL (FAST) family of digital logic integrated circuits is characterized in a 680-page manual. The FAST data book has complete rating, specification,

waveform, packaging, and ordering information for 166 devices. Families covered range from gates and flip-flops to memory and microprocessor support chips.

Fairchild Camera and Instrument Corp., Product Planning Department, Digital Unit, 333 Western Ave., South Portland, Maine 04106; (207) 775-8706.

CIRCLE 423

Schottky and p-i-n diodes

A binder consisting of 40 individual data sheets details a variety of Schottky, p-i-n, limiter, silicon multiplier, and varactor diodes. Each data sheet presents features, applications, and specifications, as well as charts and package outlines.

Metelics Corp., 1031 E. Duane Ave., Suite D, Sunnyvale, Calif. 94086; (408) 737-8181.

CIRCLE 424

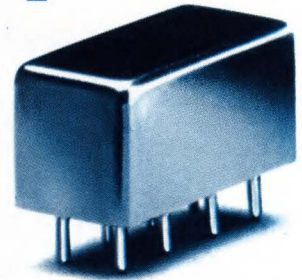
Standard and custom timing controls

It's About Time is a 48-page publication that describes a full line of timing controls. Products include digital plug-in time-delay relays, open-board time-delay relays, encapsulated solid-state timing controls, digital appliance controls, and accessories.

Infitec Inc., PO Box 4774, Syracuse, N.Y. 13221; (315) 455-2419.

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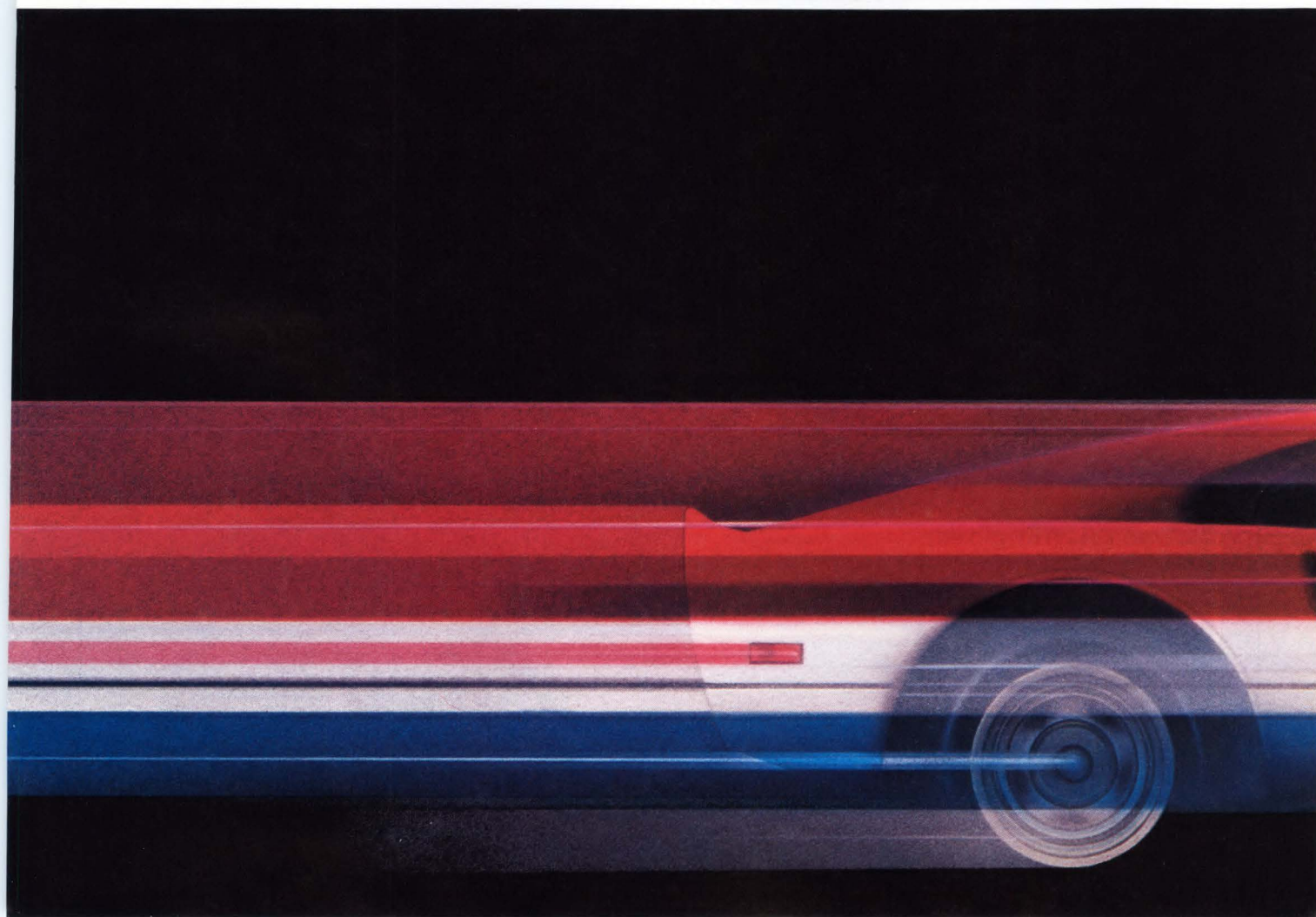
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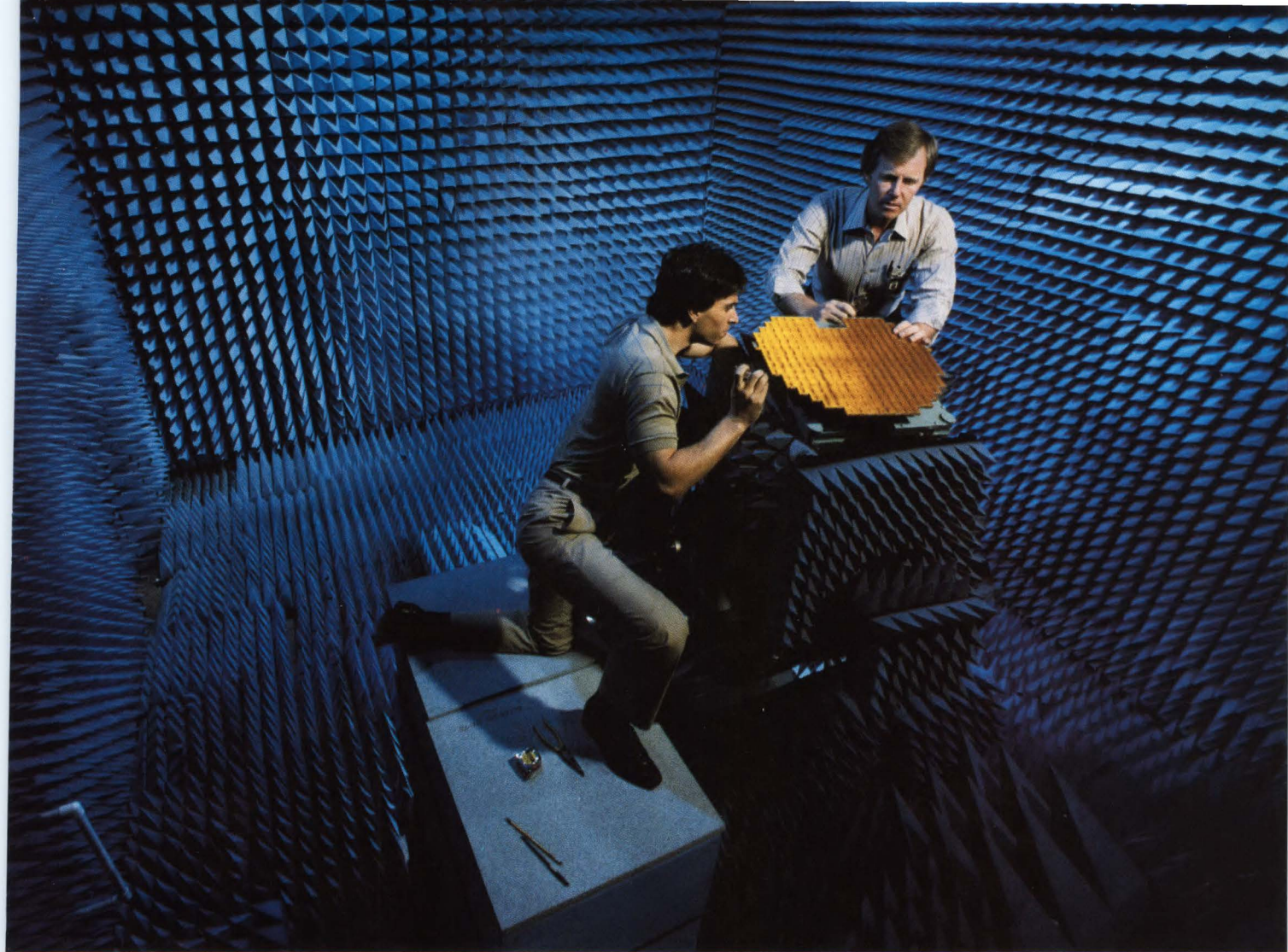
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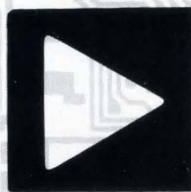
You should have a BSEE with 3-5 years engineering experience within the electronic industry. You should also possess strong managerial skills. Business degree a plus.

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Interested applicants should forward a resume or letter stating experience, including salary history, to Bob Pothler, Analog Devices, Inc., Microelectronics Division, 831 Woburn St., Wilmington, MA 01887 or call him at 617-657-7960, ext. 3212.

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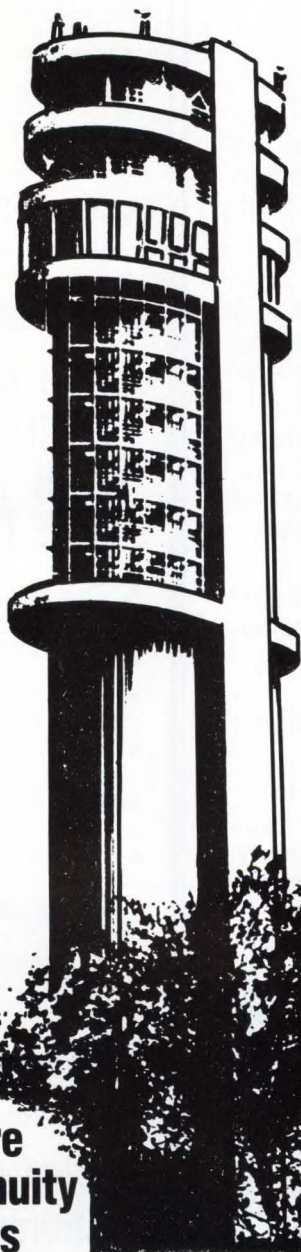


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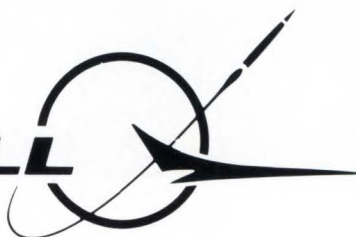
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You will perform design and development of wiring and electrical/electronic component integration and installation. Activities include determination of requirements, selection of wire and electrical components, integration of and interconnect system for wires, cables, connectors, junction boxes, switch panels, and all components and subsystems of the electrical power and electronic systems. Tasks include working with MIL-SPECS and standard parts, generation of installation concepts and complex layouts, direct drafting of releasable drawings and performing liaison with manufacturing and engineering mock-ups. BS in Engineering required.

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EMP Analysis

You will perform design analysis and testing to assess airborne and ground based electrical/electronic systems relative to nuclear EMP phenomena. Analysis encompasses the use of computer code and mathematical models to determine the electromagnetic coupling paths and transfer functions from the external EMP environment to selected circuits within the systems. Tasks involve laboratory testing and analysis at the component through subsystem level to determine upset and damaged thresholds, planning and performing system level EMP tests when system is exposed to pulsed and CW simulated fields and providing design solutions to EMP hardened systems, and laboratory experiments to assess and verify hardening of systems. You will also translate free field EMP environments to avionics component design requirements, pin injection voltages as a function of cable configuration, component surface currents, resultant internal fields and effects on circuits. BS in Engineering required.

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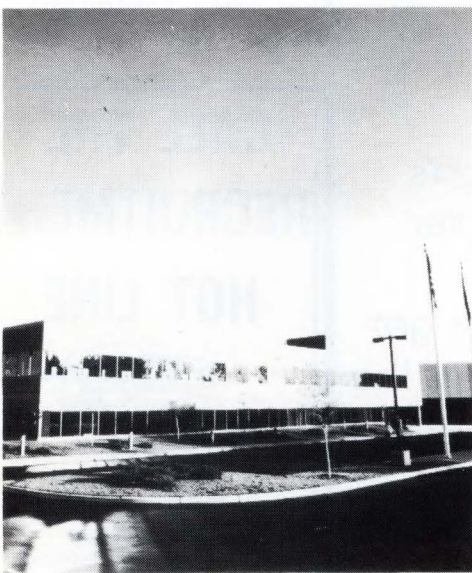
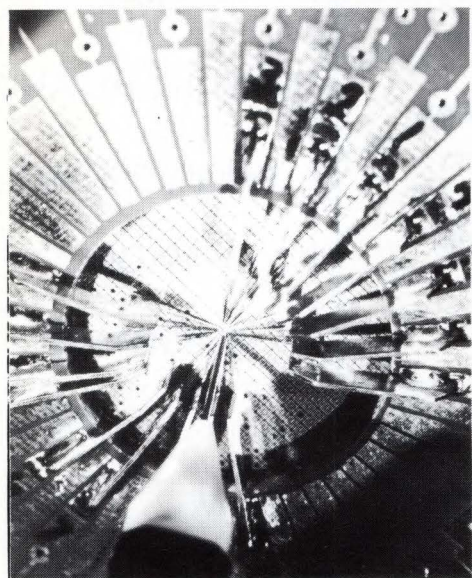
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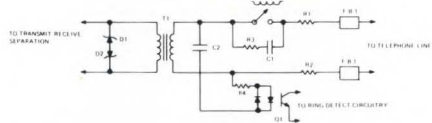


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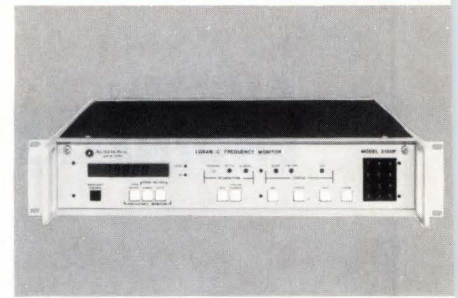
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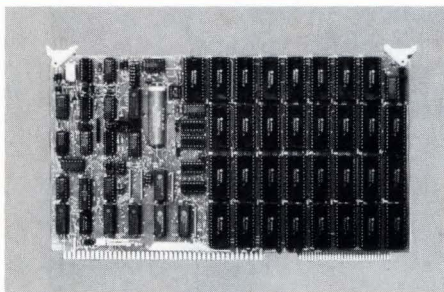
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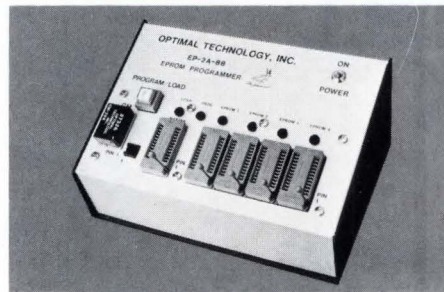
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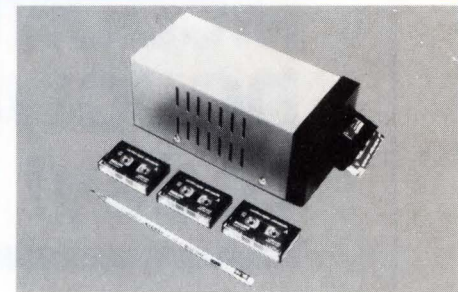
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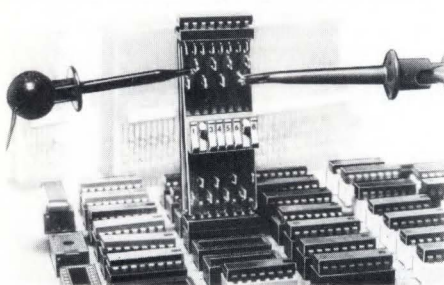
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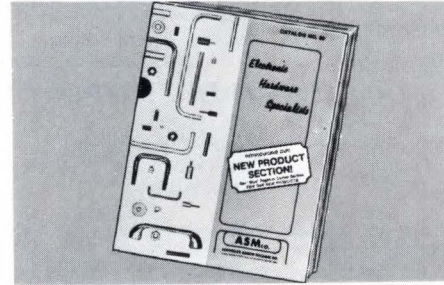
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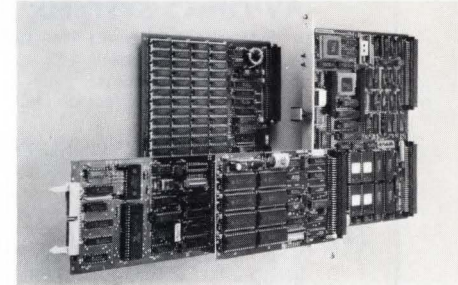
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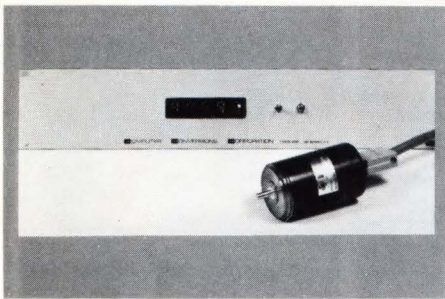
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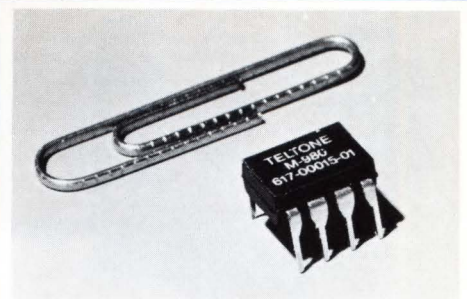
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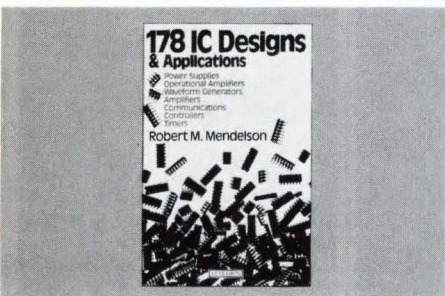
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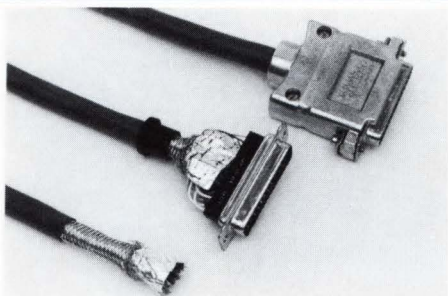
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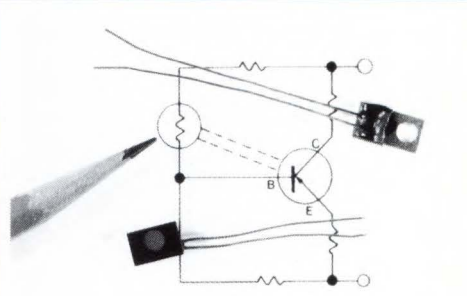
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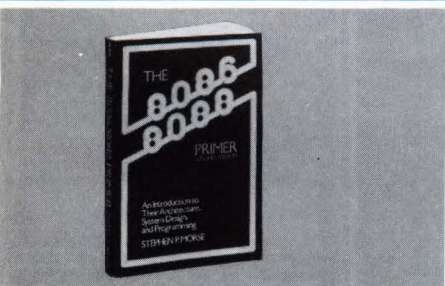
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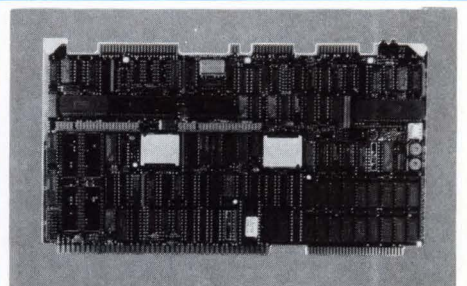
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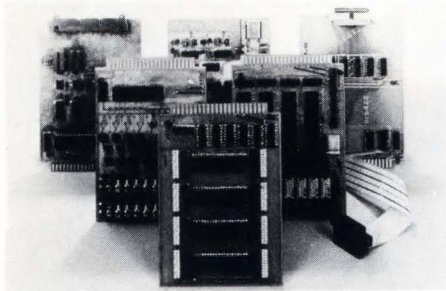
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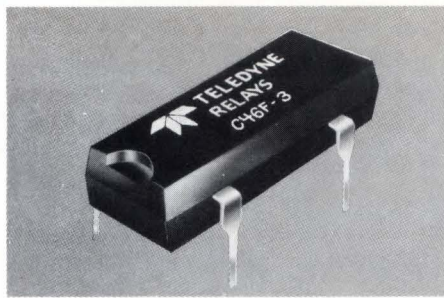
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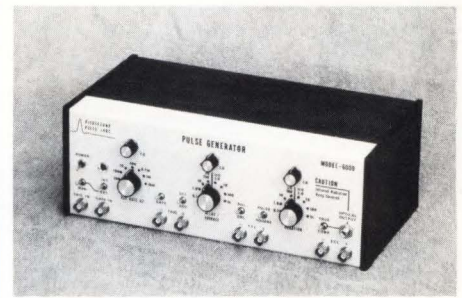
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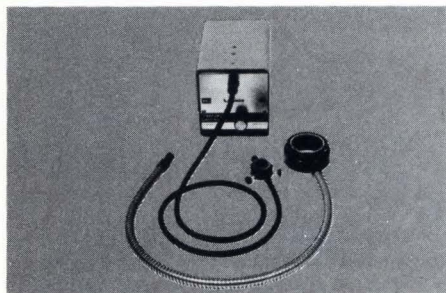
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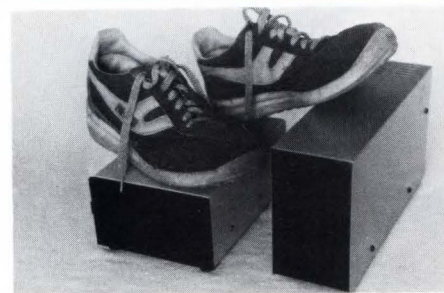
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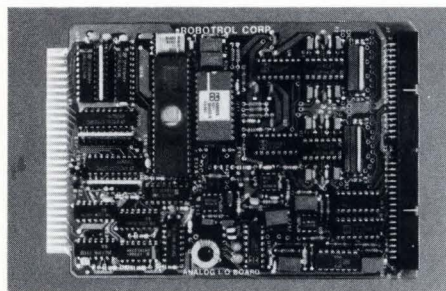
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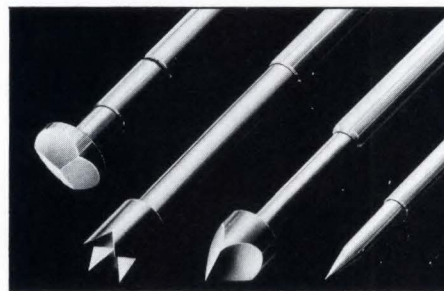
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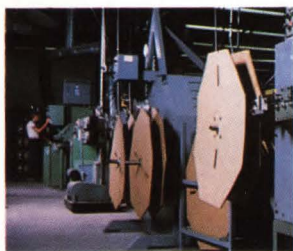
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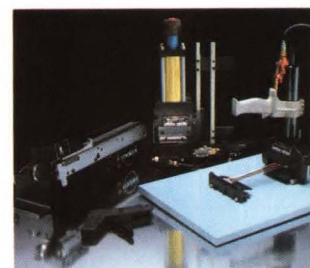
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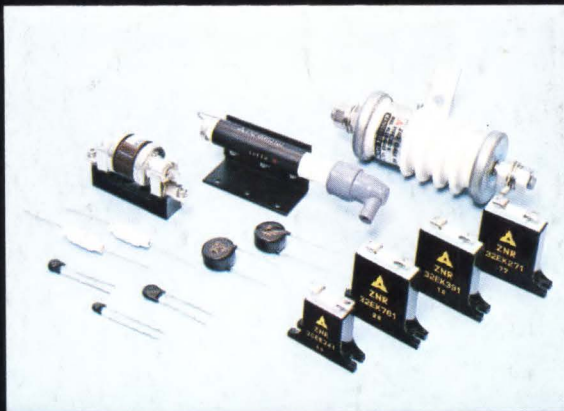
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